REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add parameter I_{LIR} to table I. Remove vendor CAGE 34335. Change drawing CAGE code. Editorial changes throughout.	89-03-01	Monica L. Poelking
B	Changes in accordance with NOR 5962-R022-99. – LTG	99-01-28	Monica L. Poelking
C	Correct supply voltage range in paragraph 1.3. Delete I_{OH} and I_{OL} in footnote 4/ in table I. Update boilerplate. Editorial changes throughout. – TVN	00-07-14	Monica L. Poelking
D	Update boilerplate to MIL-PRF-38535 requirements. – CFS	05-08-22	Thomas M. Hess

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	D																		
SHEET	15																		

REV STATUS OF SHEETS																
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

PREPARED BY
Greg A. Pitz

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Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
87-03-10

REVISION LEVEL
D

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, NMOS, PROGRAMMABLE INTERRRUPT CONTROLLER, MONOLITHIC SILICON

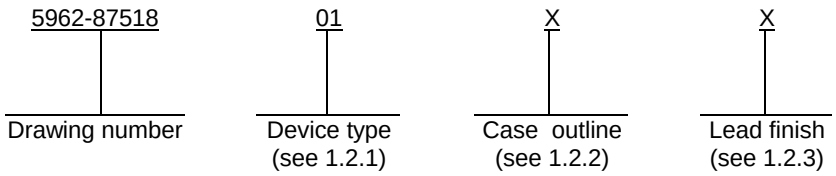
SIZE	CAGE CODE	
A	**67268**	**5962-87518**

SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	8259A	Programmable interrupt controller

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
3	CQCC1-N28	28	Square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range ..... -0.5 V dc to +7 V dc
Input voltage range ..... -0.5 V dc to +7 V dc
Maximum power dissipation (P_D) ..... 1.0 W
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 5 seconds) ..... +270°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Minimum low level input voltage (V_{IL}) ..... -0.5 V dc
Minimum high level input voltage (V_{IH}) ..... +2.3 V dc
Maximum low level input voltage (V_{IL}) ..... +0.8 V dc
Maximum high level input voltage (V_{IH}) ..... V_{CC} + 0.5 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the Qualifying Activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, Appendix A. The compliance indicator “C” shall be replaced with a “Q” or “QML” certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the “Q” or “QML” certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.7 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}	V_{CC} = 5 V ±10%	All	1, 2, 3		0.8 1/	V
Input high voltage	V_{IH}	V_{CC} = 5 V ±10%	All	1, 2, 3	2.3		V
Low level output voltage	V_{OL}	V_{CC} = 5 V ±10%, I_{OL} = 2.2 mA	All	1, 2, 3		0.45	V
High level output voltage	V_{OH}	V_{CC} = 5 V ±10%, I_{OH} = -400 µA	All	1, 2, 3	2.4		V
Interrupt high level output voltage	$V_{OH (INT)}$	V_{CC} = 4.5 V, I_{OH} = -100 µA	All	1, 2, 3	3.5		V
		I_{OH} = -400 µA			2.4		
Input load current	I_{LI}	V_{CC} = 5.5 V V_{IN} = 0.0 V to 5.5 V	All	1, 2, 3	-10 2/	+10	µA
Input load current, IR0-IR7	I_{LIR}	V_{CC} = 5.5 V V_{IN} = 0.0 V to 5.5 V	All	1, 2, 3	-300 2/	+10	µA
Output leakage current	I_{LOL}	V_{CC} = 5.5 V V_{OUT} = 0.45 V to 4.5 V	All	1, 2, 3	-10 2/	+10	µA
	I_{LOH}	V_{CC} = 5.5 V, V_{OUT} = V_{CC}				+10	
V_{CC} supply current	I_{CC}	V_{CC} = 5.5 V 3/ Outputs load static	All	1, 2, 3		125	mA
Input capacitance	C_{IN}	T_C = +25°C, f_C = 1 MHz See 4.3.1d	All	4		10	pF
I/O capacitance	$C_{I/O}$	T_C = +25°C See 4.3.1d		4		20	
Functional test		See 4.3.1c	All	7, 8			
A_0/$\overline{CS}$ setup to $\overline{RD}$ / $\overline{INTA}$ falling	t_{AHRL}	See figure 3 4/	All	9, 10, 11	0		ns
A_0/$\overline{CS}$ hold after $\overline{RD}$ / $\overline{INTA}$ rising	t_{RHAX}		All	9, 10, 11	0		ns
$\overline{RD}$ pulse width	t_{RLRH}		All	9, 10, 11	235		ns
A_0/$\overline{CS}$ setup to $\overline{WR}$ falling	t_{AHWL}		All	9, 10, 11	0		ns
A_0/$\overline{CS}$ hold after $\overline{WR}$ rising	t_{WHAX}		All	9, 10, 11	0		ns
$\overline{WR}$ pulse width	t_{WLWH}		All	9, 10, 11	290		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Data setup to $\overline{WR}$ rising	t_{DVWH}	See figure 3 4/	All	9, 10, 11	240		ns
Data hold after $\overline{WR}$ rising	t_{WHDX}		All	9, 10, 11	0		ns
Interrupt request width (low) 5/	t_{JLJH}		All	9, 10, 11	100		ns
Cascade setup to second or third $\overline{INTA}$ falling (slave only)	t_{CVIAL}		All	9, 10, 11	55		ns
End of $\overline{RD}$ to next command	t_{RHRL}		All	9, 10, 11	300		ns
End of $\overline{WR}$ to next command	t_{WHRL}		All	9, 10, 11	370		ns
Data valid from $\overline{RD}$ / $\overline{INTA}$ falling 6/	t_{RLDV}		All	9, 10, 11		200	ns
Data float after $\overline{RD}$ / $\overline{INTA}$ rising 6/	t_{RHDZ}		All	9, 10, 11	10 2/	100	ns
Interrupt output delay 6/	t_{JHIH}		All	9, 10, 11		350	ns
Cascade valid from first $\overline{INTA}$ falling (master only) 6/	t_{IALCV}		All	9, 10, 11		565	ns
Enable active from $\overline{RD}$ falling or $\overline{INTA}$ falling 6/	t_{RLEL}		All	9, 10, 11		125	ns
Enable inactive from $\overline{RD}$ rising or $\overline{INTA}$ rising 6/	t_{RHEH}		All	9, 10, 11		150	ns
Data valid from stable address 6/	t_{AHDV}		All	9, 10, 11		200	ns
Cascade valid to valid data 6/	t_{CVDV}		All	9, 10, 11		300	ns

See footnotes on next sheet.

TABLE I. Electrical performance characteristics - Continued.

1/ Due to the test equipment limitations, actual tested values may differ from those specified but specific limits are guaranteed.

2/ Guaranteed if not tested to the limits specified.

3/ I_{CC} is measured in a static condition with outputs in a worst case state having standard I_{OL}/I_{OH} loads applied.

4/ Test conditions: V_{CC} = 5 V ±10%, V_{IL} = 0.45 V, V_{IH} = 2.4 V, V_{OL} = 0.8 V, V_{OH} = 2.0 V (see figure 3).

5/ This is low time required to clear the input latch in the edge triggered mode.

6/ Test conditions: Capacitance of data bus: Maximum test = 100 pF, minimum test = 15 pF, C_{IN} = 100 pF, C_{ENABLE} = 15 pF (see figure 3).

Device type	All		
Case outlines	X and 3		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{CS}$	15	CAS2
2	$\overline{WR}$	16	$\overline{SP}$ / $\overline{EN}$
3	$\overline{RD}$	17	INT
4	D_7	18	IR0
5	D_6	19	IR1
6	D_5	20	IR2
7	D_4	21	IR3
8	D_3	22	IR4
9	D_2	23	IR5
10	D_1	24	IR6
11	D_0	25	IR7
12	CAS0	26	$\overline{INTA}$
13	CAS1	27	A_0
14	GND	28	V_{CC}

FIGURE 1. Terminal connections.

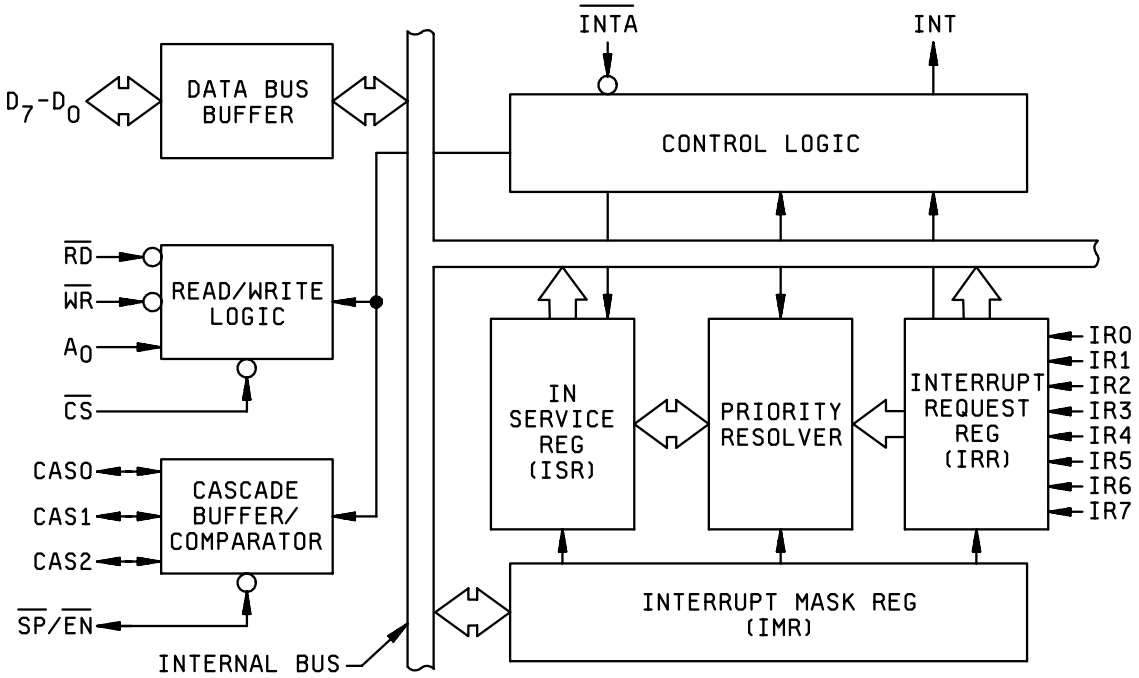
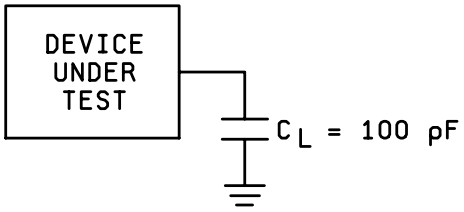
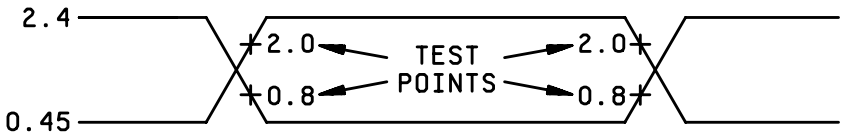


FIGURE 2. Block diagram.



NOTE: C_L includes jig capacitance.

INPUT/OUTPUT WAVEFORM



NOTES:
1. AC testing inputs are driven at 2.4 V for a logic “1” and 0.45 V for a logic “0”.
2. Timing measurements are made at 2.0 V for a logic “1” and 0.8 V for a logic “0”.

FIGURE 3. Test circuit and switching waveforms.

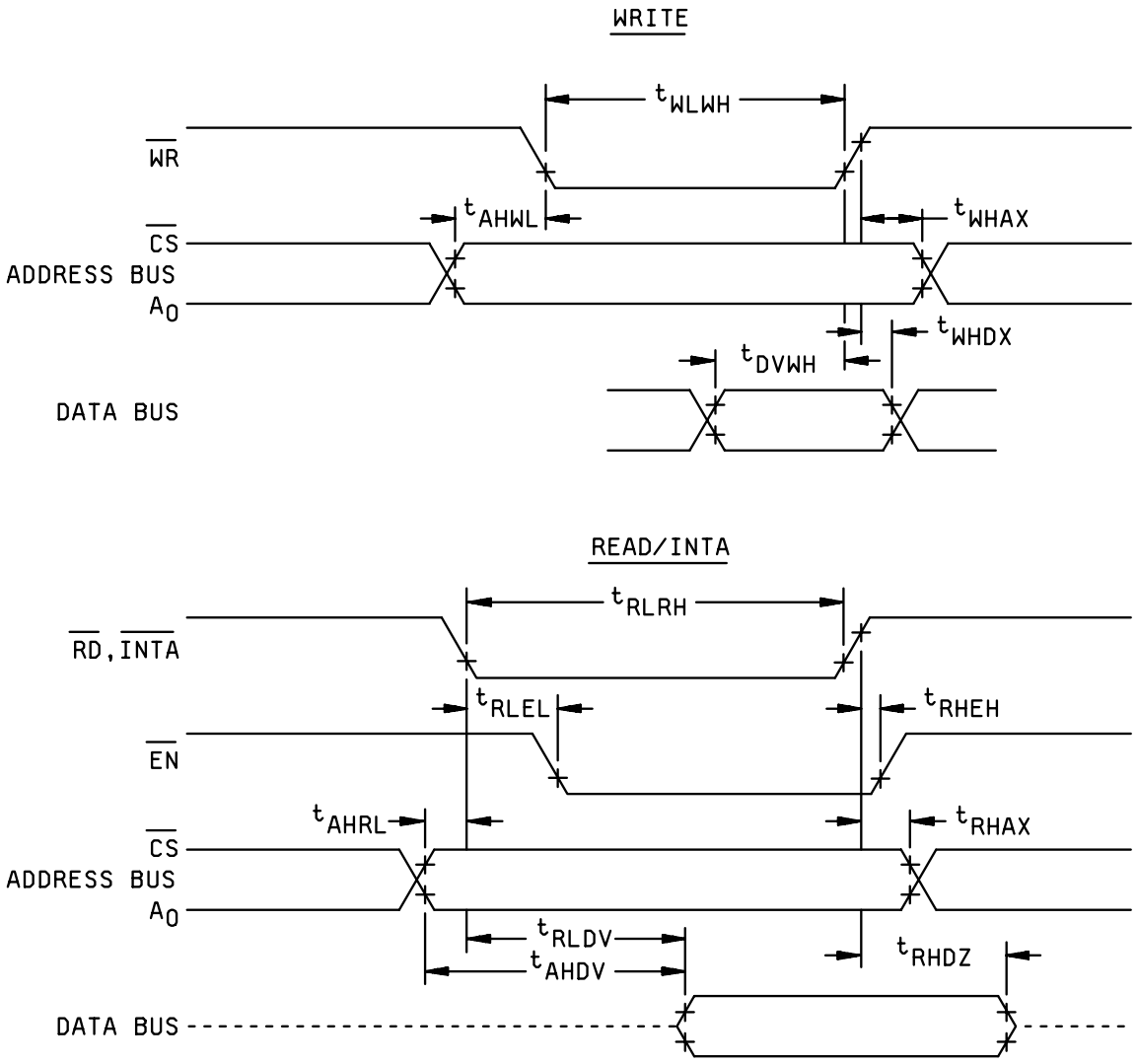
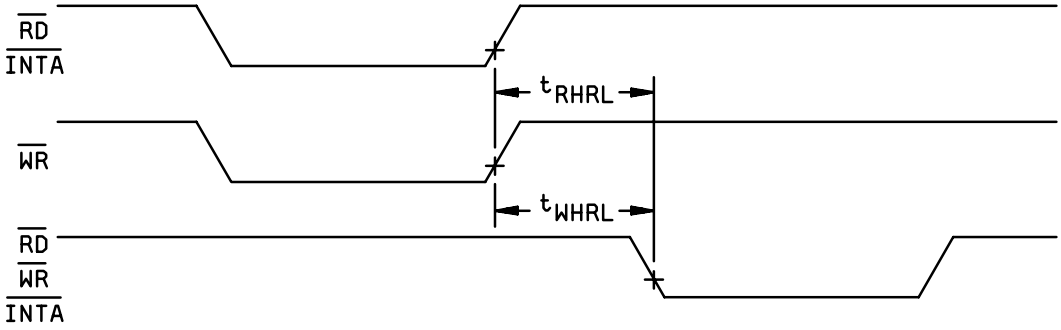
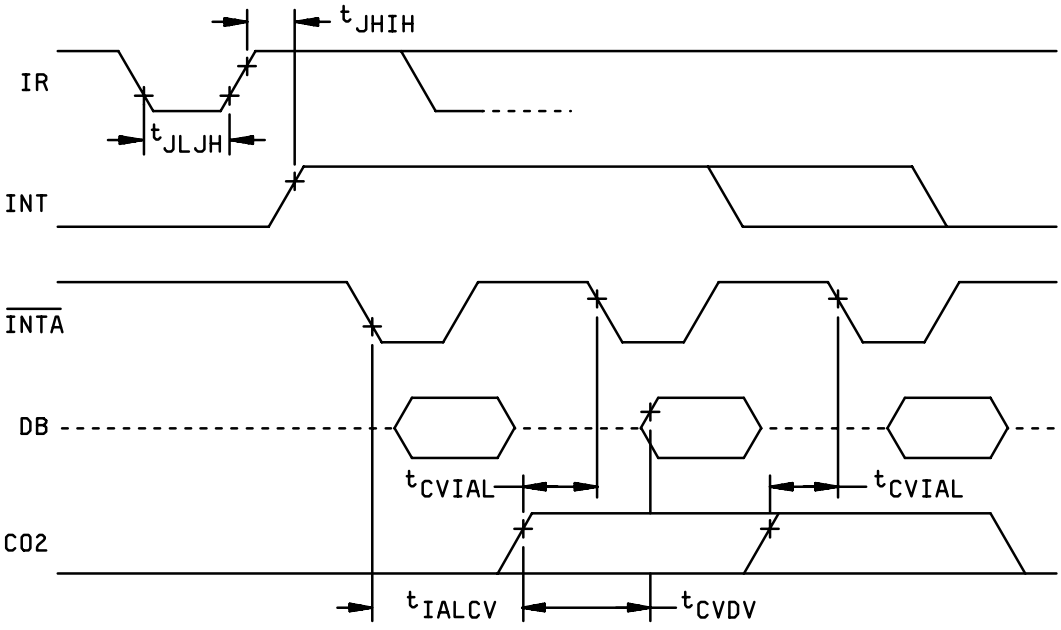


FIGURE 3. Test circuit and switching waveforms - Continued.

RECOVERY TIME



INTA SEQUENCE



NOTES:

1. Interrupt output must remain in HIGH at least until leading edge of first $\overline{\text{INTA}}$.
2. Cycle 1 in iAPX86, and iAPX88 systems, the data bus is not active.

FIGURE 3. Test circuit and switching waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8A, 10
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 testing shall be sufficient to verify the functional operation of the device.

d. Subgroup 4 (C_{IN} and $C_{I/O}$ measurements) shall be measured initially and after process or design changes which may affect input or output capacitance. A minimum sample size of five devices with zero rejects shall be required.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614)-692-0547.

6.6 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and table III herein.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Pin description.

Pin number	Pin name	I/O	Description
28	V_{CC}		Power: +5 V supply
14	GND		Ground.
1	$\overline{CS}$	I	Chip select: A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the device. $\overline{INTA}$ functions are independent of $\overline{CS}$.
2	$\overline{WR}$	I	Write: A low on this pin when $\overline{CS}$ is low enables the device to accept command words from the CPU.
3	$\overline{RD}$	I	Read: A low on this pin when $\overline{CS}$ is low enables the device to release status onto the data bus for the CPU.
4 – 11	D7 – D0	I/O	Bidirectional data bus: Control status and interrupt-vector information are transferred via the bus.
12, 13, 15	CAS0 - CAS2	I/O	Cascade lines: The CAS lines form a private device bus to control a multiple device structure. These pins are outputs for a master device and inputs for a slave device.
16	$\overline{SP}$ / $\overline{EN}$	I/O	Slave program/enable buffer: This is a dual function pin. When in the buffered mode, it can be used as an output to control buffer transceivers ($\overline{EN}$). When not in the buffered mode, it is used as an input to designate as a master ($\overline{SP}$ = 1) or slave ($\overline{SP}$ = 0)
17	INT	O	Interrupt: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
18 – 25	IR0 – IR7	I	Interrupt requests: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (edge triggered mode), or just by a high level on an IR input (level triggered mode).
26	$\overline{INTA}$	I	Interrupt acknowledge: This pin is used to enable device interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
27	A_0	I	A_0 address line: This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the device to decipher various command words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A_0 address line (A_1 for iAPX 86, 88).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-08-22

Approved sources of supply for SMD 5962-87518 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and/or QML-38535 during the next revision. MIL-HDBK-103 and/or QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and/or QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8751801XA	3V146	MD8259A/B
5962-87518013A	3V146	MR8259A/B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics 10 Malcolm Hoyt Drive Newburyport, MA 01950