REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical changes to table I. Editorial changes throughout.	92-10-27	Monica L. Poelking
B	Changes in accordance with NOR 5962-R019-99.	99-01-28	Monica L. Poelking
C	Incorporated revision B and updated boilerplate and editorial changes throughout. Added Rochester Electronics as source of supply CAGE code 3V146. - LTG	00-10-19	Thomas M. Hess
D	Update boilerplate to MIL-PRF-38535 requirements. - LTG	01-04-02	Thomas M. Hess
E	Update boilerplate to current MIL-PRF-38535 requirements. - CFS	07-06-25	Thomas M. Hess

REV																				
SHEET																				
REV	E																			
SHEET	15																			
REV STATUS			REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E			
OF SHEETS			SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A

PREPARED BY
Ray Monnin

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
D. A. DiCenzo

APPROVED BY
N. A. Hauck

DRAWING APPROVAL DATE
87-07-02

REVISION LEVEL
E

MICROCIRCUIT, DIGITAL, PROGRAMMABLE PERIPHERAL INTERFACE, MONOLITHIC SILICON

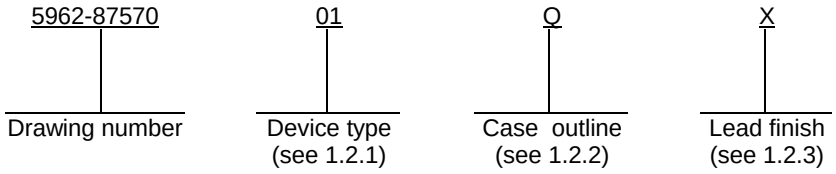
SIZE	CAGE CODE	
A	**67268**	**5962-87570**

SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	8255A	Programmable peripheral interface
02	8255A-5	Programmable peripheral interface

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GCIP1-T40 or CDIP2-T40	40	Dual-in-line
X	CQCC1-N44	44	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range ..... -0.5 V dc to +7.0 V dc
Input voltage range ..... -0.5 V dc to +7.0 V dc
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 1.0 W 1/
Thermal resistance, junction-to-case (θ_{JC}):
Case Q ..... See MIL-STD-1835
Case X ..... See MIL-STD-1835
Junction temperature (T_J) ..... +126.9°C
Lead temperature (soldering, 10 seconds) ..... +300°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +5.0 V dc ±10 percent
Minimum high level input voltage (V_{IH}) ..... +2.2 V dc
Maximum low level input voltage (V_{IL}) ..... +0.8 V dc
Minimum low level input voltage (V_{IL}) ..... -0.5 V dc
Maximum high level input voltage (V_{IH}) ..... +5.5 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the "Q" or "QML" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low-level input voltage	V_{IL}	V_{CC} = 5.5 V, V_{CC} = 4.5 V	All	1, 2, 3		0.8	V
High-level input voltage	V_{IH}	V_{CC} = 5.5 V, V_{CC} = 4.5 V	All	1, 2, 3	2.2		V
Output low voltage-DATABUS	V_{OL}	V_{CC} = 5.5 V, I_{OL} = 2.5 mA	All	1, 2, 3		0.45	V
Output low voltage-PORTS	V_{OL}	V_{CC} = 5.5 V, I_{OL} = 1.7 mA	All	1, 2, 3		0.45	V
Output high voltage-DATABUS	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -400 µA	All	1, 2, 3	2.4		V
Output high voltage-PORTS	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -200 µA	All	1, 2, 3	2.4		V
Darlington drive current	I_{DAR}	V_{CC} = 5.5 V, V_{CC} = 4.5 V (Ports B and C)	All	1, 2, 3	-1.0	-4.0	mA
Power supply current	I_{CC}	V_{CC} = 5.5 V 1/	All	1, 2, 3		120	mA
Input load current	I_{IL}	V_{CC} = 5.5 V V_{IN} = 5.5 V to 0.0 V	All	1, 2, 3	-10.0	+10.0	µA
Output float leakage	I_{OFL}	V_{CC} = 5.5 V V_{OUT} = 5.5 V to 0.45 V	All	1, 2, 3	-10.0	+10.0	µA
Input capacitance	C_{IN}	T_C = +25°C, F_C = 1 MHz See 4.3.1c	All	4		25	pF
I/O capacitance	$C_{I/O}$	T_C = +25°C, see 4.3.1c Unmeasured pins are returned to ground. V_{CC} = GND = 0.0 V	All	4		25	pF
Functional tests		See 4.3.1d	All	7, 8			
Address stable before READ	t_{AR}	V_{CC} = 5.5 V, 4.5V V_{IH} = 2.4 V, V_{IL} = 0.45 V V_{OH} = 2.0 V, V_{OL} = 0.8 V C_L = 100 pF See figure 4	All	9, 10, 11	0.0		ns
Address stable after READ	t_{RA}		All	9, 10, 11	0.0		ns
READ pulse width	t_{RR}		All	9, 10, 11	300.0		ns
Data valid from READ	t_{RD}		01	9, 10, 11		250.0	ns
			02	9, 10, 11		200.0	
Data float after READ	t_{DF} 2/		01	9, 10, 11	10.0 3/	150.0	ns
			02	9, 10, 11	10.0	100.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Time between READS and/or WRITES	t_{RV}	V_{CC} = 5.5 V, 4.5V V_{IH} = 2.4 V, V_{IL} = 0.45 V V_{OH} = 2.0 V, V_{OL} = 0.8 V C_L = 100 pF See figure 4	All	9, 10, 11	850.0 3/		ns
Address stable before WRITE	t_{AW}		All	9, 10, 11	0.0		ns
Address stable after WRITE	t_{WA}		All	9, 10, 11	20.0		ns
Write pulse width	t_{WW}		01	9, 10, 11	400.0		ns
			02	9, 10, 11	300.0		
Data valid to WRITE (T. E.)	t_{DW}		All	9, 10, 11	100.0		ns
Data valid after WRITE	t_{WD}		All	9, 10, 11	30.0		ns
WRITE = 1 to output	t_{WB}		All	9, 10, 11		350.0	ns
Peripheral data before READ	t_{IR}		All	9, 10, 11	0.0		ns
Peripheral data after READ	t_{HR}		All	9, 10, 11	0.0		ns
ACK pulse width	t_{AK}		All	9, 10, 11	300.0		ns
STB pulse width	t_{ST}		All	9, 10, 11	500.0		ns
Peripheral data before T. E. of STB	t_{PS}		All	9, 10, 11	0.0		ns
Peripheral data after T. E. of STB	t_{PH}		All	9, 10, 11	180.0		ns
ACK = 0 to output	t_{AD}		All	9, 10, 11		300.0	ns
ACK = 1 to output float	t_{KD} 3/		All	9, 10, 11	20.0 3/	250.0 3/	ns
WRITE = 1 to OBF = 0	t_{WOB}		All	9, 10, 11		650.0	ns
ACK = 0 to OBF = 1	t_{AOB}		All	9, 10, 11		350.0	ns
STB = 0 to IBF = 1	t_{SIB}		All	9, 10, 11		300.0	ns
READ = 1 to IBF = 0	t_{RIB}		All	9, 10, 11		300.0	ns
READ = 0 to INTR = 0	t_{RIT}		All	9, 10, 11		400.0	ns
STB = 1 to INTR = 1	t_{SIT}		All	9, 10, 11		300.0	ns
ACK = 1 to INTR = 1	t_{AIT}		All	9, 10, 11		350.0	ns
WRITE = 0 to INTR = 0 4/	t_{WIT}		All	9, 10, 11		850.0	ns

1/ I_{CC} test conditions: The supply current is measured with loaded outputs while running ac patterns.
2/ AC float timing parameters t_{DF} and t_{KD} are tested logic 0 to float only.
3/ Guaranteed if not tested.
4/ When measured from WRITE = 0 to INTR = 0, the limits shall be as follows: For device type 01, maximum limit shall be as specified at 850 ns.

Device type	All		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	PA_3	23	PB_4
2	PA_2	24	PB_5
3	PA_1	25	PB_6
4	$\overline{PA_0}$	26	PB_7
5	$\overline{RD}$	27	V_{CC}
6	$\overline{CS}$	28	NC
7	GND	29	NC
8	NC	30	D_7
9	A_1	31	D_6
10	A_0	32	D_5
11	PC_7	33	D_4
12	PC_6	34	D_3
13	PC_5	35	D_2
14	PC_4	36	D_1
15	PC_0	37	D_0
16	PC_1	38	RESET
17	PC_2	39	$\overline{NC}$
18	PC_3	40	WR
19	PB_0	41	PA_7
20	PB_1	42	PA_6
21	PB_2	43	PA_5
22	PB_3	44	PA_4

Device type	All		
Case outline	Q		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	PA_3	21	PB_3
2	PA_2	22	PB_4
3	PA_1	23	PB_5
4	$\overline{PA_0}$	24	PB_6
5	$\overline{RD}$	25	PB_7
6	CS	26	V_{CC}
7	GND	27	D_7
8	A_1	28	D_6
9	A_0	29	D_5
10	PC_7	30	D_4
11	PC_6	31	D_3
12	PC_5	32	D_2
13	PC_4	33	D_1
14	PC_0	34	D_0
15	PC_1	35	$\overline{RESET}$
16	PC_2	36	WR
17	PC_3	37	PA_7
18	PB_0	38	PA_6
19	PB_1	39	PA_5
20	PB_2	40	PA_4

FIGURE 1. Terminal connections.

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input operation (read)
0	0	0	1	0	Port A-data bus
0	1	0	1	0	Port B-data bus
1	0	0	1	0	Port C-data bus
					Output operation (write)
0	0	1	0	0	Data bus-port A
0	1	1	0	0	Data bus-port B
1	0	1	0	0	Data bus-port C
1	1	1	0	0	Data bus-control
					Disable function
X	X	X	X	1	Data bus-three-state
1	1	0	1	0	Illegal condition
X	X	1	1	0	Data bus three-state

FIGURE 2. Truth table.

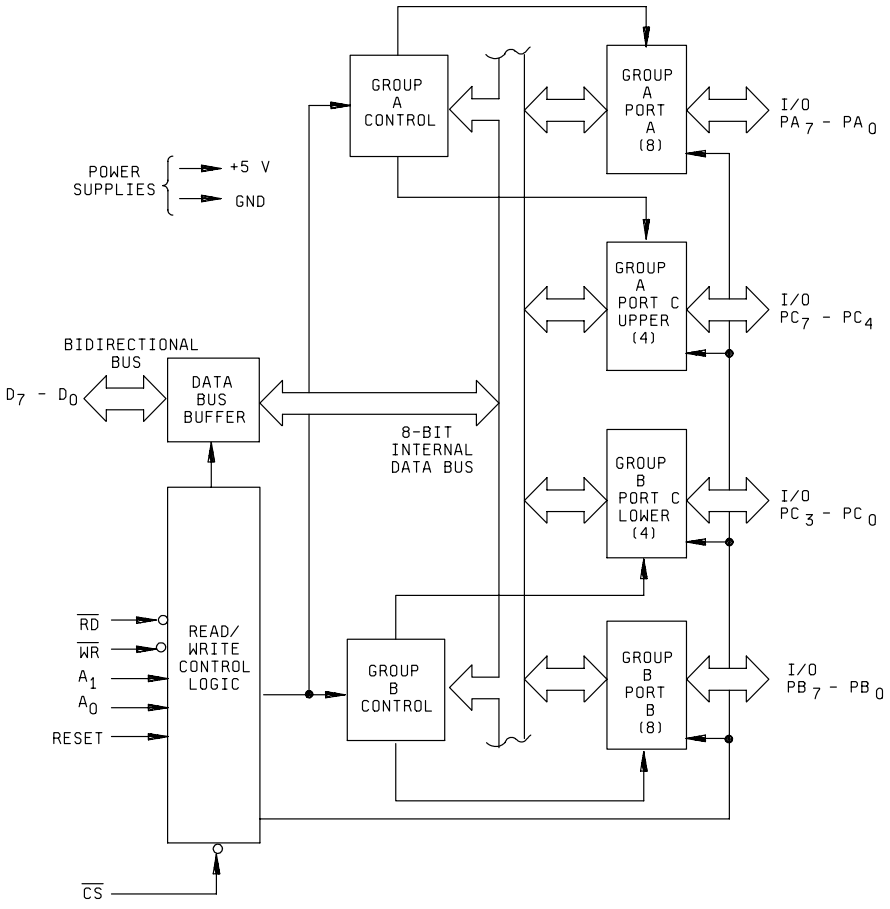
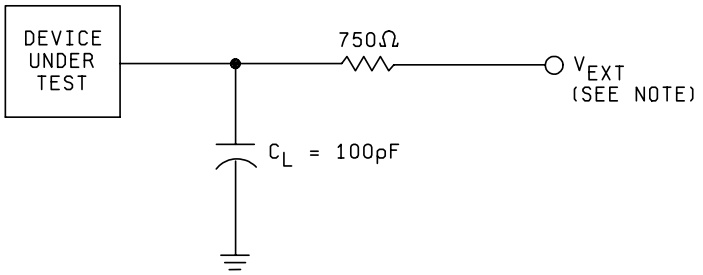
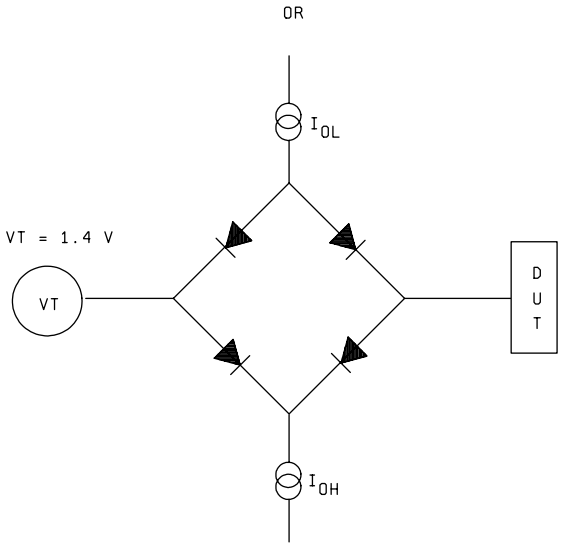


FIGURE 3. Logic diagram.

AC testing load circuits

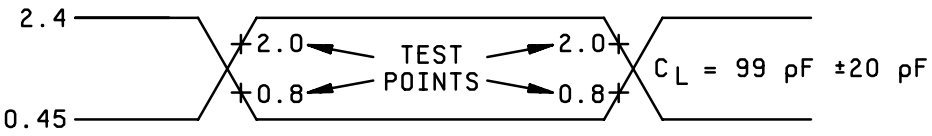


NOTE: V_{EXT} is set at various voltages during testing to guarantee the specification.



NOTE: This test circuit is the dynamic load.

AC testing input and output waveforms



NOTE: AC testing. Inputs are driven at 2.4 V for a logic “1” and 0.45 V for a logic “0”. Timing measurements are made at 2.0 V for a logic “1” and 0.8 V for a logic “0”.

FIGURE 4. Timing waveforms.

Switching waveforms

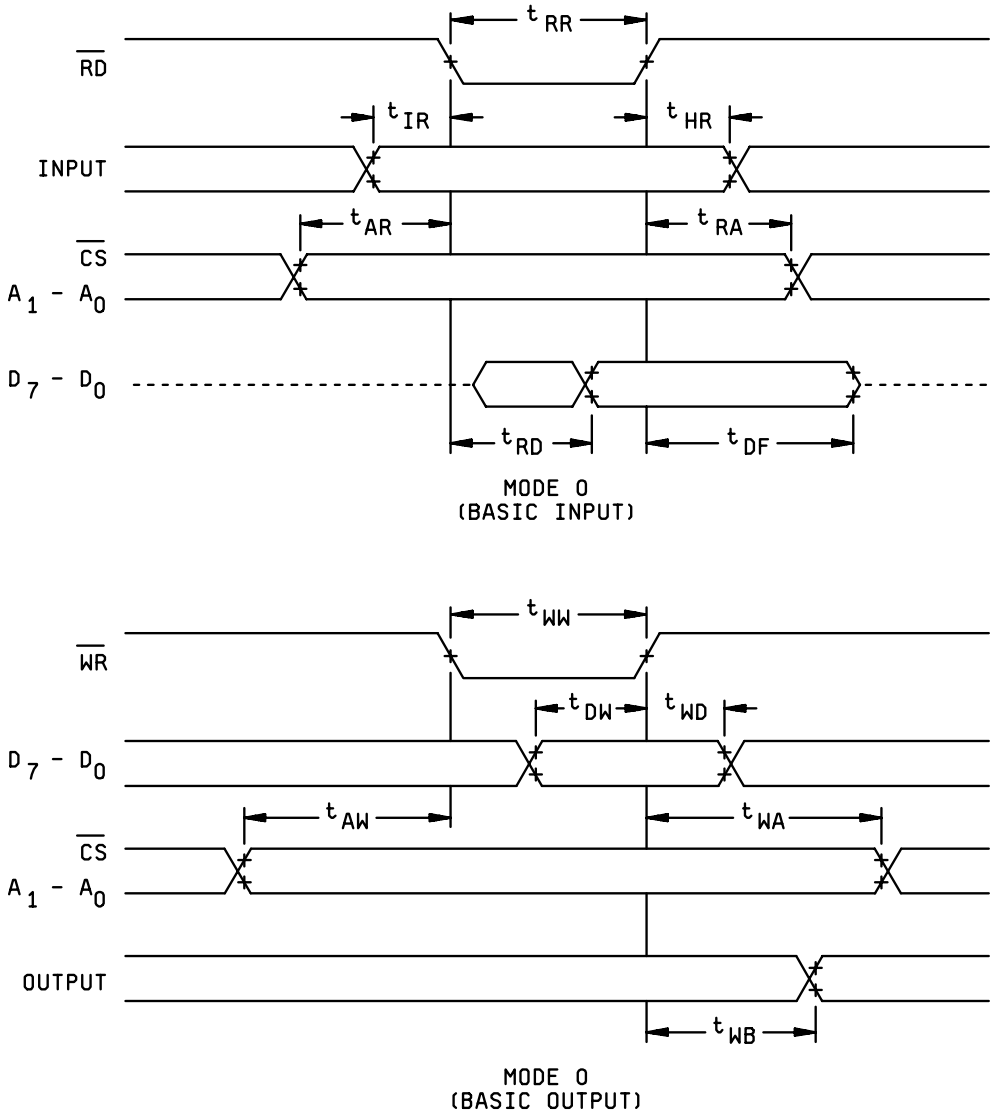
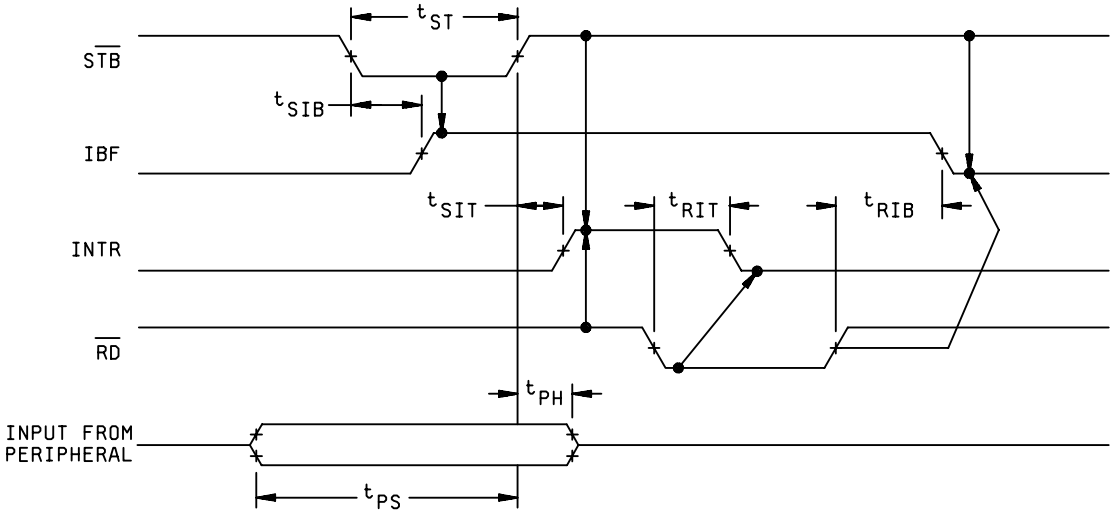
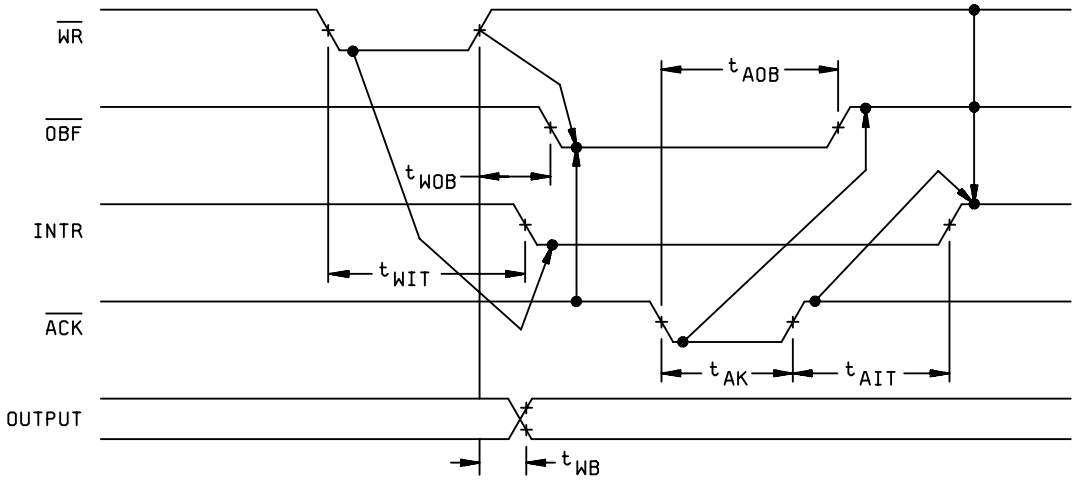


FIGURE 4. Timing waveforms - Continued.

Switching waveforms



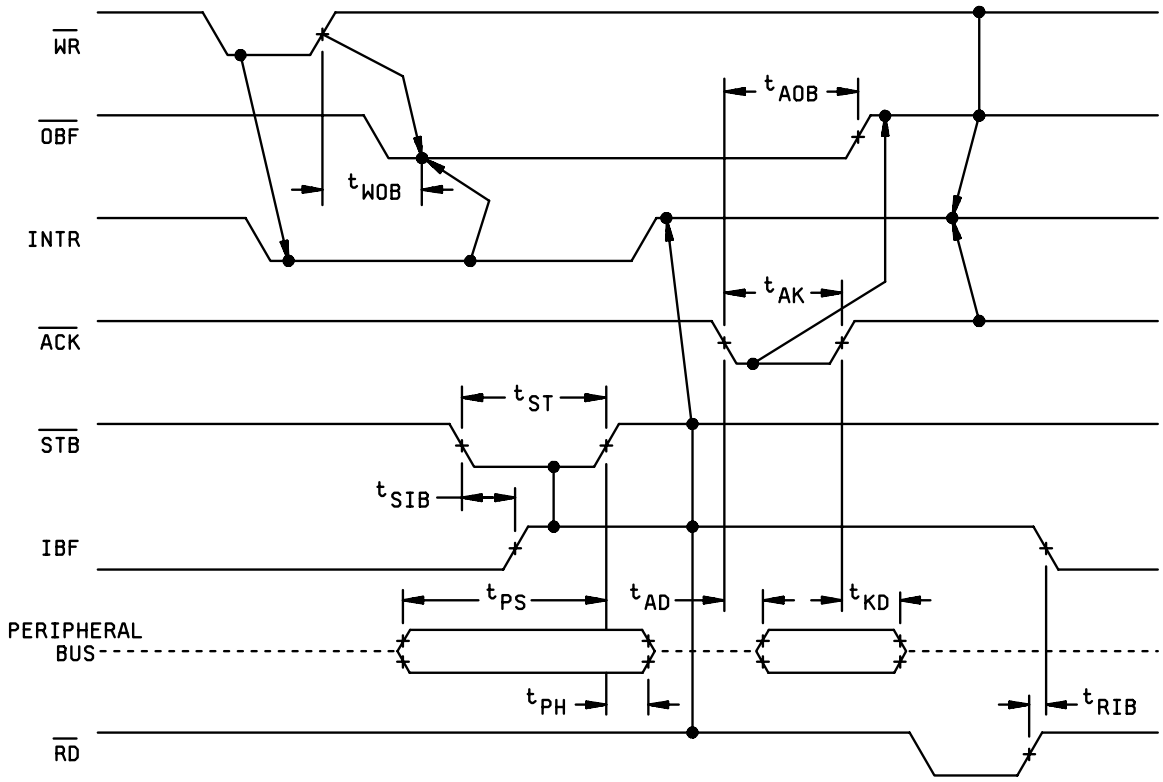
MODE 1 (STROBED INPUT)



MODE 1 (STROBED OUTPUT)

FIGURE 4. Timing waveforms - Continued.

Switching waveforms



MODE 2
(BIDIRECTIONAL)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occur before $\overline{RD}$ is permissible (INTR = IBF • MASK • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • MASK • $\overline{ACK}$ • $\overline{WR}$).

FIGURE 4. Timing waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3 or 2, 8A, 10

1/ PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero failures shall be required.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Pin descriptions. The following pin descriptions are applicable to this drawing.

Pin no. case X	Pin no. case Q	Name	I/O	Pin description
30-37	27-34	D7-D0	I/O	Data bus (bidirectional)
38	35	Reset	I	Reset input
6	6	$\overline{CS}$	I	Chip select
5	5	$\overline{RD}$	I	Read input
40	36	$\overline{WR}$	I	Write input
10,9	9, 8	A0, A1	I	Port address
41-44, 1-4	37-40, 1-4	PA7-PA0	I/O	Port A (bit)
26-19	25-18	PB7-PB0	I/O	Port B (bit)
11-15, 18-16	10-13, 17-14	PC7-PC0	I/O	Port C (bit)
27	26	V_{CC}		+5.0 V
7	7	GND		0.0 V

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-06-25

Approved sources of supply for SMD 5962-87570 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8757001QA	3V146	MD8255A/BQA
5962-8757001XA	3V146	MR8255A/BXA
5962-8757002QA	3/	8255A-5

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics Inc. 16 Malcolm Hoyt Drive Newburyport, MA 01950

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