| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Add criteria for QD device types. Add vendor CAGE 3V146. Correct the SMD title. Update boilerplate to MIL-PRF-38535 requirements. - CFS | 02-06-10 | Thomas M. Hess |
| B | Correct the $I_{IL}$ test $V_{CC}$ from 4.5 V to 5.5 V in table I. Correct waveform timing reference 5 on figure 4. - CFS | 02-07-24 | Thomas M. Hess |
| C | Update boilerplate to current MIL-PRF-38535 requirements. - CFS | 07-12-05 | Thomas M. Hess |

**The current CAGE is 67268.**

| REV | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | C | C | C | | | | | | | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | | | | | | | | | | | | | | | | | |

| REV STATUS | REV | C | C | C | C | C | C | C | C | C | C | C | C | C |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

PREPARED BY
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**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
D. A. DiCenzo

APPROVED BY
N. A. Hauck

DRAWING APPROVAL DATE
20 April 1987

MICROCIRCUIT, DIGITAL, BIPOLAR, DYNAMIC MEMORY CONTROLLER, MONOLITHIC SILICON

| REVISION LEVEL | SIZE | CAGE CODE | |
|---|---|---|---|
| C | A | **14933** | **5962-87574** |

SHEET 1 OF 17

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

| 5962-87574 | 01 | Q | X |
|---|---|---|---|
| Drawing number | Device type (see 1.2.1) | Case outline (see 1.2.2) | Lead finish (see 1.2.3) |

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 2964B | Dynamic Memory Controller |

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| Q | GDIP1-T40 or CDIP2-T40 | 40 | Dual-in-line |
| U | CQCC1-N44 | 44 | Square leadless chip carrier |

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range ($V_{CC}$) ..... -0.5 V dc to +7.0 V dc
Input voltage range ..... -0.5 V dc to +5.5 V dc
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation, $P_D$ 1/ ..... 0.9 W at $T_C$ = 125°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case ($\theta_{JC}$) ..... See MIL-STD-1835
Junction temperature ($T_J$) ..... 155°C
DC voltage applied to outputs for high output state ..... -0.5 V dc to $V_{CC}$ maximum
DC output current, into outputs ..... +20 mA
DC input current ..... -30 mA to +5.0 mA

1.4 Recommended operating conditions.

Supply voltage ($V_{CC}$) ..... +4.5 V dc minimum to +5.5 V dc maximum
Minimum high-level input voltage ($V_{IH}$) ..... +2.0 V dc
Maximum low-level input voltage ($V_{IL}$) ..... +0.8 V dc
Case operating temperature range ($T_C$) ..... -55°C to +125°C

1/ Must withstand the added $P_D$ due to short circuit test (e.g., $I_{SC}$).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the "Q" or "QML" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>unless otherwise specified | | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Output high voltage | $V_{OH}$ | $V_{CC}$ = 4.5 V<br>$V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = -1 mA | $\overline{TC}$ | 1, 2, 3 | 01 | 2.5 | | V |
| | | | Others | 1, 2, 3 | 01 | 3.0 | | V |
| Output high voltage | $V_{OH}$ | $V_{CC}$ = 4.5 V<br>$V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = -15 mA | All outputs except $\overline{TC}$ | 1, 2, 3 | 01 | 2.0 | | V |
| Output low voltage | $V_{OL}$ | $V_{CC}$ = 4.5 V<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | All outputs except $\overline{TC}$.<br>$I_{OL}$ = 16 mA | 1, 2, 3 | 01 | | 0.5 | V |
| | | | $\overline{TC}$, $I_{OL}$ = 8 mA | 1, 2, 3 | 01 | | 0.5 | V |
| Input high level | $V_{IH}$ | Guaranteed input logical high voltage for all inputs. | | 1, 2, 3 | 01 | 2.0 | | V |
| Input low level | $V_{IL}$ | Guaranteed input logical low voltage for all inputs. | | 1, 2, 3 | 01 | | 0.8 | V |
| Input clamp voltage | $V_{IC}$ | $V_{CC}$ = 4.5 V; $I_{IN}$ = -18 mA | | 1, 2, 3 | 01 | | -1.5 | V |
| Input low current | $I_{IL}$ | $V_{CC}$ = 5.5 V<br>$V_{IN}$ = 0.4 V | $\overline{RAS}$ | 1, 2, 3 | 01 | | -3.2 | mA |
| | | | $\overline{CAS}$, MSEL, $\overline{RFSH}$ | 1, 2, 3 | 01 | | -1.6 | mA |
| | | | $A_0$-$A_{15}$, $\overline{CLR}$, $RSEL_{0,\ 1}$, LE | 1, 2, 3 | 01 | | -0.4 | mA |
| Input high current | $I_{IH}$ | $V_{CC}$ = 5.5 V<br>$V_{IN}$ = 2.7 V | $\overline{RAS}$ | 1, 2, 3 | 01 | | 100 | µA |
| | | | $\overline{CAS}$, MSEL, $\overline{RFSH}$ | 1, 2, 3 | 01 | | 50 | µA |
| | | | $A_0$-$A_{15}$, $\overline{CLR}$, $RSEL_{0,\ 1}$, LE | 1, 2, 3 | 01 | | 20 | µA |
| Input high current | $I_{IH}$ | $V_{CC}$ = 5.5 V<br>$V_{IN}$ = 5.5 V | $\overline{RAS}$ | 1, 2, 3 | 01 | | 2.0 | mA |
| | | | $\overline{CAS}$, MSEL, $\overline{RFSH}$ | 1, 2, 3 | 01 | | 1.0 | mA |
| | | | $A_0$-$A_{15}$, $\overline{CLR}$, $RSEL_{0,\ 1}$, LE | 1, 2, 3 | 01 | | 0.1 | mA |
| Output short circuit current | $I_{SC}$ 1/ | $V_{CC}$ = 5.5 V | | 1, 2, 3 | 01 | -40 | -100 | mA |
| Power supply current | $I_{CC}$ 2/ | -55°C and +25°C | | 1, 3 | 01 | | 164 | mA |
| | | +125°C | | 2 | 01 | | 150 | mA |
| $A_{15}$ enable current | $I_T$ | $A_{15}$ connected to +12 V through 1 k ohm ±10%. | | 1, 2, 3 | 01 | | 5 | mA |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 3/ 4, 5/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified | | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| $A_i$ to $O_i$ delay | $t_{PD}$ | See figure 4. Parameter reference 1 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 23 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 30 | ns |
| $\overline{RASI}$ to $\overline{RASi}$ ($\overline{RFSH}$ = H) | $t_{PHL}$ | See figure 4. Parameter reference 2 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 23 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 27 | ns |
| $\overline{RASI}$ to $\overline{RASi}$ ($\overline{RFSH}$ = L) | $t_{PHL}$ | See figure 4. Parameter reference 3 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 23 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 27 | ns |
| MSEL to $O_i$ | $t_{PD}$ | See figure 4. Parameter reference 4 | $C_L$ = 50 pF | 9, 10, 11 | 01 | 5 | | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | 7 | | ns |
| MSEL to $O_i$ | $t_{PD}$ | See figure 4. Parameter reference 5 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 25 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 31 | ns |
| $\overline{CASI}$ to $\overline{CASO}$ ($\overline{RFSH}$ = H) | $t_{PHL}$ | See figure 4. Parameter reference 6 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 19 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 26 | ns |
| $\overline{RSELi}$ to $\overline{RASi}$ (LE = H, $\overline{RASI}$ = L) | $t_{PHL}$ | See figure 4. Parameter reference 7 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 24 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 30 | ns |
| $\overline{RFSH}$ to $\overline{TC}$ ($\overline{RASI}$ = L) | $t_{PLH}$ | See figure 4. Parameter reference 8 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 50 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 55 | ns |
| $\overline{RASI}$ to $\overline{TC}$ ($\overline{RFSH}$ = L) | $t_{PLH}$ | See figure 4. Parameter reference 9 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 40 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 55 | ns |
| $\overline{RASI}$ = L ($\overline{RFSH}$ = L) | $t_{PW}$ | See figure 4. Parameter reference 10 | $C_L$ = 50 pF | 9, 10, 11 | 01 | 50 | | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | 50 | | ns |
| $\overline{RASI}$ = H ($\overline{RFSH}$ = L) | $t_{PW}$ | See figure 4. Parameter reference 11 | $C_L$ = 50 pF | 9, 10, 11 | 01 | 50 | | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | 50 | | ns |
| $\overline{RFSH}$ to Oi ($\overline{RASI}$ = X) | $t_{PD}$ | See figure 4. Parameter reference 12 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 25 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 30 | ns |
| $\overline{RFSH}$ to $\overline{RASi}$ ($\overline{RASI}$ = L) | $t_{PHL}$ | See figure 4. Parameter reference 13 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 29 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 36 | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 3/ 4/ 5/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified | | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| $\overline{CLR}$ = L | $t_{PW}$ | See figure 4. Parameter reference 14 | $C_L$ = 50 pF | 9, 10, 11 | 01 | 35 | | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | 35 | | ns |
| $\overline{RFSH}$ to $\overline{CASO}$ ($\overline{RASI}$ = L, $\overline{CASI}$ = L) | $t_{PLH}$ 7/ | See figure 4. Parameter reference 15 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 25 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 31 | ns |
| LE to Oi | $t_{PD}$ | See figure 4. Parameter reference 16 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 40 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 50 | ns |
| LE to $\overline{RASi}$ | $t_{PHL}$ | See figure 4. Parameter reference 17 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 45 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 54 | ns |
| $\overline{CLR}$ to $\overline{TC}$ | $t_{PLH}$ | See figure 4. Parameter reference 18 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 56 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 60 | ns |
| $\overline{CLR}$ to Oi ($\overline{RFSH}$ = L) | $t_{PLH}$ | See figure 4. Parameter reference 19 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 54 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 62 | ns |
| Ai to LE Set-up time | $t_S$ 8/ | See figure 4. Parameter reference 20 | $C_L$ = 50 pF | 9, 10, 11 | 01 | 5 | | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | 5 | | ns |
| Ai to LE Hold time | $t_H$ 8/ | See figure 4. Parameter reference 21 | $C_L$ = 50 pF | 9, 10, 11 | 01 | 15 | | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | 12 | | ns |
| RSELi to LE Set-up time | $t_S$ 8/ | See figure 4. Parameter reference 22 | $C_L$ = 50 pF | 9, 10, 11 | 01 | 5 | | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | 5 | | ns |
| RSELi to LE Hold time | $t_H$ 8/ | See figure 4. Parameter reference 23 | $C_L$ = 50 pF | 9, 10, 11 | 01 | 25 | | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | 25 | | ns |
| $\overline{CLR}$ recover time | $t_S$ | See figure 4. Parameter reference 24 | $C_L$ = 50 pF | 9, 10, 11 | 01 | 18 | | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | 18 | | ns |
| Oi to $\overline{RASi}$ ($\overline{RFSH}$ = H) | $t_{SKEW}$ 9/ | See figure 4. Parameter reference 25 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 6 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 7 | ns |
| Oi to $\overline{CASO}$ | $t_{SKEW}$ 9/ | See figure 4. Parameter reference 26 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 8 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 8 | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 3/ 4/ 5/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified | | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Oi to $\overline{RASi}$ ($\overline{RFSH}$ = L) | $t_{SKEW}$ 10/ | See figure 4. Parameter reference 27 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 10 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 10 | ns |
| Oi to $\overline{RASi}$ ($\overline{MSEL}$ = ↓) | $t_{SKEW}$ 11/ | See figure 4. Parameter reference 28 | $C_L$ = 50 pF | 9, 10, 11 | 01 | | 5 | ns |
| | | | $C_L$ = 150 pF 6/ | 9, 10, 11 | 01 | | 5 | ns |

1/ Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

2/ $I_{CC}$ is worst case when the address inputs are latched high, the refresh counter is at terminal count (255). $\overline{RASI}$ and $\overline{CASI}$ are high and all other inputs are low.

3/ Minimum spec limits for $t_{PW}$, $t_S$ and $t_H$ are minimum system operating requirements. Limits for $t_{SKEW}$ and $t_{PD}$ are guaranteed test limits for the device.

4/ All ac parameters are specified at the 1.5 V level.

5/ AC and function testing are performed at $V_{IL}$ = 0 V and $V_{IH}$ = 3.5 V.

6/ AC testing is performed to a 50 pF typical capacitive load. The ac limits for 150 pF are not tested, but are correlated to the 50 pF measurements.

7/ $\overline{RFSH}$ inhibits $\overline{CASO}$ during refresh. Specification is for $\overline{CASO}$ inhibit time.

8/ Set-up and hold tests are not performed. These parameters are guaranteed by correlation and characterization.

9/ Oi to $\overline{RASi}$ ($\overline{RFSH}$ = high) skew is guaranteed maximum difference between fastest $\overline{RASI}$ to $\overline{RASi}$ delay and slowest Ai to Oi delay within a single device. Oi to $\overline{CASO}$ skew is maximum difference between fastest $\overline{CASI}$ to $\overline{CASO}$ delay and slowest MSEL to Oi delay within a single device.

10/ Oi to $\overline{RASi}$ ($\overline{RFSH}$ = low) skew is guaranteed maximum difference between fastest $\overline{RASI}$ to $\overline{RASi}$ delay and slowest $\overline{RFSH}$ to Oi delay within a single device

11/ Oi to $\overline{RASi}$ (MSEL = ↓) skew is guaranteed maximum difference between fastest MSEL↓ to Oi delay and slowest $\overline{RASI}$ to $\overline{RASi}$ delay within a single device.

| Device type | 01 | | | | |
|---|---|---|---|---|---|
| Case outline | Q | U | Case outline | Q | U |
| Terminal number | Terminal symbol | Terminal symbol | Terminal number | Terminal symbol | Terminal symbol |
| 1 | $\overline{RAS}_2$ | $\overline{RAS}_2$ | 23 | $A_4$ | $A_{12}$ |
| 2 | $\overline{RAS}_3$ | $\overline{RAS}_3$ | 24 | $A_{11}$ | $O_4$ |
| 3 | $\overline{RASI}$ | $\overline{RASI}$ | 25 | $\overline{RFSH}$ | $A_4$ |
| 4 | RSEL0 | RSEL0 | 26 | $O_3$ | $A_{11}$ |
| 5 | RSEL1 | RSEL1 | 27 | $A_3$ | $\overline{RFSH}$ |
| 6 | $\overline{CASO}$ | NC | 28 | $A_{10}$ | NC |
| 7 | $\overline{CASI}$ | $\overline{CASO}$ | 29 | $O_2$ | $O_3$ |
| 8 | $\overline{CLR}$ | $\overline{CASI}$ | 30 | GND | $A_3$ |
| 9 | $\overline{TC}$ | $\overline{CLR}$ | 31 | $A_2$ | $A_{10}$ |
| 10 | $V_{CC}$ | $\overline{TC}$ | 32 | $A_9$ | $O_2$ |
| 11 | $A_{15}$ | $V_{CC}$ | 33 | $O_1$ | GND |
| 12 | $O_7$ | $A_{15}$ | 34 | $A_1$ | $A_2$ |
| 13 | $A_7$ | $O_7$ | 35 | $A_8$ | $A_9$ |
| 14 | $A_{14}$ | $A_7$ | 36 | LE | $O_1$ |
| 15 | $O_6$ | $A_{14}$ | 37 | $O_0$ | $A_1$ |
| 16 | MSEL | $O_6$ | 38 | $A_0$ | $A_8$ |
| 17 | $A_6$ | NC | 39 | $\overline{RAS}_0$ | NC |
| 18 | $A_{13}$ | MSEL | 40 | $\overline{RAS}_1$ | LE |
| 19 | $O_5$ | $A_6$ | 41 | --- | $O_0$ |
| 20 | $A_5$ | $A_{13}$ | 42 | --- | $A_0$ |
| 21 | $A_{12}$ | $O_5$ | 43 | --- | $\overline{RAS}_0$ |
| 22 | $O_4$ | $A_5$ | 44 | --- | $\overline{RAS}_1$ |

NC = No connection

FIGURE 1. Terminal connections.

$\overline{RAS}$ output function table

| $\overline{RFSH}$ | $\overline{RASI}$ | $RSEL_1$ | $RSEL_0$ | $\overline{RAS_0}$ | $\overline{RAS_1}$ | $\overline{RAS_2}$ | $\overline{RAS_3}$ |
|---|---|---|---|---|---|---|---|
| L | H | X | X | H | H | H | H |
| L | L | X | X | L | L | L | L |
| H | H | X | X | H | H | H | H |
| H | L | L | L | L | H | H | H |
| H | L | L | H | H | L | H | H |
| H | L | H | L | H | H | L | H |
| H | L | H | H | H | H | H | L |

$\overline{CASO}$ function table

| $\overline{RFSH}$ | $\overline{CASI}$ | $\overline{CASO}$ |
|---|---|---|
| H | L | L |
| H | H | H |
| L | X | H |

Address output function table

| MSEL | $\overline{RFSH}$ | $O_0 – O_7$ |
|---|---|---|
| H | H | $A_0 – A_7$ |
| L | H | $A_8 – A_{15}$ |
| X | L | Refresh address |

Refresh address counter function table

| $A_{15}$ | $\overline{CLR}$ | $\overline{RFSH}$ | $\overline{RASI}$ | $\overline{TC}$ | Refresh count | Function |
|---|---|---|---|---|---|---|
| X | L | X | X | X | $FF_H$ | Clear counter |
| X | H | ↓ | X | X | NC | Output refresh address no change for counter |
| X | H | ↑ | L | X | Count - 1 | Return to memory cycle mode and decrement counter |
| X | H | L | ↓ | X | NC | Output all $\overline{RAS_i}$ to RAM no change for counter |
| X | H | L | ↑ | X | Count - 1 | Return $\overline{RAS_i}$ to HIGH and decrement counter |
| L or H | H | X | X | L | $00_H$ | Terminal count for 256 line refresh |
| +12 V* | H | X | X | L | $00_H$ and $80_H$ | Terminal count for 128 line refresh |

* - Through 1kΩ resistor.

FIGURE 2. Truth tables.

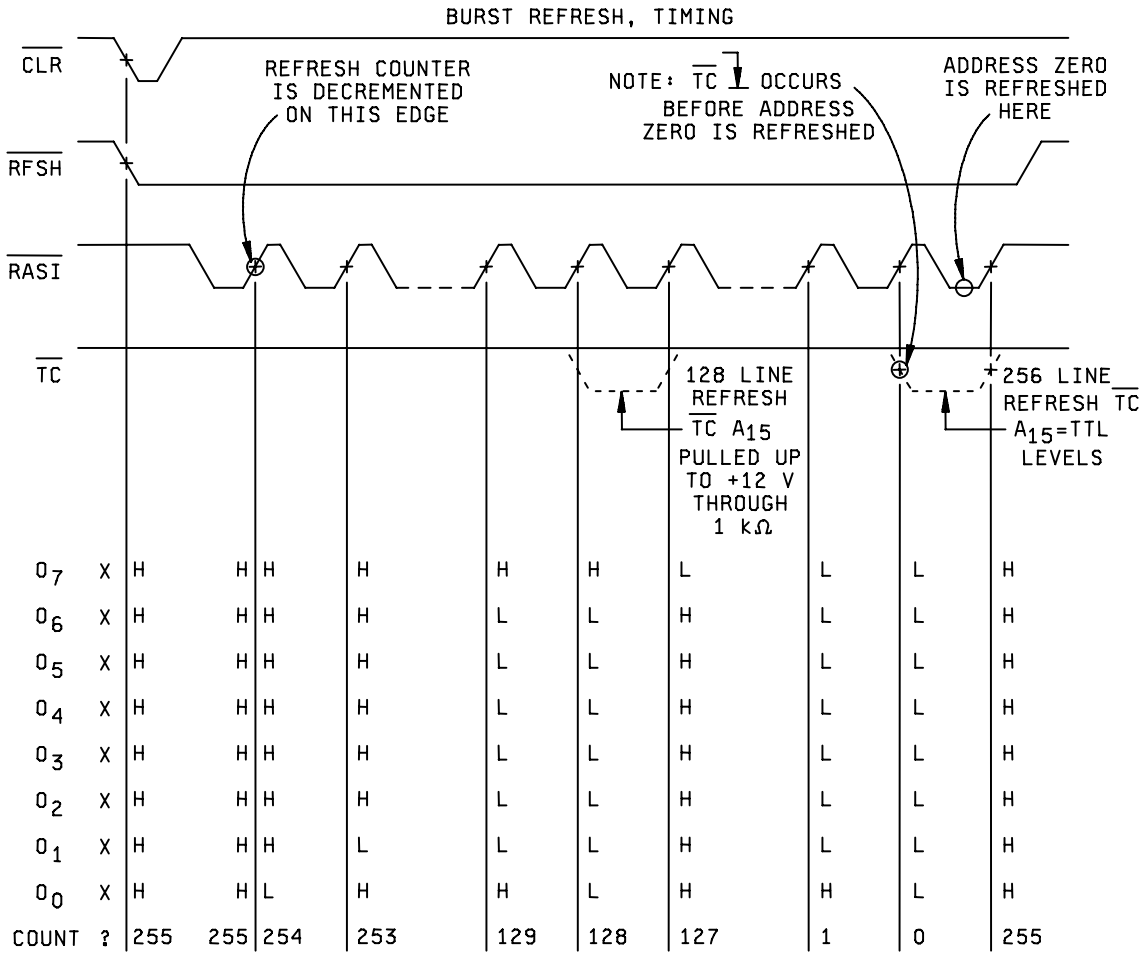


FIGURE 2. Truth tables - Continued.

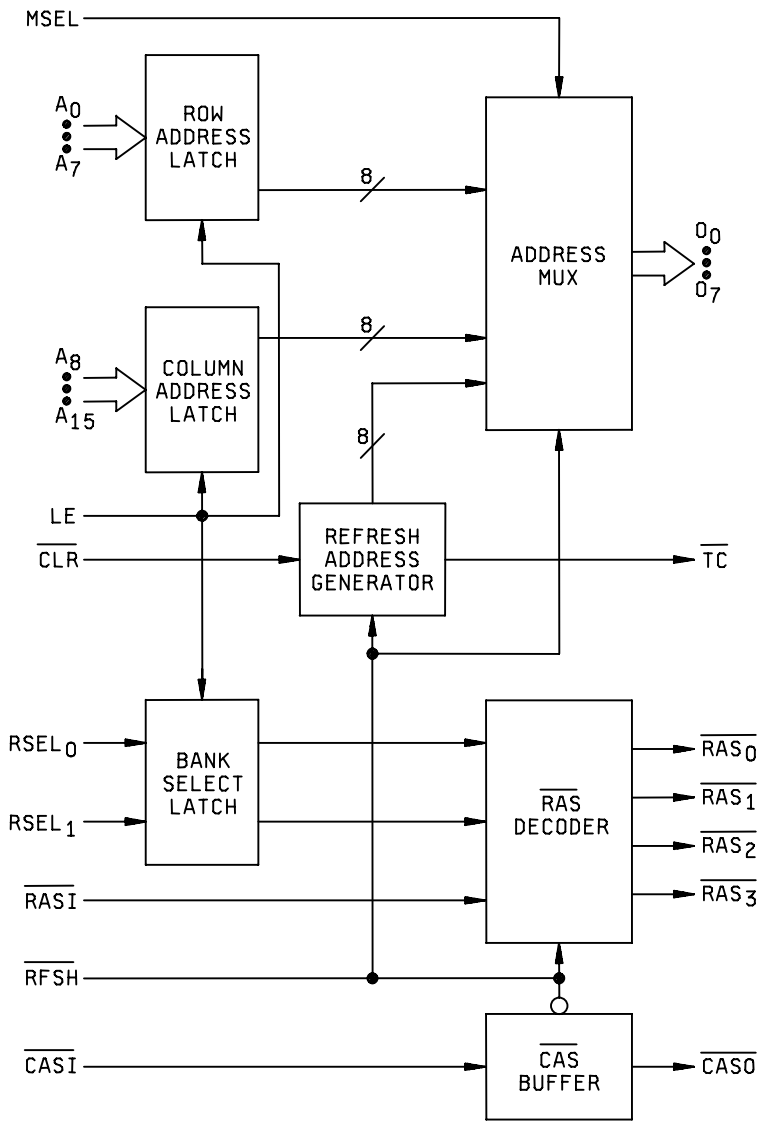


FIGURE 3. Block diagram.

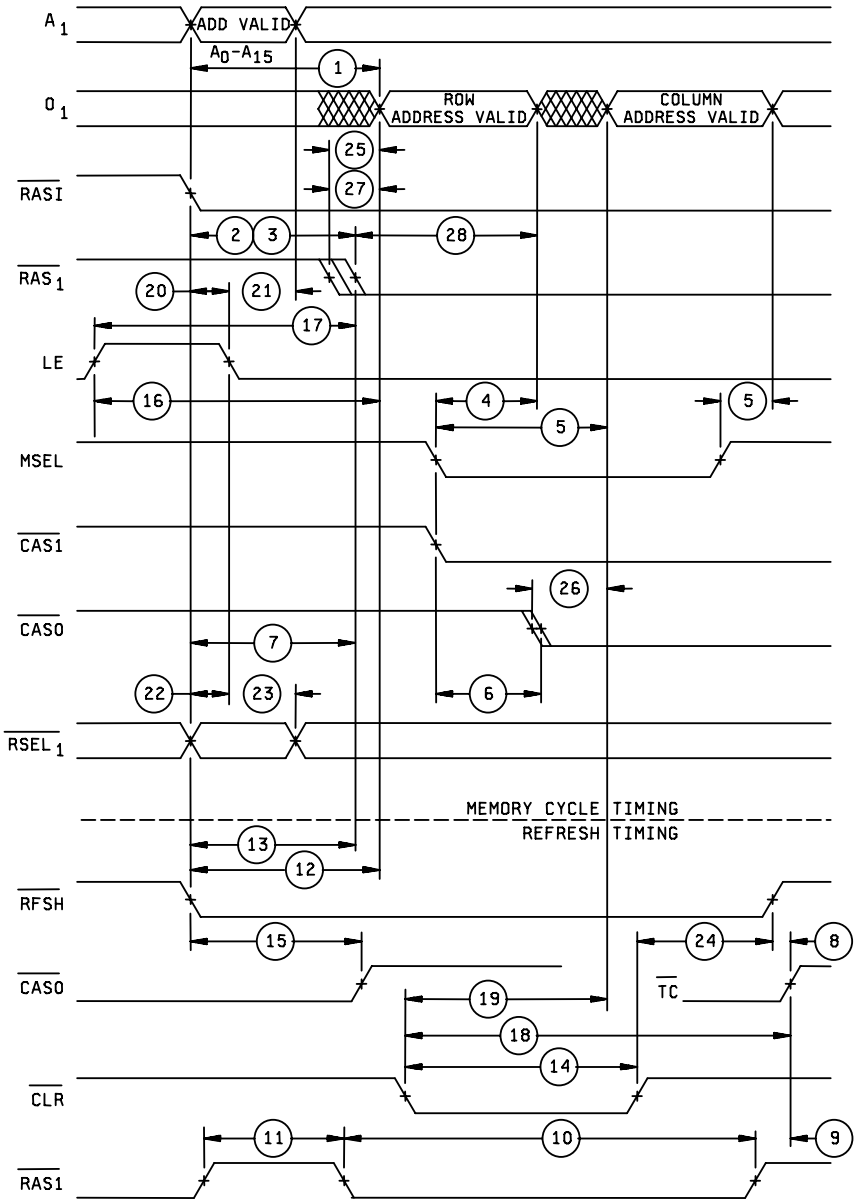


FIGURE 4. Timing waveforms.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) | --- |
| Final electrical test parameters (method 5004) | 1/ 1, 2, 3, 7, 8, 9, 10, 11 |
| Group A test requirements (method 5005) | 1, 2, 3, 7, 8, 9, 10, 11 |
| Groups C and D end-point electrical parameters (method 5005) | 1, 7, 9 |

1/ PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and table III herein.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Pin description.

| Pin number | Name | I/O | Description |
|---|---|---|---|
| | $A_0 – A_7$ | I | The low order address inputs are used to latch eight row address inputs for the RAM. These inputs drive the outputs $O_0 – O_7$ when MSEL is high |
| | $A_8 – A_{15}$ | I | The high order address inputs are used to latch eight column address inputs for the RAM. These inputs drive the outputs $O_0 – O_7$ when MSEL is low. |
| 11 | $A_{15}$ | I | $A_{15}$ is a dual input. With normal TTL level inputs, $A_{15}$ acts as an address input for 64k RAMs. If $A_{15}$ is pulled up to +12 V through a 1 kilohm resistor, the terminal count output, $\overline{TC}$, will go low every 128 counts (for 16k RAMs) instead of every 256 counts. |
| | $O_0 – O_7$ | O | The RAM address output. The eight-bit width is designed for dynamic RAMs up to 64k. |
| 16 | MSEL | I | The multiplexer-select input determines whether the low order or high order address input appears at the multiplexer outputs $O_0 – O_7$. When MSEL is high, the low order address latches ($A_0 – A_7$) are connected to the outputs. When MSEL is low, the high order address latches are connected to the outputs. |
| 25 | $\overline{RFSH}$ | I | The refresh control input. When active low, the $\overline{RFSH}$ input switches the address output multiplexer to output the inverted contents of the eight-bit refresher counter. $\overline{RFSH}$ low also inhibits the $\overline{CAS}$ buffer and changes the mode of the RAS decoder from one-of-four to four-of-four so that all four $\overline{RAS}$ decoder outputs, $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$, and $\overline{RAS_3}$ go low in response to a low input at $\overline{RASI}$. This action refreshes one row address in each of the four $\overline{RAS}$ decoded memory banks. The refresh counter is advanced at the end of each refresh cycle by the low-to-high transition of $\overline{RFSH}$ or $\overline{RASI}$ (whichever occurs first). In burst mode refresh, $\overline{RFSH}$ may be held low and refresh accomplished by toggling RASI. |
| 9 | $\overline{TC}$ | O | The terminal count output. A low output at $\overline{TC}$ indicates that the refresh counter has been sequenced through either 128 or 256 refresh addresses depending on the $A_{15}$. The $\overline{TC}$ output remains active low until the refresh counter is advanced by the rising edge of RASI or $\overline{RFSH}$. |
| 8 | $\overline{CLR}$ | I | The refresh counter clear input. An active low input at $\overline{CLR}$ resets the refresh counter to all low (refresh address output to all high). |
| 36 | LE | I | The address latch enable input. An active high input at LE causes the two 8-bit address latches and the 2-bit $\overline{RAS}$ select input latch to go transparent, accepting new input data. A low input on LE latches the input data which meet set-up and hold time requirements. |
| 4, 5 | $RSEL_0$ and $RSEL_1$ | I | The $\overline{RAS}$ decoder select inputs. Data (latched) at these inputs (normally higher order addresses) is decoded by the $\overline{RAS}$ decoder to "$\overline{RAS}$ select" one of four banks of memory with $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$, or $\overline{RAS_3}$. |
| 3 | $\overline{RASI}$ | I | The row address strobe input. During normal memory cycles the selected $\overline{RAS}$ decoder output $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$, or $\overline{RAS_3}$ will go active low in response to an active low input at $\overline{RASI}$. During refresh ($\overline{RFSH}$ = low), all $\overline{RAS}$ outputs go low in response to RASI = low. |

TABLE III. Pin description - Continued.

| Pin number | Name | I/O | Description |
|---|---|---|---|
| 39, 40, 1, 2 | $RAS_0$, $RAS_1$, $RAS_2$, $RAS_3$ | O | Row address strobe outputs ($\overline{RAS}i$). Each provides a row address strobe output for one of the four banks of memory. Each will go active low only when selected by $RSEL_0$ and $RSEL_1$ and only when $\overline{RASI}$ goes active low. All $RAS_{0-3}$ outputs go active low in response to RASI when $\overline{RFSH}$ goes low. |
| 7 | $\overline{CASI}$ | I | The column address strobe. An active low input at $\overline{CASI}$ will result in an active low output at $\overline{CASO}$, unless a refresh cycle is in progress ($\overline{RFSH}$ = low). |
| 6 | $\overline{CASO}$ | O | The column address strobe output. The active low $\overline{CASO}$ output strobes the column address into the dynamic RAM, CASO is inhibited during refresh (RFSH = low). |

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-12-05

Approved sources of supply for SMD 5962-87574 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/ .

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-8757401QA | 3V146 | 2964B/BQA |
| 5962-8757401UA | 3V146 | 2964B/BUA |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 3V146 | Rochester Electronics, Inc.<br>16 Malcolm Hoyt Drive<br>Newburyport, MA 01950 |