REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Delete one vendor, CAGE 34335. Made changes to table I, table II, figure 1, and throughout drawing. Added figure 8. Device 02QX is inactive for new design.	88-10-12	M. A. Frye
B	Updated boilerplate. Added provisions for the supply of QD certified parts to the drawing. Added CAGE 3V146 to drawing. - glg	00-09-19	Raymond Monnin
C	Boilerplate update, part of 5 year review. ksr	06-10-11	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET	C	C																		
REV	15	16																		
SHEET																				

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Rick Officer

CHECKED BY
D. A. DiCenzo

APPROVED BY
N. A. Hauck

DRAWING APPROVAL DATE
07-August 1987

REVISION LEVEL
C

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUITS, MEMORY, DIGITAL, NMOS, 256 x 8 BIT RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87593**

SHEET 1 OF 16

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-87593	01	Q	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	8155	2K RAM W/ I/O ports and timer, I_{IL} ($\overline{CE}$)
02	8156	2K RAM W/ I/O ports and timer, I_{IL} (CE)

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	CDIP2-T40 or GDIP1-T40	40	dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage to ground potential ..... -0.5 V dc to +7.0 V dc
DC input voltage with respect to GND ..... -0.5 V dc to +7.0 V dc
Maximum power dissipation (P_D): ..... 1.5 W
Lead temperature (soldering, 10 seconds) ..... +270°C
Thermal resistance, junction-to-case (Θ_{JC}) ..... See MIL-STD-1835
Storage temperature range ..... -65°C to +150°C
Junction temperature (T_J) ..... +150°C

1.4 Recommended operating conditions.

Case operating temperature range (T_C) ..... -55°C to +125°C
Input low voltage (V_{IL}) ..... 0.8 V dc
Input high voltage (V_{IH}) ..... 2.0 V dc
Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturer's approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or alternative approved by the Qualifying Activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Case outlines. The case outlines shall be in accordance 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 or QML-38535 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall test sufficient to verify the functional operation of the device.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^{\circ}C \le T_C \le +125^{\circ}C$	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}	V_{CC} = 4.5 V	1, 2, 3	All	1/ -0.5	0.8	V
Input high voltage	V_{IH}	V_{CC} = 4.5 V	1, 2, 3	All	2.0	1/ V_{CC} +0.5	V
Output low voltage	V_{OL}	V_{IL} = 0.8 V, I_{OL} = 2.0 mA V_{CC} = 5.5 V, V_{IH} = 2.0 V	1, 2, 3	All		0.45	V
Output high voltage	V_{OH}	V_{IL} = 0.8 V, V_{IH} = 2.0 V V_{CC} = 5.5 V, I_{OH} = -400 µA	1, 2, 3	All	2.4		V
Input leakage current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 5.5 V to 0 V	1, 2, 3	All		10 -10	µA µA
Output leakage current	I_{OL}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V to 0.45 V	1, 2, 3	All		10 -10	µA µA
V_{CC} supply current	I_{CC}	V_{CC} = 5.5 V 2/	1, 2, 3	All		125	mA
Chip enable leakage (CE)	I_{IL}	V_{CC} = 5.5 V V_{IN} = 5.5 V to 0 V	1, 2, 3	01		160	µA
Chip enable leakage (CE)	I_{IL}	V_{CC} = 5.5 V V_{IN} = 5.5 V to 0 V	1, 2, 3	02		100	µA
Functional testing		See 4.3.1c	7, 8				

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Address to LATCH setup time	t_{AL}	V_{CC} = 5.5 V, 4.5 V	9, 10, 11	All	50		ns
Address hold time after LATCH	t_{LA}	V_{IH} = 2.4 V V_{IL} = 0.45 V	9, 10, 11	All	80		ns
LATCH to READ/WRITE control	t_{LC}	V_{OH} = 2.0 V	9, 10, 11	All	100		ns
Valid data out from READ control	t_{RD}	V_{OL} = 0.8 V	9, 10, 11	All		170	ns
Address stable to data out valid	t_{AD}		9, 10, 11	All		400	ns
LATCH enable width	t_{LL}		9, 10, 11	All	100		ns
Data bus float after READ 3/	t_{RDF}		9, 10, 11	All	0	100	ns
READ/WRITE control to LATCH enable	t_{CL}		9, 10, 11	All	20		ns
READ/WRITE control width	t_{CC}		9, 10, 11	All	250		ns
Data into WRITE setup time	t_{DW}	4/	9, 10, 11	All	150		ns
Data in hold time after WRITE	t_{WD}		9, 10, 11	All	25		ns
Recovery time between controls	t_{RV}		9, 10, 11	All	300		ns
WRITE to port output	t_{WP}		9, 10, 11	All		400	ns
Port input setup time	t_{PR}		9, 10, 11	All	70		ns
Port input hold time	t_{RP}		9, 10, 11	All	50		ns
STB to buffer full	t_{SBF}		9, 10, 11	All		400	ns
STB width	t_{SS}		9, 10, 11	All	200		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Device types	Limits		Unit
					Min	Max	
READ to buffer empty	t_{RBE}	V_{CC} = 5.5 V, 4.5 V	9, 10, 11	All		400	ns
STB to INTR on	t_{SI}	V_{IH} = 2.4 V V_{IL} = 0.45 V	9, 10, 11	All		400	ns
READ to INTR off	t_{RDI}	V_{OH} = 2.0 V	9, 10, 11	All		400	ns
Port setup time to STB	t_{PSS}	V_{OL} = 0.8 V V_{IL} = 0.45 V	9, 10, 11	All	50		ns
Port hold time after STB	t_{PHS}	4/	9, 10, 11	All	120		ns
STB to buffer empty	t_{SBE}		9, 10, 11	All		400	ns
WRITE to buffer full	t_{WBF}		9, 10, 11	All		400	ns
WRITE to INTR off	t_{WI}		9, 10, 11	All		400	ns
TIMER-IN to $\overline{\text{TIMER-OUT}}$ low	t_{TL}		9, 10, 11	All		400	ns
TIMER-IN to $\overline{\text{TIMER-OUT}}$ high	t_{TH}		9, 10, 11	All		400	ns
Data bus enable from READ control	t_{RDE}		9, 10, 11	All	10		ns
TIMER-IN low time	t_1		9, 10, 11	All	88		ns
TIMER-IN high time	t_2		9, 10, 11	All	120		ns

1/ These V_{IL} and V_{IH} values are guaranteed by design and are not tested.

2/ The supply current is measured with unloaded outputs while running functional patterns.

3/ AC float timing parameter t_{rdf} is tested logic 0 to float only.

4/ See figures 2, 3, 4, 5, and 6.

Device types	All
Case outlines	Q
Terminal number	Terminal symbol
1	PC3
2	PC4
3	TIMER IN
4	RESET
5	PC5
6	$\overline{\text{TIMEROUT}}$
7	$\overline{\text{IO/M}}$
8	CE or $\overline{\text{CE}}$
9	$\overline{\text{RD}}$
10	$\overline{\text{WR}}$
11	ALE
12	AD0
13	AD1
14	AD2
15	AD3
16	AD4
17	AD5
18	AD6
19	AD7
20	Vss
21	PA0
22	PA1
23	PA2
24	PA3
25	PA4
26	PA5
27	PA6
28	PA7
29	PB0
30	PB1
31	PB2
32	PB3
33	PB4
34	PB5
35	PB6
36	PB7
37	PC0
38	PC1
39	PC2
40	V_{CC}

FIGURE 1. Terminal connections.

Pin description.

Pin no.	Name	I/O	Pin description
4	RESET	I	The RESET signal is a pulse provided by the 8085AH to initialize the system. Input high on this line resets the chip and initializes the three I/O ports to input code. The width of RESET pulse should typically be 600 ns. (Two 8085AH clock cycle times.)
12-19	AD_0-AD_7	I/O	These are 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data bus. The 8-bit address is latched into the address latch on the falling edge of the ALE. The address can be either for the memory section or the I/O section depending on the polarity of the IO/M input signal. The 8-bit data is either written into the chip or read from the chip depending on the status of $\overline{\text{WRITE}}$ or $\overline{\text{READ}}$ input signal.
8	CE - $\overline{\text{CE}}$	I	Chip enable. On the 01 device, this pin is $\overline{\text{CE}}$ and is active low. On the 02 device, this pin is CE and is active high.
9	$\overline{\text{RD}}$	I	Input low on this line with the chip enable active enables the AD_{0-7} buffers. If IO/M pin is LOW, the RAM content will be read out to the AD bus. Otherwise, the content of the selected I/O port will be read to the AD bus.
10	$\overline{\text{WR}}$	I	Input low on this line with the chip enable active causes the data on the AD lines to be written to the RAM or I/O ports, depending on the of IO/M.
11	ALE	I	Address latch enable. This control signal latches the address on the AD_{0-7} lines and the state of the chip enable and IO/$\overline{\text{M}}$ into the chip at the falling edge of ALE.
7	IO/$\overline{\text{M}}$	I	IO/$\overline{\text{MEMORY}}$ select. This line selects the memory if LOW and selects the IO if HIGH.

FIGURE 1. Terminal connections - continued.

Pin description.

Pin no.	Name	I/O	Pin description
21-28	PA_0-PA_7	I/O	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/Status register.
29-36	PB_0-PB_7	I/O	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/Status register.
37-39 1, 2, 5	PC_0-PC_5	I/O	These 6 pins can function as either input port, output port or as control signals for PA and PB. Programming is done through the C/E register. When PC_{0-5} are used as control signals, they will produce the following: PC_0-A INTR (Port A interrupt) PC_1-A BF (Port A buffer full) PC_2-$\overline{\text{A STB}}$ (Port A strobe) PC_3-B INTR (Port B interrupt) PC_4-B BF (Port B buffer full) PC_5-$\overline{\text{B STB}}$ (Port B strobe)
3	Timer In	I	This is the input to the counter timer.
6	$\overline{\text{Timer Out}}$	O	This pin is the timer output. This output can be either a square wave or a pulse depending on the timer code.
40	V_{CC}		+5 volt supply.
20	V_{SS}		Ground reference.

FIGURE 1. Terminal connections - continued.

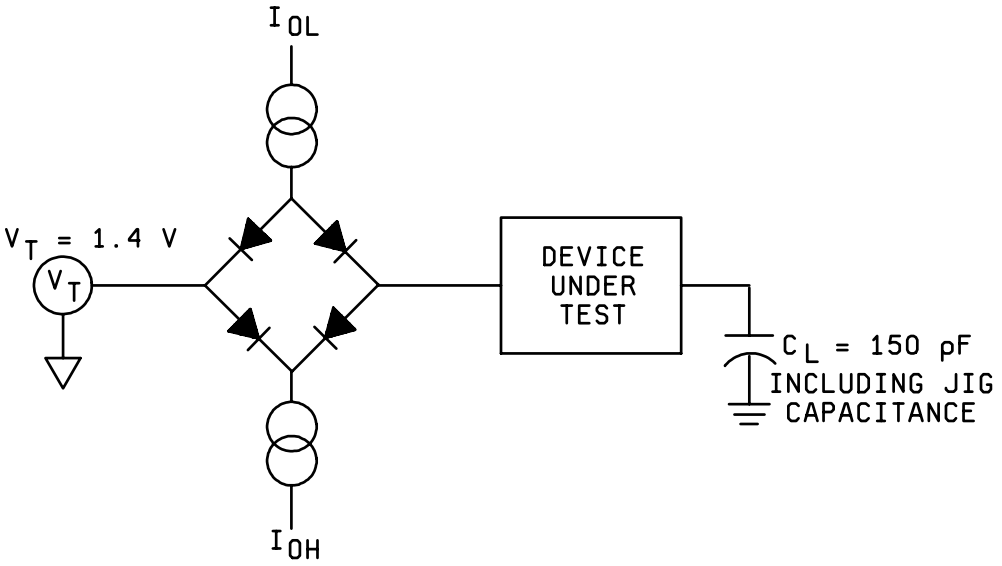


FIGURE 2. AC testing load circuit.

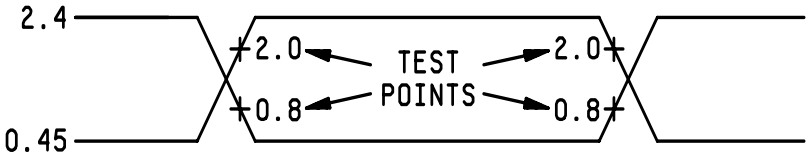
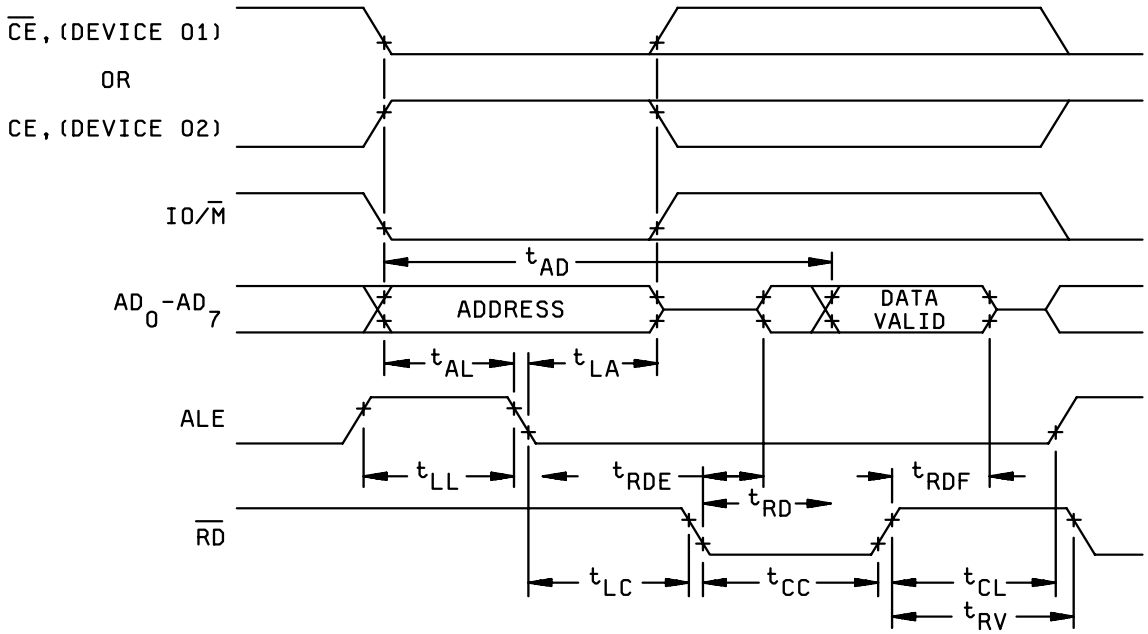


FIGURE 3. AC switching circuit and input/output waveform.

Read cycle



Write cycle

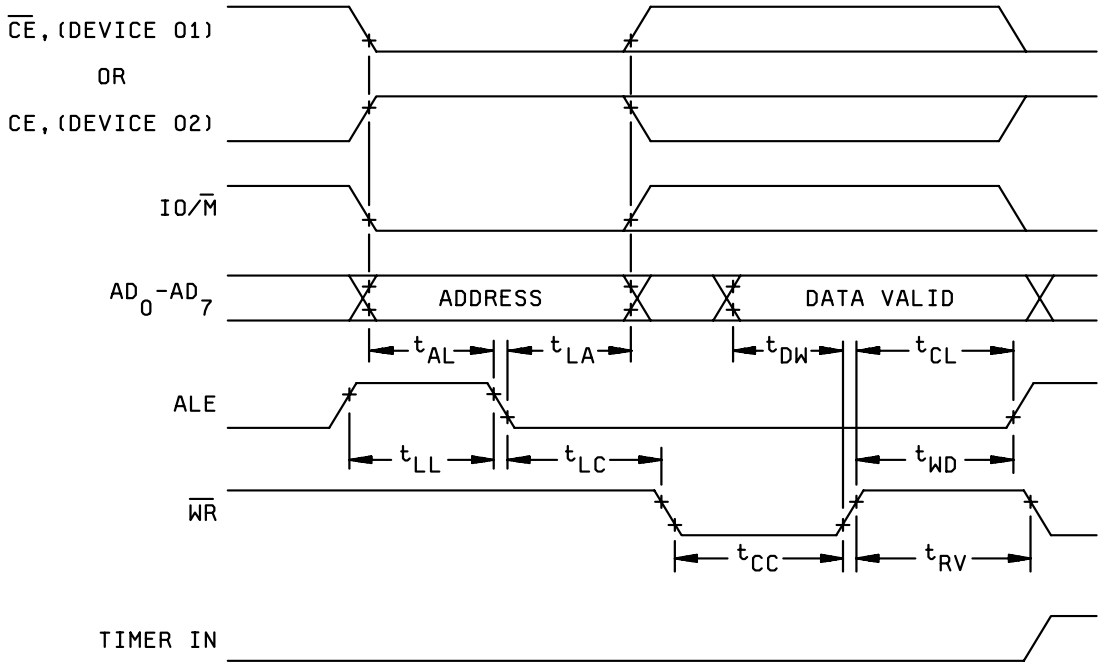
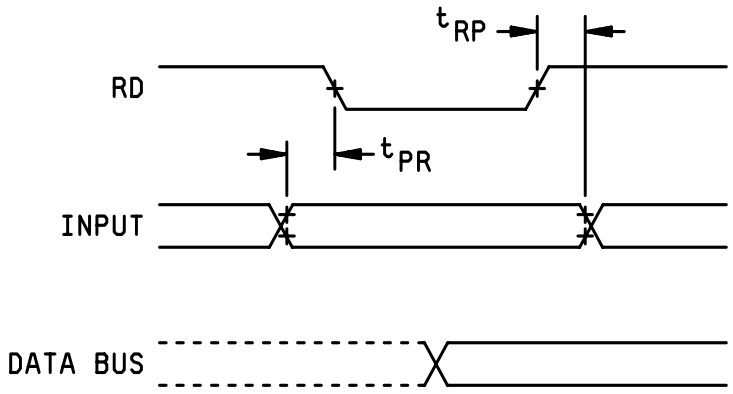
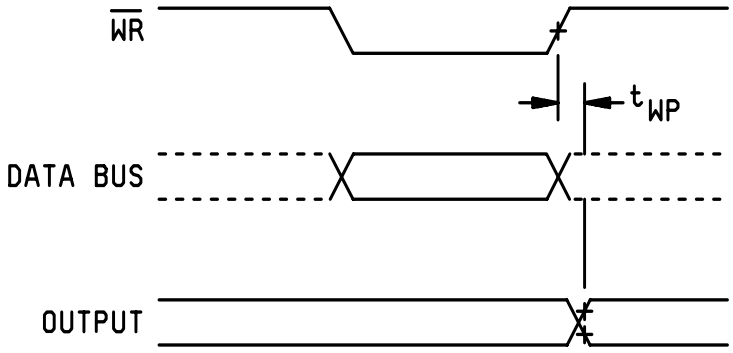


FIGURE 4. Timing waveforms.

Basic input mode

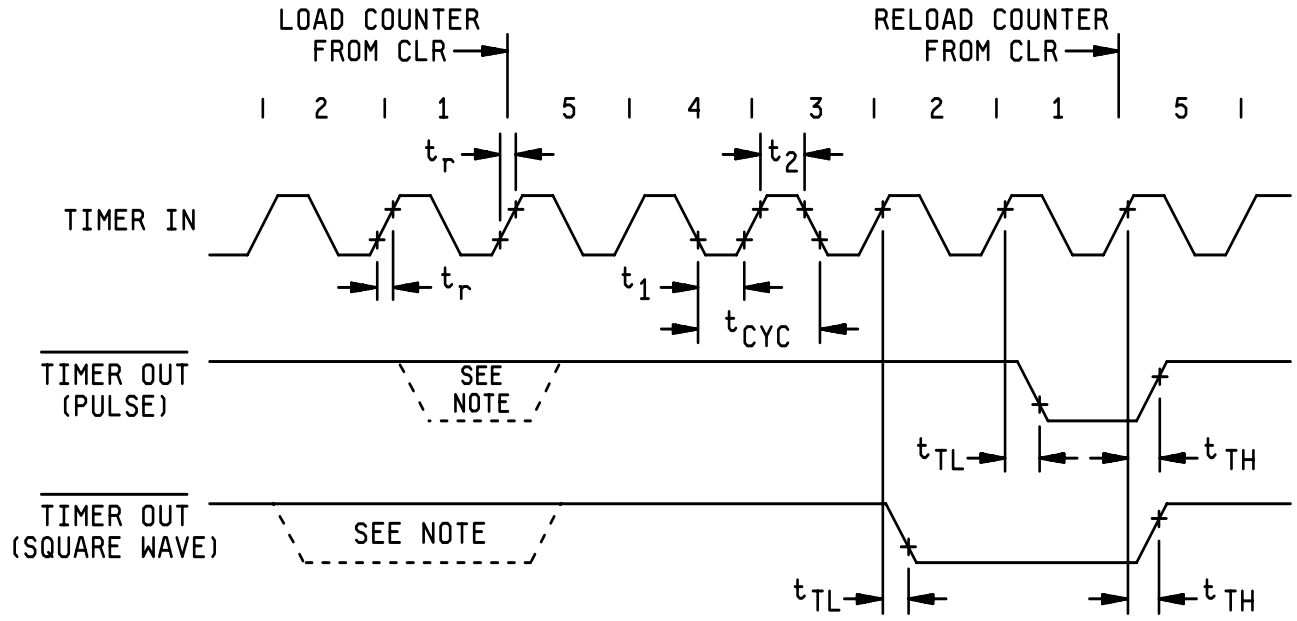


Basic output mode



NOTE: See read cycle and write cycle for data bus timing.

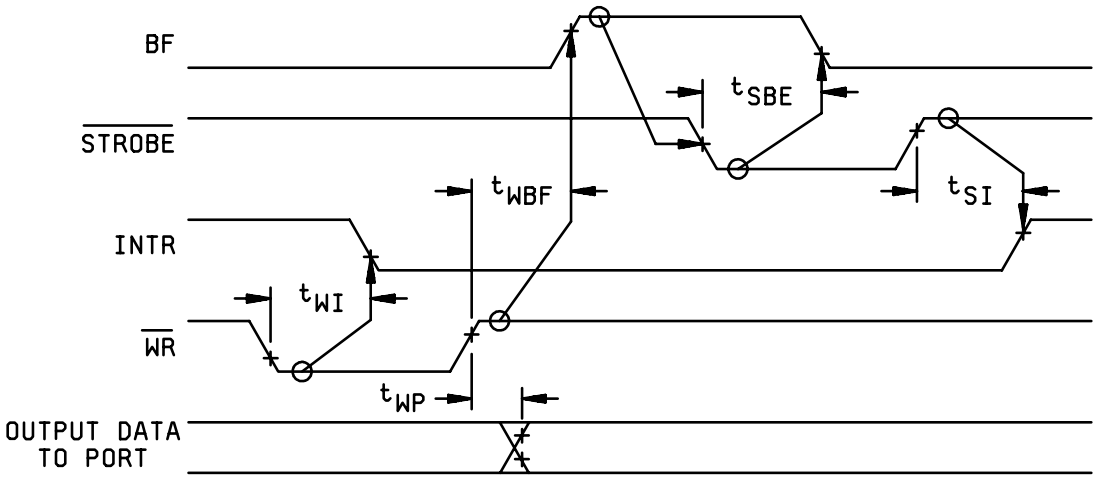
FIGURE 4. Timing waveforms.- continued.



NOTE: The timer output is periodic if in automatic reload mode (M_1 mode bit = 1).

FIGURE 5. Timer output waveform countdown from 5 to 1.

Strobed output



Strobed input

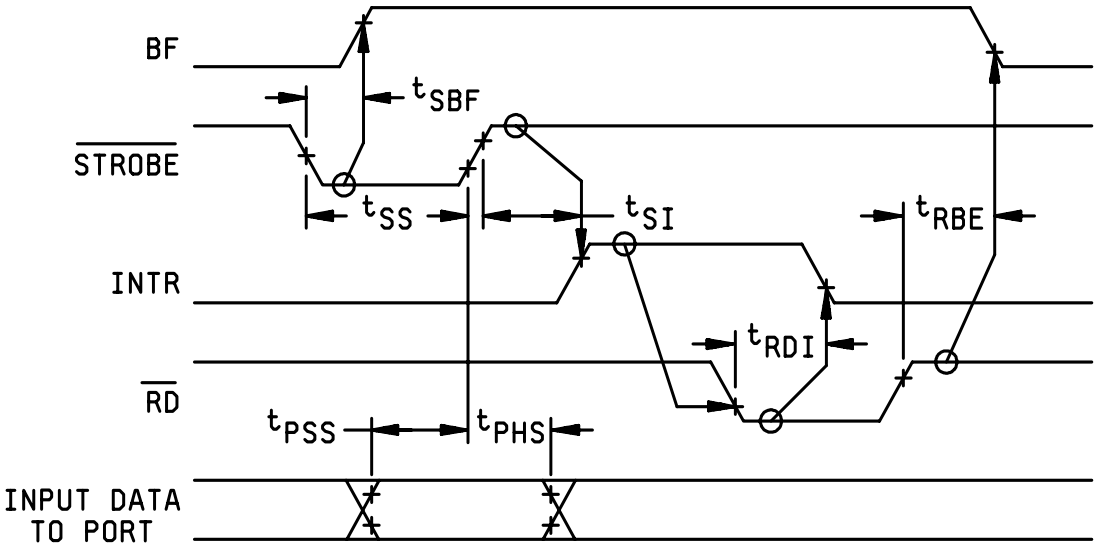


FIGURE 6. Strobed input/output timing waveforms.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8A,8B, 9,10**,11**
Group A test requirements (method 5005)	1*, 2, 3, 7, 8A, 8B, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	2, 8A, 10 or 1, 2, 3

* PDA applies to subgroups 1 and 7
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614)-692-0547.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-10-11

Approved sources of supply for SMD 5962-87593 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Microcircuit drawing part number 1/	Vendor CAGE number	Vendor similar part number 2/
5962-8759301QA	3V146	MD8155H/BQA
5962-8759302QA	3/	AM8156/BQA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics Inc. 10 Malcolm Hoyt Drive Newburyport, MA 01950

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.