REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change V_{OH} and V_{OL} test conditions. Change I_{IL} test limit. Change figure 1. Change t_{SKEW} test condition. Change CAGE code to 67268. Delete footnotes 4/ and 5/ from table I and apply the information to the applicable test conditions. Delete the block diagram from figure 2 and 3.2.2. Editorial changes throughout.	89-09-12	M. Frye
B	Changes in accordance with NOR 5962-R214-92.	92-05-15	M. Frye
C	Update drawing to current requirements. Editorial changes throughout. – drw	05-03-10	Raymond Monnin

CURRENT CAGE CODE 67268
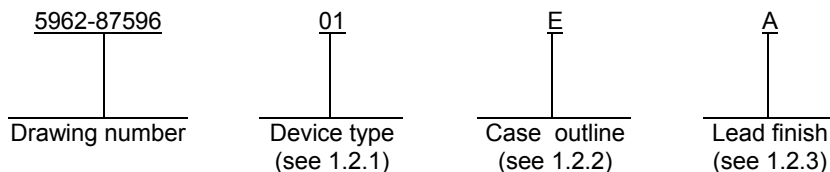
THE FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED

REV																
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REV STATUS		REV	C	C	C	C	C	C	C	C	C	C	C			
OF SHEETS		SHEET	1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A	PREPARED BY Joseph A. Kerby	DEFENSE SUPPLY CENTER COLUMBUS **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**		
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Charles E. Besore			
	APPROVED BY M. Frye	MICROCIRCUIT, LINEAR, QUAD DIFFERENTIAL LINE RECEIVER, MONOLITHIC SILICON		
	DRAWING APPROVAL DATE 87-06-01			
	REVISION LEVEL C	SIZE A	CAGE CODE **14933**	**5962-87596**
		SHEET 1 OF 11		

1. SCOPE

1.1 <u>Scope</u>. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 <u>Part or Identifying Number (PIN)</u>. The complete PIN is as shown in the following example:

<table>
<tr><td>5962-87596</td><td>01</td><td>E</td><td>A</td></tr>
<tr><td>|</td><td>|</td><td>|</td><td>|</td></tr>
<tr><td>Drawing number</td><td>Device type
(see 1.2.1)</td><td>Case outline
(see 1.2.2)</td><td>Lead finish
(see 1.2.3)</td></tr>
</table>

1.2.1 <u>Device type</u>. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	26LS34	Quad differential line receiver

1.2.2 <u>Case outlines</u>. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	flat pack
2	CQCC1-N20	20	square leadless chip carrier

1.2.3 <u>Lead finish</u>. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 <u>Absolute maximum ratings</u>.

Supply voltage range..	-0.5 V to +7.0 V
Enable voltage range	-1.5 V to +7.0 V
Common mode voltage (V_{CM})...	±25 V
Differential input voltage (V_{ID})...	30 V
Output sink current (I_O)..	50 mA
Storage temperature range	-65°C to +165°C
Maximum power dissipation (P_D) <u>1/</u>...	400 mW
Lead temperature (soldering, 10 seconds)...	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case E..	80°C/W
Case F..	65°C/W
Case 2	70°C/W
Junction temperature (T_J)	+150°C

1.4 <u>Recommended operating conditions</u>.

Supply voltage (V_{CC})	4.5 V to 5.5 V
ENABLE high level input voltage (V_{IH})...	2.0 V
ENABLE low level input voltage (V_{IL})	0.8 V
Ambient temperature range (T_A)	-55°C to +125°C

<u>1/</u>   Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS`

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Switching test circuit. The switching test circuit shall be as specified on figure 2.

3.2.4 Switching waveforms. The switching waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Differential input voltage	V_{TH}	$V_{OUT} = V_{OL}$ or V_{OH} 1/	0 V ≤ V_{CM} ≤ +5 V	1, 2, 3	01		±100	mV
			-7 V ≤ V_{CM} ≤ +12 V				±200	
			-15 V ≤ V_{CM} ≤ +15 V				±400	
Input resistance	R_{IN}	-15 V ≤ V_{CM} ≤ +15 V 2/ (one input ac GND)		1, 2, 3	01	12	40	kΩ
Input current	I_{IN}	$V_{IN} = +12$ V		1, 2, 3	01		+1.0	mA
		$V_{IN} = -7$ V					-0.8	
High level output voltage	V_{OH}	$V_{CC} = 4.5$ V, $\Delta V_{IN} = +1.0$ V V$\overline{ENABLE}$ = 0.8 V	$I_{OH} = -12$ mA	1, 2, 3	01	+2.0		V
			$I_{OH} = -1$ mA			+2.4		
Low level output voltage	V_{OL}	$V_{CC} = 4.5$ V, $\Delta V_{IN} = -1.0$ V V$\overline{ENABLE}$ = 0.8 V	$I_{OL} = 16$ mA	1, 2, 3	01		+0.4	V
			$I_{OL} = 24$ mA				+0.5	
Enable clamp voltage	V_{IC}	$I_{IN} = -18$ mA, $V_{CC} = 4.5$ V		1, 2, 3	01		-1.5	V
Off-state (high impedance) output current	I_O	$V_{CC} = 5.5$ V	$V_{OUT} = 2.4$ V	1, 2, 3	01		+50	µA
			$V_{OUT} = 0.4$ V				-50	
ENABLE level input current	I_{IH1}	$V_{CC} = 5.5$ V, $V_{IN} = 2.7$ V		1, 2, 3	01		+20	µA
ENABLE level input current	I_{IL}	$V_{CC} = 5.5$ V, $V_{IN} = 0.4$ V		1, 2, 3	01		-0.20	mA
ENABLE level input current	I_{IH2}	$V_{CC} = 5.5$ V, $V_{IN} = 5.5$ V		1, 2, 3	01		+100	µA
Output short circuit current 3/	I_{OS}	$V_{CC} = 5.5$ V, $V_{OUT} = 0$ V, $\Delta V_{IN} = +1.0$ V		1, 2, 3	01	-30	-120	mA
Supply current	I_{CC}	All V_{IN} = GND, $V_{CC} = 5.5$ V, outputs disabled		1, 2, 3	01		+70	mA
Input hysteresis	V_{HYST}	$V_{CC} = 5.0$ V		1, 2, 3	01	+90	+300	mV
Open circuit input voltage	V_{IOC}			1, 2, 3	01	+2.0	+3.0	V
Functional testing		See 4.3.1c		7, 8	01			

See footnotes at end of table.

Test	Symbol	Conditions -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Propagation delay from input to output	t_{PLH}	C_L = 50 pF, R_{L1} = 1 kΩ, R_{L2} = 280Ω, see figures 2 and 3	T_A = +25°C, V_{CC} = 5.0 V	9	01		24	ns
			V_{CC} = 4.5 V to 5.0 V	9, 10, 11			30	
Propagation delay from input to output	t_{PHL}		T_A = +25°C, V_{CC} = 5.0 V	9			24	
			V_{CC} = 4.5 V to 5.0 V	9, 10, 11			30	
Propagation delay from ENABLE to output	t_{PZH}		T_A = +25°C, V_{CC} = 5.0 V	9			16	
			V_{CC} = 4.5 V to 5.0 V	9, 10, 11			22	
Propagation delay from ENABLE to output	t_{PZL}		T_A = +25°C, V_{CC} = 5.0 V	9			22	
			V_{CC} = 4.5 V to 5.0 V	9, 10, 11			33	
Propagation delay from ENABLE to output	t_{PHZ}	C_L = 5 pF, R_{L1} = 1 kΩ, R_{L2} = 280Ω, see figures 2 and 3	T_A = +25°C, V_{CC} = 5.0 V	9	01		18	ns
			V_{CC} = 4.5 V to 5.0 V	9, 10, 11			27	
Propagation delay from ENABLE to output	t_{PLZ}		T_A = +25°C, V_{CC} = 5.0 V	9			18	
			V_{CC} = 4.5 V to 5.0 V	9, 10, 11			27	
Propagation delay SKEW	t_{SKEW}	| t_{PLH} − t_{PHL} |	T_A = +25°C, V_{CC} = 5.0 V	9	01		±4	ns
			V_{CC} = 4.5 V to 5.0 V	9, 10, 11			±5	
Propagation delay from $\overline{ENABLE}$ to output	t_{PZH}	C_L = 50 pF, R_{L1} = 1 kΩ, R_{L2} = 280Ω, see figures 2 and 3	T_A = +25°C, V_{CC} = 5.0 V	9	01		26	ns
			V_{CC} = 4.5 V to 5.0 V	9, 10, 11			39	
Propagation delay from $\overline{ENABLE}$ to output	t_{PZL}		T_A = +25°C, V_{CC} = 5.0 V	9			33	
			V_{CC} = 4.5 V to 5.0 V	9, 10, 11			49	
Propagation delay from $\overline{ENABLE}$ to output	t_{PHZ}	C_L = 5 pF, R_{L1} = 1 kΩ, R_{L2} = 280Ω, see figures 2 and 3	T_A = +25°C, V_{CC} = 5.0 V	9	01		20	ns
			V_{CC} = 4.5 V to 5.0 V	9, 10, 11			30	
Propagation delay from $\overline{ENABLE}$ to output	t_{PLZ}		T_A = +25°C, V_{CC} = 5.0 V	9			20	
			V_{CC} = 4.5 V to 5.0 V	9, 10, 11			30	

1/ Input voltage is not tested directly due to tester accuracy limitations but is tester correlated.
2/ R_{IN} is not directly tested but is correlated.
3/ Not more than one output should be shorted at a time. Duration of short circuit test should not exceed one second.

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Device type	01	
Case outlines	E and F	2
Terminal number	Terminal symbol	
1	INPUT A-	NC
2	INPUT A+	INPUT A-
3	OUTPUT A	INPUT A+
4	ENABLE	OUTPUT A
5	OUTPUT C	ENABLE
6	INPUT C+	NC
7	INPUT C-	OUTPUT C
8	GND	INPUT C+
9	INPUT D-	INPUT C-
10	INPUT D+	GND
11	OUTPUT D	NC
12	$\overline{\text{ENABLE}}$	INPUT D-
13	OUTPUT B	INPUT D+
14	INPUT B+	OUTPUT D
15	INPUT B-	$\overline{\text{ENABLE}}$
16	V_{CC}	NC
17	- - -	OUTPUT B
18	- - -	INPUT B+
19	- - -	INPUT B-
20	- - -	V_{CC}

FIGURE 1. Terminal connections.

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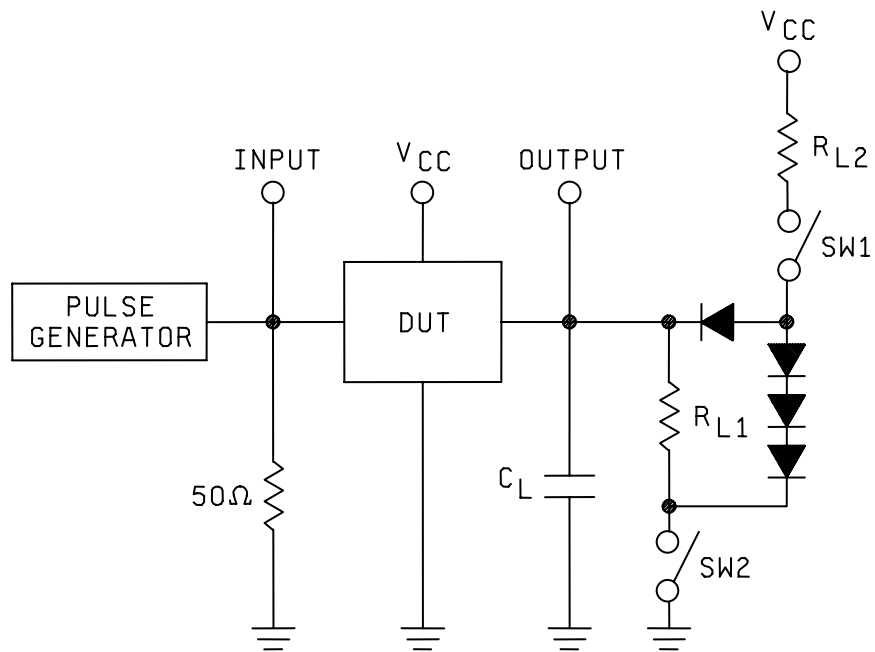| Switch matrix		
Parameter	SW1	SW2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

FIGURE 2. Switching test circuit.

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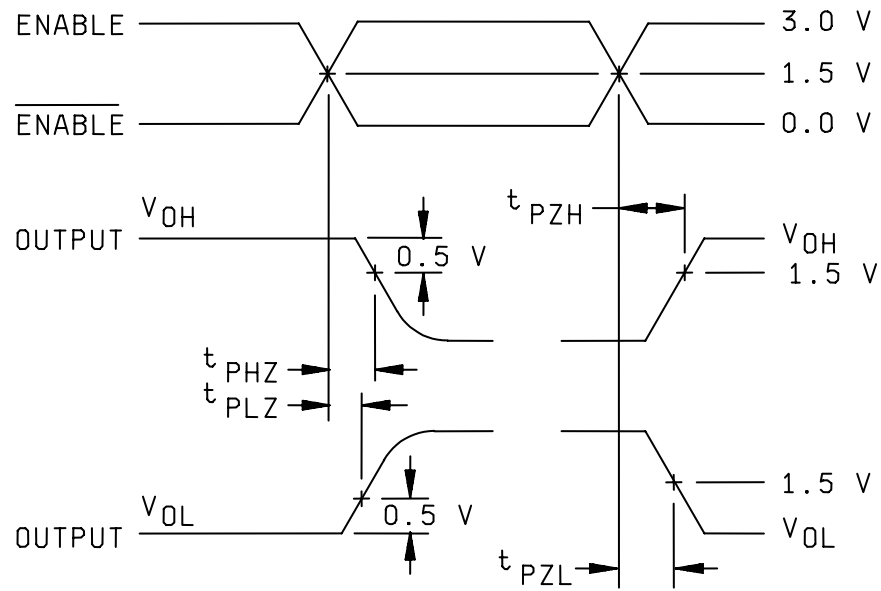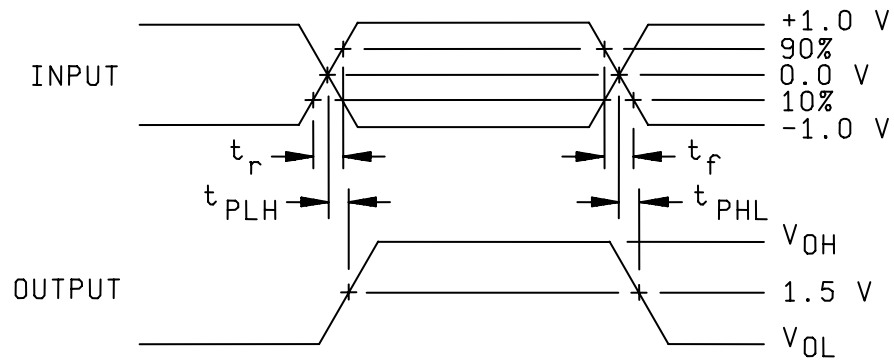
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FIGURE 3. Switching waveforms.

3.5 <u>Marking</u>. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 <u>Certification/compliance mark</u>. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 <u>Notification of change</u>. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 <u>Verification and review</u>. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a.   Burn-in test, method 1015 of MIL-STD-883.

   (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

   (2) T_A = +125°C, minimum.

b.   Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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4.3 <u>Quality conformance inspection</u>. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 <u>Group A inspection</u>.

a.   Tests shall be as specified in table II herein.

b.   Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c.   Subgroups 7 and 8 testing shall be sufficient to verify the functional operation of the device.

TABLE II. <u>Electrical test requirements</u>.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

*   PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed
    to the limits specified in table I.

4.3.2 <u>Groups C and D inspections</u>.

a.   End-point electrical parameters shall be as specified in table II herein.

b.   Steady-state life test conditions, method 1005 of MIL-STD-883.

(1)   Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3)   Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-03-10

Approved sources of supply for SMD 5962-87596 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8759601EA	3V146	26LS34/BEA
	3/	AM26LS34/BEA
5962-8759601FA	3V146	26LS34/BFA
	3/	AM26LS34/BFA
5962-87596012A	3V146	26LS34/B2A
	3/	AM26LS34/B2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics 10 Malcolm Hoyt Drive Newburyport, MA 01950

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.