REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline U. Add vendor cage 18325. Add programming method B. Changes 4.3.1c and 4.3.1e. Editorial changes throughout.	89-03-01	W. Heckman
B	Add device type 02, editorial changes throughout. Add test circuit to figure 3. Add vendor CAGE 34649 for case outline U.	90-03-09	W. Heckman
C	Add symbols, definitions, and functional descriptions. Convert to one part - one part number format.	91-02-14	W. Heckman
D	Changes in accordance with NOR 5962-R231-92.	92-07-16	M. Poelking
E	Add device types 03 - 06. Add case outlines X, Y. Editorial changes throughout.	96-01-02	M. Poelking
F	Add paragraph 6.7 PIN supersession information. Update boilerplate to MIL-PRF-38535 requirements. - LTG	04-09-03	Thomas M. Hess
G	Add device types 07 and 08. Update boilerplate to current MIL-PRF-38535 requirements. - CFS	07-02-09	Thomas M. Hess
H	Add QD device criteria to paragraphs 3.1 and 3.5.1. - CFS	07-09-04	Thomas M. Hess
J	Correct the clock rising edge to input data valid, t_{XHDV}, from minimum column to the maximum column, in table I. Change margin test method B: 5, 6, and 8, in section 4.2.1. - PHN	12-11-06	Thomas M. Hess

REV																				
SHEET																				
REV	J	J	J	J	J	J	J	J	J	J	J	J	J							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27							

REV STATUS	REV	J	J	J	J	J	J	J	J	J	J	J	J	J
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Thomas M. Hess

CHECKED BY
Thomas M. Hess

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
23 July 1987

REVISION LEVEL
J

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, DIGITAL, 8-BIT CHMOS MICROCONTROLLER WITH 4K BYTES EPROM MEMORY, MONOLITHIC SILICON

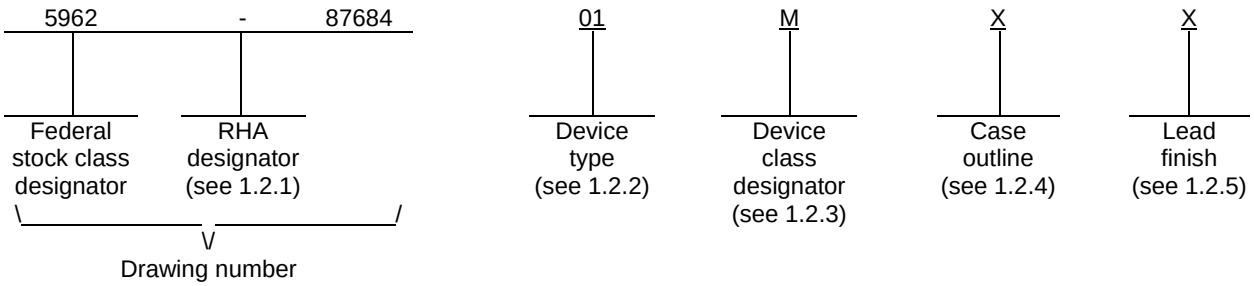
SIZE	CAGE CODE	
A	**67268**	**5962-87684**

SHEET 1 OF 27

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device class V), high reliability (device classes M and Q), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Temperature range
01	87C51	8-bit microcontroller with 4k-bytes EPROM memory. (3.5 to 12MHz)	-55°C to 125°C
02	87C51-16	8-bit microcontroller with 4k-bytes EPROM memory. (3.5 to 16MHz)	-55°C to 125°C
03	87C51	8-bit microcontroller with one time programmable memory. (3.5 to 12MHz)	-40°C to 85°C
04	87C51-16	8-bit microcontroller with one time programmable memory. (3.5 to 16MHz)	-40°C to 85°C
05	87C51	8-bit microcontroller with one time programmable memory. (3.5 to 12MHz)	-55°C to 125°C
06	87C51-16	8-bit microcontroller with one time programmable memory. (3.5 to 16MHz)	-55°C to 125°C
07	87C51	8-bit microcontroller with 4k-bytes one time programmable memory. (3.5 to 12MHz)	-55°C to 125°C
08	87C51-16	8-bit microcontroller with 4k-bytes one time programmable memory. (3.5 to 16MHz)	-55°C to 125°C

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
N	Certification and qualification to MIL-PRF-38535 with a nontraditional performance environment (encapsulated in plastic)
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835, JEDEC Publication 95, and as follows:

Outline letter	Descriptive designator	Terminals	Package style	Document
U	CQCC1-N44	44	Square leadless chip carrier 1/	MIL-STD-1835
Q	CDIP2-T40 or GDIP1-T40	40	Dual-in-line 1/	MIL-STD-1835
M	GQCC1-J44	44	J-leaded chip carrier 1/	MIL-STD-1835
X	See figure 1	40	Plastic dual-in-line	JEP 95
Y	See figure 1	44	Plastic J-leaded chip carrier	JEP 95

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 2/

Storage temperature range ..... -65°C to +150°C
Voltage on $\overline{EA}/V_{PP}$ pin to V_{SS} ..... 0 V dc to +13.0 V dc
Voltage on any pin to V_{SS} ..... -0.5 V dc to +6.5 V dc
Power dissipation (P_D) ..... 1.5 W
Maximum junction temperature (T_J) ..... +200°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}):
  Cases U, Q, and M ..... See MIL-STD-1835
  Case X ..... 15°C/W
  Case Y ..... 14°C/W

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) ..... 5.0 V dc ±10%
Case operating temperature range (T_C)
  Devices 01, 02, 05, 06, 07, 08 ..... -55°C to +125°C
  Devices 03, 04 ..... -40°C to +85°C
Maximum input low voltage (except EA) ..... $0.2V_{CC}$ - 0.25 V
Maximum input low voltage (EA) ..... $0.2V_{CC}$ - 0.45 V
Minimum input high voltage (except XTAL1, RESET) ..... $0.2V_{CC}$ + 1.1 V
Minimum input high voltage (XTAL1 & RESET) ..... $0.7V_{CC}$ + 0.2 V

1/ For device types 01 and 02 only, the lid shall be transparent to permit ultraviolet light erasure.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer's QM plan, the "QD" certification mark shall be used in place of the "Q" or "QML" certification mark.

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime 's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.

3.11.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.6 and table III.

3.11.3 Verification of erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input low voltage (except EA)	V_{IL}			1, 2, 3	All	0 2/	0.2 V_{CC} 0.25	V
Input low voltage to $\overline{EA}$	V_{IL1}			1, 2, 3	All	0 2/	0.2V_{CC} 0.45	V
Input high voltage (except XTAL1, RESET)	V_{IH}			1, 2, 3	All	0.2V_{CC} +1.1	V_{CC} +0.5 2/	V
Input high voltage (XTAL1, RESET)	V_{IH1}			1, 2, 3	All	0.7V_{CC} +0.2	V_{CC} +0.5 2/	V
Output low voltage (Ports 1, 2, 3)	V_{OL}	I_{OL} = 1.6 mA	$V_{IN} = V_{IH}$ min, V_{IL} max, V_{CC} = 4.5 V	1, 2, 3	All		0.45	V
Output low voltage Port 0, ALE, $\overline{PSEN}$	V_{OL1}	I_{OL} = 3.2 mA		1, 2, 3	All		0.45	V
Output high voltage (Ports 1, 2, 3)	V_{OH}	I_{OH} = -60 µA		1, 2, 3	All	2.4		V
		I_{OH} = -10 µA		1, 2, 3	All	0.90V_{CC}		V
Output high voltage port 0 in external bus mode, ALE, $\overline{PSEN}$	V_{OH1}	I_{OH} = -800 µA		1, 2, 3	All	2.4		V
		I_{OH} = -80 µA		1, 2, 3	All	0.90V_{CC}		V
Logic 0 input current, ports 1, 2, 3	I_{IL}	V_{IN} = 0.45 V		1, 2, 3	All		-75	µA
Logic 1 to 0 transition current ports 1, 2, 3	I_{TL}			1, 2, 3	All		-750	µA
Input leakage current port 0	I_{LI}	$V_{IN} = V_{IH}$ min		1, 2, 3	All	0	10	µA
		$V_{IN} = V_{IL}$ max		1, 2, 3	All	0	-10	µA
Reset pull down resistor	R_{RST}			1, 2, 3	All	50	300	kΩ
Pin capacitance	C_{IO}	See 4.4.1c		4	All		25	pF
Supply current:	I_{CC1}			1, 2, 3	01, 03,			
Running at 12 MHz		3/			05, 07		35	mA
Idle at 12 MHz 4/							6	mA
Power down							75	µA
Supply current:	I_{CC2}			1, 2, 3	02, 04,			
Running at 16 MHz		3/			06, 08		40	mA
Idle at 16 MHz 4/							7	mA
Power down							75	µA
Functional tests		See 4.4.1b		7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS							
Oscillator frequency	$1/t_{CLCL}$	See figure 4 5/ 6/	9, 10, 11	01, 03, 05, 07	3.5	12.0	MHz
			9, 10, 11	02, 04, 06, 08	3.5	16.0	
			9, 10, 11	All	3.5	12.0	
ALE pulse width	t_{LHLL}		9, 10, 11	01, 03, 05, 07	112		ns
			9, 10, 11	02, 04, 06, 08	68		
			9, 10, 11	All	$2t_{CLCL}$ -55		
Address valid to ALE low	t_{AVLL}		9, 10, 11	01, 03, 05, 07	13.0		ns
			9, 10, 11	02, 04, 06, 08	5.0		
			9, 10, 11	All	t_{CLCL} -70 7/		
Address hold after ALE low	t_{LLAX}		9, 10, 11	01, 03, 05, 07	33.0		ns
			9, 10, 11	02, 04, 06, 08	12.0		
			9, 10, 11	All	t_{CLCL} -50		
ALE low to valid instr. in	t_{LLIV}		9, 10, 11	01, 03, 05, 07		218	ns
			9, 10, 11	02, 04, 06, 08		132	
			9, 10, 11	All		$4t_{CLCL}$ 115	
ALE low to $\overline{\text{PSEN}}$ low	t_{LLPL}		9, 10, 11	01, 03, 05, 07	28		ns
			9, 10, 11	02, 04, 06, 08	7.0		
			9, 10, 11	All	t_{CLCL} -55		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{PSEN}$ pulse width	t_{PLPH}	See figure 4 5/ 6/	9, 10, 11	01, 03, 05, 07	190		ns
			9, 10, 11	02, 04, 06, 08	125		
			9, 10, 11	All	$3t_{CLCL}$ -60		
$\overline{PSEN}$ low to valid instr. in	t_{PLIV}		9, 10, 11	01, 03, 05, 07		130	ns
			9, 10, 11	02, 04, 06, 08		65	
			9, 10, 11	All		$3t_{CLCL}$ -120	
Input instr. hold after $\overline{PSEN}$	t_{PXIX}		9, 10, 11	All	0		ns
Input instr. float after $\overline{PSEN}$	t_{PXIZ}		9, 10, 11	01, 03, 05, 07		58	ns
			9, 10, 11	02, 04, 06, 08		37	
			9, 10, 11	All		t_{CLCL} -25	
Address to valid instr. in	t_{AVIV}		9, 01, 11	01, 03, 05, 07		312	ns
			9, 10, 11	02, 04, 06, 08		188	
			9, 10, 11	All		$5t_{CLCL}$ -120	
$\overline{PSEN}$ low to address float	t_{PLAZ}		9, 10, 11	All		25	ns
$\overline{RD}$ pulse width	t_{RLRH}		9, 10, 11	01, 03, 05, 07	400		ns
			9, 10, 11	02, 04, 06, 08	270		
			9, 10, 11	All	$6t_{CLCL}$ -100		
$\overline{WR}$ pulse width	t_{WLWH}		9, 10, 11	01, 03, 05, 07	400		ns
			9, 10, 11	02, 04, 06, 08	270		
			9, 10, 11	All	$6t_{CLCL}$ -100		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{RD}$ low to valid data in	t_{RLDV}	See figure 4 5/ 6/	9, 10, 11	01, 03, 05, 07		232	ns
			9, 10, 11	02, 04, 06, 08		123	
			9, 10, 11	All		$5t_{CLCL}$ -185	
Data hold after $\overline{RD}$	t_{RHDX}		9, 10, 11	All	0		ns
Data float after $\overline{RD}$	t_{RHDZ}		9, 10, 11	01, 03, 05, 07		82	ns
			9, 10, 11	02, 04, 06, 08		38	
			9, 10, 11	All		$2t_{CLCL}$ -85	
ALE low to valid data in	t_{LLDV}		9, 10, 11	01, 03, 05, 07		496	ns
			9, 10, 11	02, 04, 06, 08		320	
			9, 10, 11	All		$8t_{CLCL}$ -170	
Address to valid data in	t_{AVDV}		9, 10, 11	01, 03, 05, 07		565	ns
			9, 10, 11	02, 04, 06, 08		370	
			9, 10, 11	All		$9t_{CLCL}$ -185	
ALE low to $\overline{RD}$ or $\overline{WR}$ low	t_{LLWL}		9, 10, 11	01, 03, 05, 07	185	315	ns
			9, 10, 11	02, 04, 06, 08	120	250	
			9, 10, 11	All	$3t_{CLCL}$ -65	$3t_{CLCL}$ +65	
Address to $\overline{RD}$ or $\overline{WR}$ low	t_{AVWL}		9, 10, 11	01, 03, 05, 07	188		ns
			9, 10, 11	02, 04, 06, 08	102		
			9, 10, 11	All	$4t_{CLCL}$ -145		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data valid to $\overline{WR}$ transition	t_{QVWX}	See figure 4 5/ 6/	9, 10, 11	01, 03, 05, 07	8.0		ns
			9, 10, 11	02, 04, 06, 08	5.0		
			9, 10, 11	All	t_{CLCL} -75 7/		
Data hold after $\overline{WR}$	t_{WHQX}		9, 10, 11	01, 03, 05, 07	18		ns
			9, 10, 11	02, 04, 06, 08	5.0		
			9, 10, 11	All	t_{CLCL} -65 7/		
$\overline{RD}$ low to address float	t_{RLAZ}		9, 10, 11	All		0	ns
$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{WHLH}		9, 10, 11	01, 03, 05, 07	18	148	ns
			9, 10, 11	02, 04, 06, 08	5.0	127	
			9, 10, 11	All	t_{CLCL} -65 7/	t_{CLCL} +65	
Serial port clock cycle time	t_{XLXL}	See figure 4 4/ 5/ 6/	9, 10, 11	01, 03, 05, 07	1000 8/		ns
			9, 10, 11	02, 04, 06, 08	740 8/		
			9, 10, 11	All	$12t_{CLCL}$ 8/		
Output data setup to clock rising edge	t_{QVXH}		9, 10, 11	01, 03, 05, 07	700		ns
			9, 10, 11	02, 04, 06, 08	484		
			9, 10, 11	All	$10t_{CLCL}$ -133		
Output data hold after clock rising edge	t_{XHQX}		9, 10, 11	01, 03, 05, 07	50		ns
			9, 10, 11	02, 04, 06, 08	6.0		
			9, 10, 11	All	$2t_{CLCL}$ -117		
Input data hold after clock rising edge	t_{XHDX}		9, 10, 11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock rising edge to input data valid	t_{XHDV}	See figure 4 2/ 4/ 5/	9, 10, 11	01, 03, 05, 07		700	ns
			9, 10, 11	02, 04, 06, 08		484	
			9, 10, 11	All		$10t_{CLCL}$ -133	
High time	t_{CHCX}		9, 10, 11	All	20		ns
Low time	t_{CLCX}		9, 10, 11	All	20		ns
Rise time	t_{CLCH}		9, 10, 11	All		20	ns
Fall time	t_{CHCL}		9, 10, 11	All		20	ns

1/ All testing to be performed using worst-case test conditions unless otherwise specified. The case operating temperature of each device shall be as specified in paragraph 1.4.

2/ Guaranteed, if not tested, to the limits specified.

3/ I_{CC} is measured with all output pins disconnected: XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, $V_{IL} = V_{SS} + 0.5\ V$, $V_{IH} = V_{CC} - 0.5\ V$ measured with $\overline{EA}$ and RESET connected to V_{CC}. "Idle" current is measured with $\overline{EA}$ and RESET connected to V_{SS}. "Power down" current is measured with $\overline{EA}$ connected to V_{SS} and RESET connected to V_{SS}.

4/ Due to test equipment limitations, actual tested values may differ from those specified, but specified limits are guaranteed.

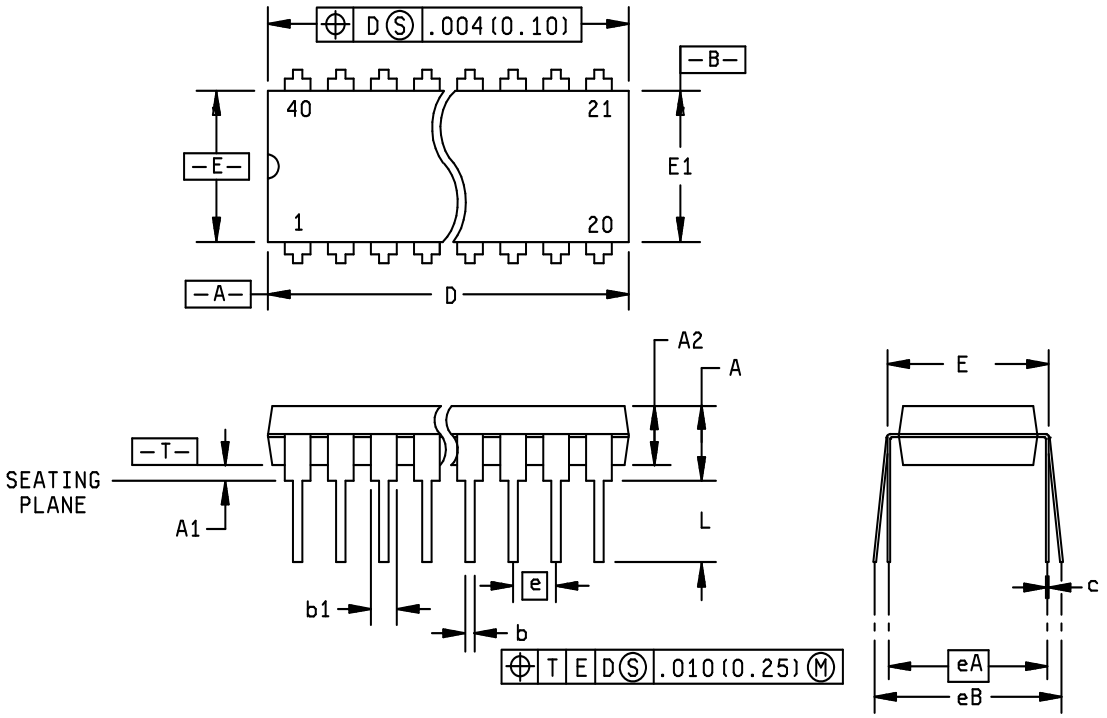
5/ All devices to be tested at 16 MHz only, but guaranteed across the specified operating frequency. Devices not meeting the limits of the 16 MHz devices may be retested to be supplied at the slower 12 MHz speed grade.

6/ Parametric values are based on a 12 MHz oscillator for device types 01 and 07, a 16 MHz oscillator for devices type 02 and 08, and a variable oscillator for all other devices.

7/ When using timing equations, the minimum value shall not be less than 5 ns.

8/ Parametric values are typical values rather than minimum values.

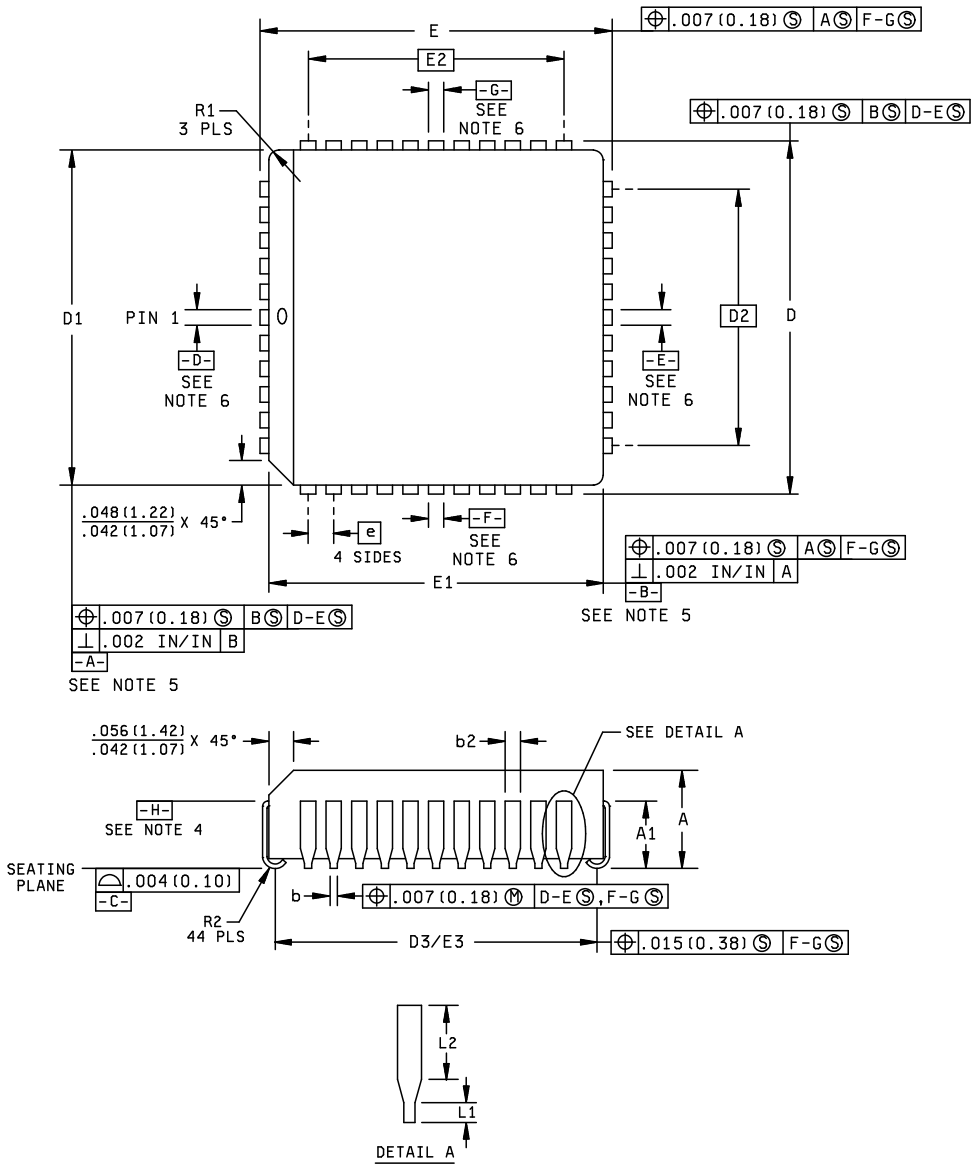
Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	4.19	5.08	.165	.200	e	2.54 BSC		.100 BSC	
A1	0.51	1.14	.020	.045	E	15.24	15.75	.600	.620
A2	3.68	3.94	.145	.155	E1	13.84	14.10	.545	.555
b	0.43	0.56	.017	.022	eA	15.24 bsc		.600 bsc	
b1	1.14	1.63	.045	.064	eB	15.24	17.65	.600	.695
c	0.25	0.38	.010	.015	L	3.05	3.51	.120	.138
D	51.94	52.45	2.045	2.065					

FIGURE 1. Case outlines.

Case Y



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	4.19	4.57	0.165	0.180	E	17.40	17.65	0.685	0.695
A1	2.29	3.05	0.090	0.120	E1	16.51	16.66	0.650	0.656
b	0.33	0.53	0.013	0.021	E2	12.70		0.500	
b2	0.66	0.81	0.026	0.032	e	1.27		0.050	
D	17.40	17.65	0.685	0.695	L1	0.64		0.025	
D1	16.51	16.66	0.650	0.656	L2	1.52		0.060	
D2	12.70		0.500		R1		0.25		0.010
D3/E3	14.99	16.00	0.590	0.630	R2	0.64	1.14	0.025	0.045

FIGURE 1. Case outlines – Continued.

Cases Q and X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	P1.0	21	P2.0(A8)
2	P1.1	22	P2.1(A9)
3	P1.2	23	P2.2(A10)
4	P1.3	24	P2.3(A11)
5	P1.4	25	P2.4(A12)
6	P1.5	26	P2.5(A13)
7	P1.6	27	P2.6(A14)
8	P1.7	28	P2.7(A15)
9	RESET	29	PSEN
10	(RXD)P3.0	30	ALS/PROG
11	(TXD)P3.1	31	EA/V_{PP}
12	(INT0)P3.2	32	P0.7(AD7)
13	(INT1)P3.3	33	P0.6(AD6)
14	(TO)P3.4	34	P0.5(AD5)
15	(TI)P3.5	35	P0.4(AD4)
16	(WR)P3.6	36	P0.3(AD3)
17	(RD)P3.7	37	P0.2(AD2)
18	XTAL2	38	P0.1(AD1)
19	XTAL1	39	P0.0(AD0)
20	V_{SS}	40	V_{CC}

Cases U, M, and Y			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	23	NC
2	P1.0	24	P2.0(A8)
3	P1.1	25	P2.1(A10)
4	P1.2	26	P2.2(A10)
5	P1.3	27	P2.3(A11)
6	P1.4	28	P2.4(A12)
7	P1.5	29	P2.5(A13)
8	P1.6	30	P2.6(A14)
9	P1.7	31	P2.7(A15)
10	RESET	32	PSEN
11	(RXD)P3.0	33	AL/PRO
12	NC	34	NC
13	(TXD)P3.1	35	EA/V_{PP}
14	(INTO)P3.2	36	P0.7(AD7)
15	(INT1)P3.3	37	P0.6(AD6)
16	(TO)P3.4	38	P0.5(AD5)
17	(T1)P3.5	39	P0.4(AD4)
18	(WR)P3.6	40	P0.3(AD3)
19	(RD)P3.7	41	P0.2(AD2)
20	XTAL2	42	P0.1(AD1)
21	XTAL1	43	P0.0(AD0)
22	V_{SS}	44	V_{CC}

FIGURE 2. Terminal connections.

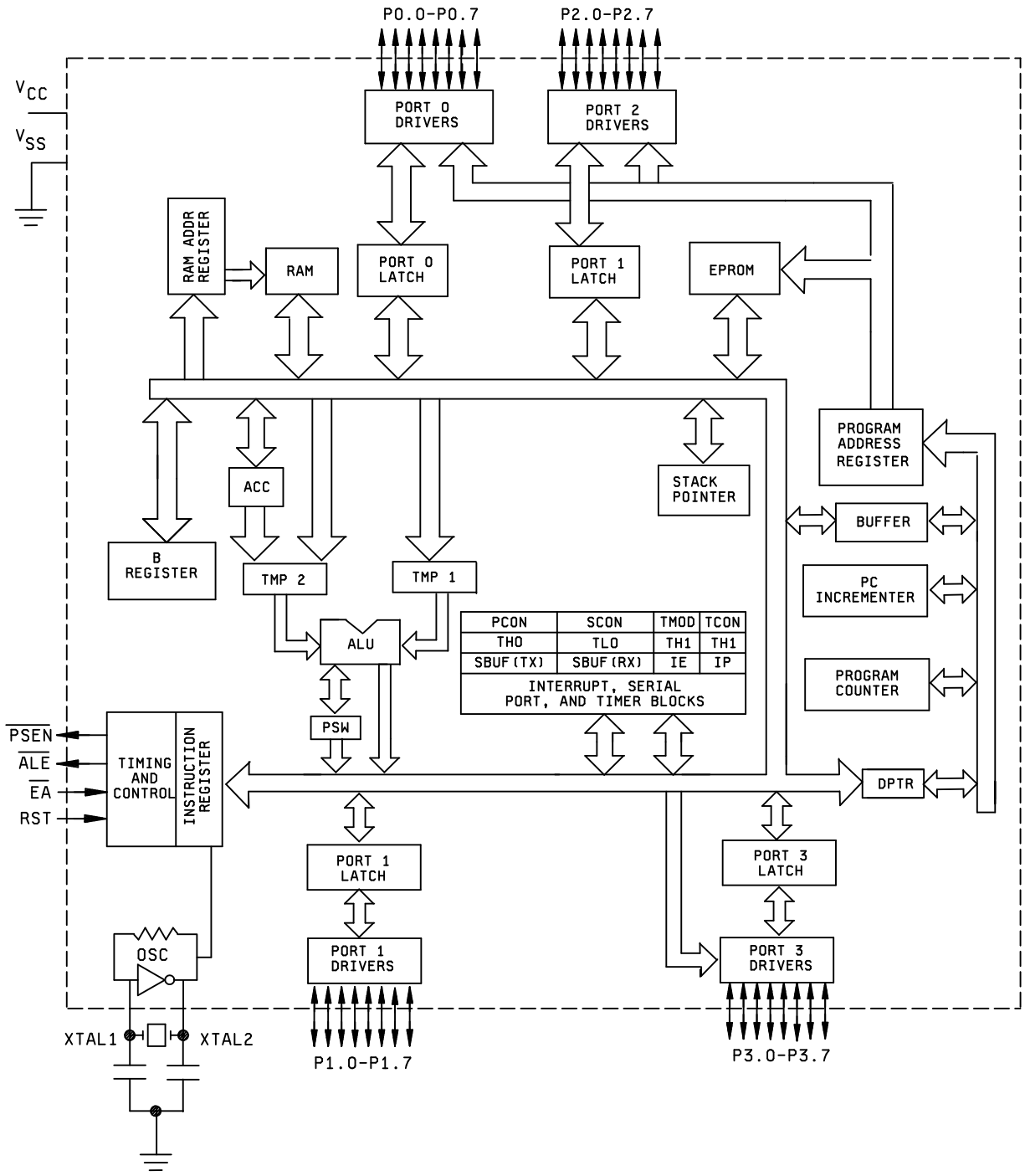
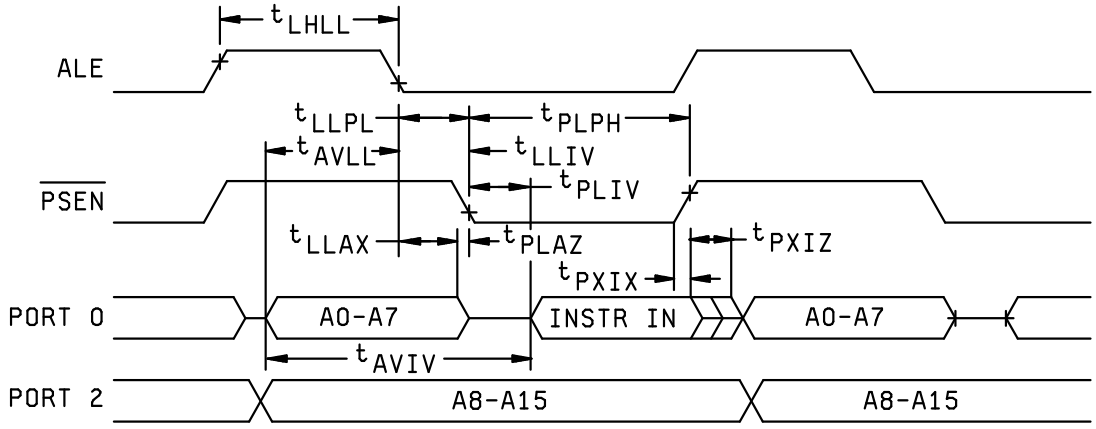


FIGURE 3. Block diagram.

EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE

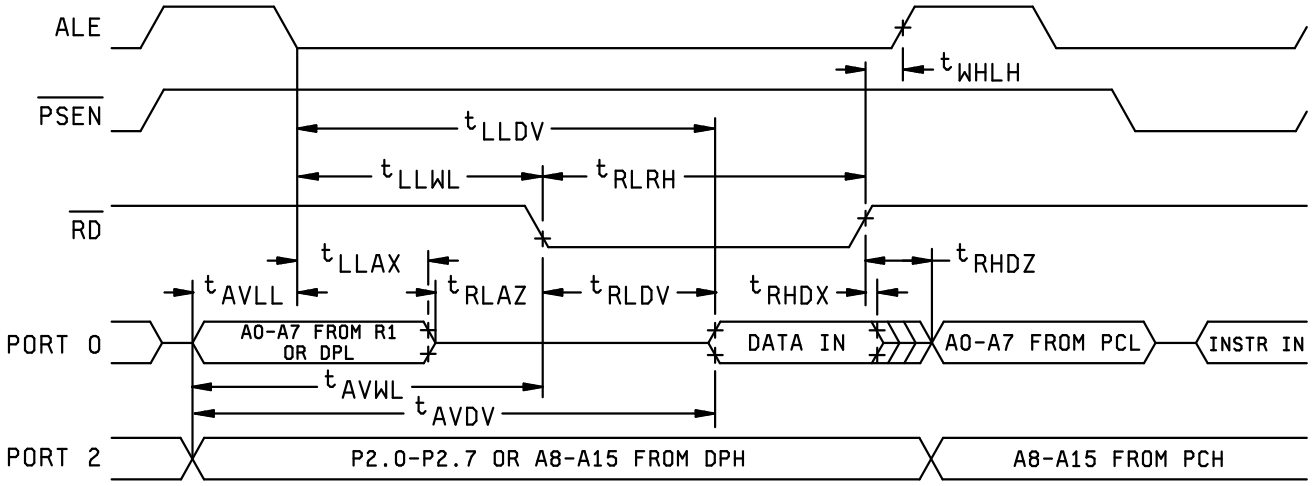
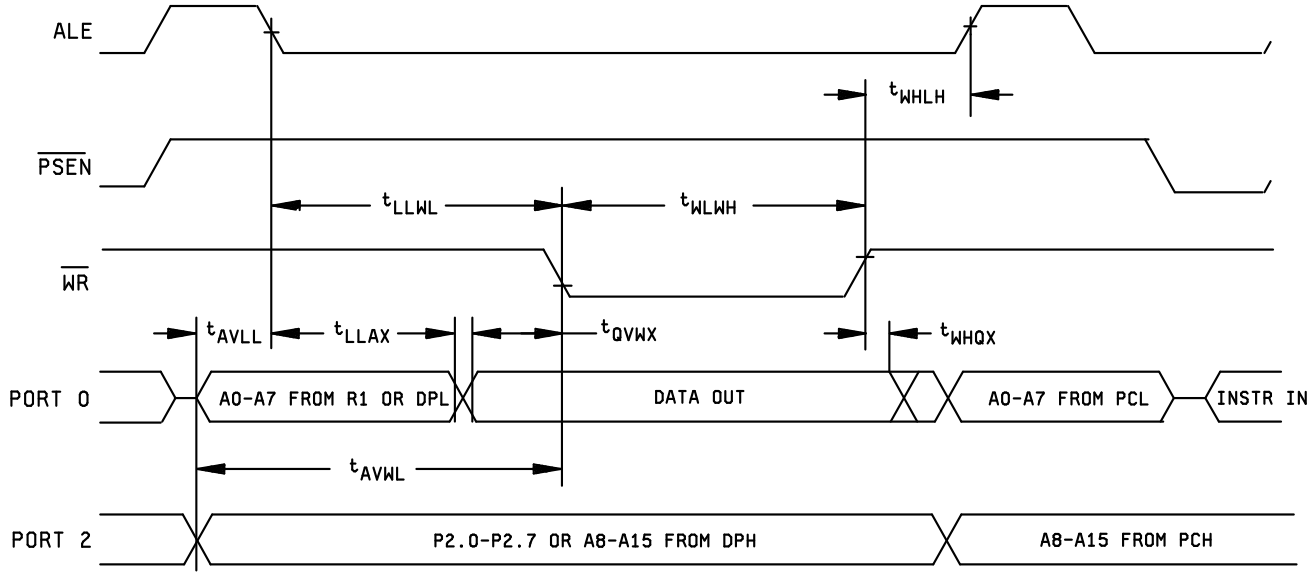


FIGURE 4. Test circuit and switching waveforms.

EXTERNAL DATA MEMORY WRITE CYCLE



EXTERNAL CLOCK DRIVE WAVEFORM

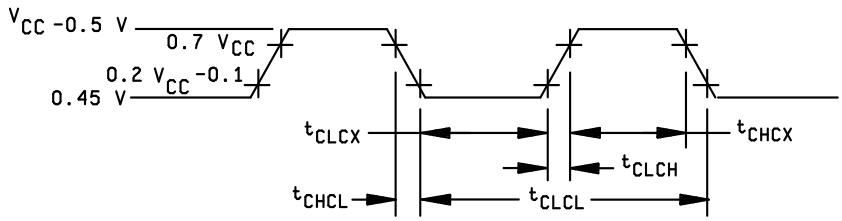
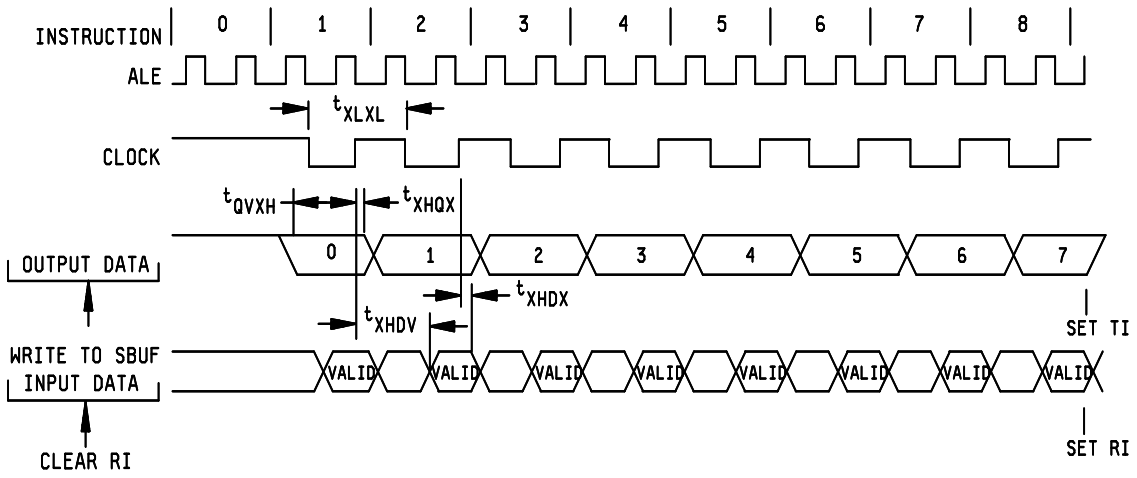
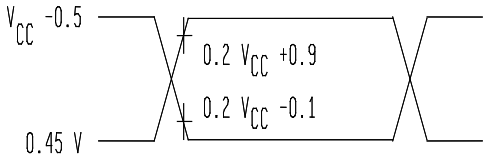
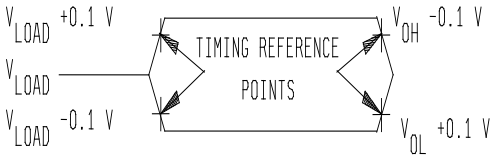


FIGURE 4. Test circuit and switching waveforms – Continued.



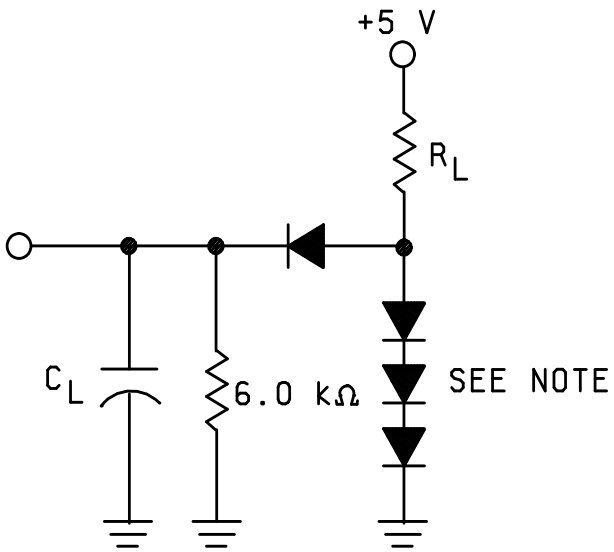


AC inputs during testing are driven at V_{CC} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IH} minimum for a logic '1' and V_{IL} maximum for a logic '0'.



For timing purposes, a port pin ceases floating when a 100 mV change from load voltage occurs and begins floating when a 100 mV change from loaded V_{OH} or V_{OL} level occurs. I_{OL} or $I_{OH} \geq \pm 20$ mA.

FIGURE 4. Test circuit and switching waveforms – Continued.



Output	R_L	C_L
Port 0, ALE, PSEN	1.2 kΩ	100pF
All other outputs	2.4 kΩ	80 pF

Notes:
1. All diodes are 1n914 or equivalent.
2. C_L includes tester and fixture capacitance.

FIGURE 4. Test circuit and switching waveforms – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A.

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.11.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at 140°C to screen for data retention lifetime.

(3) Perform a margin test using V_m = 5.9 V at 25°C using loose timing (i.e., T_{ACC} > 1 μs).

(4) Perform dynamic burn-in (see 4.2.1a).

(5) Margin at V_m = 5.9 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.11.1), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.11.3).

Margin test method B.

(1) Program at +25°C 100 percent of the bits.

(2) Bake, unbiased, for 24 hours at +250°C.

(3) Perform margin test at V_m = 5.9 V.

(4) Erase (see 3.11.1).

(5) For device types 01, 02 Program **50**% of the bits and verify (see 3.11.2).

(6) Perform interim electrical tests in accordance with table II.

(7) Perform burn-in (see 4.2.1a).

(8) One-hundred percent test at 25°C (group A, subgroups 1 and 7). V_m = **5.5** V with loose timing, apply PDA. For device types 03 - 08, the virgin state of the device must be verified.

(9) Perform remaining final electrical subgroups and group A testing.

(10) For device types 01, 02, erase devices may be submitted for groups B, C, and D at this time.

(11) For device types 01, 02, verify erasure (see 3.11.3). Steps 1 through 4 are performed at wafer level.

4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IO} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

d. All devices selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

e. The device types 03 - 08 shall be tested for programmability and AC performance compliance to the requirements of group A, subgroups 9, 10, 11. Either of the two techniques is acceptable.

(1) Testing the entire lot using additional built in test circuitry which allows the manufacturer to verify programmability and AC performance without programming user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, 11, group A testing per the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, 11. Twelve devices shall be submitted to programming. If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. (Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, 11. If more than 2 total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.)

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)				1, 7
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 8a, 10	2, 8a, 10
Group D end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 8a, 10	2, 8a, 10
Group E end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 8a, 10	2, 8a, 10

1/ PDA applies to subgroup 1 and 7.
2/ PDA applies to subgroups 2 and 8.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

a. For device types 01 and 02, all devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

b. For device types 03 - 08, the programmability shall be verified per 4.4.1e

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.5 Erasing procedure. The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-s/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

4.6 Programming procedures. The programming characteristics in table III and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration (see figure 5) for programming. The waveforms of figure 6 and programming characteristics of table III shall apply.

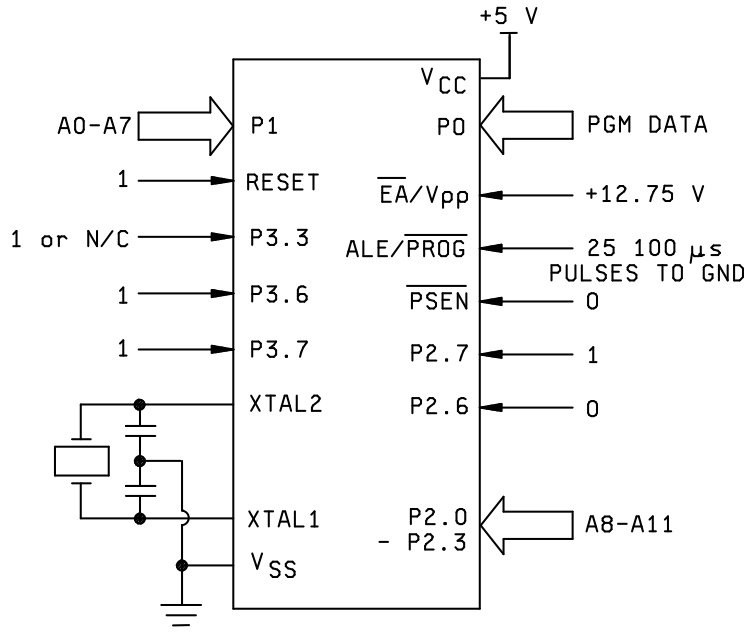
b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.5).

TABLE III. Programming characteristics.

Parameter	Symbol	Conditions	Limits		Unit
			Min	Max	
Programming supply voltage	V_{PP}	See figures 5, 6	12.5	13.0	V
Programming supply current	I_{PP}	1/		50	mA
Oscillator frequency	$1/t_{CLCL}$		4	6	MHz
Address setup to $\overline{\text{PROG}}$ low 2/	t_{AVGL}		$48t_{CLCL}$		ns
Address hold after $\overline{\text{PROG}}$ 2/	t_{GHAX}		$48t_{CLCL}$		
Data setup to $\overline{\text{PROG}}$ low 2/	t_{DVGL}		$48t_{CLCL}$		
Data hold after $\overline{\text{PROG}}$ 2/	t_{GHDX}		$48t_{CLCL}$		
P2.7 ($\overline{\text{ENABLE}}$) high to VP 2/	t_{EHSH}		$48t_{CLCL}$		
V_{PP} setup to $\overline{\text{PROG}}$ low 2/	t_{SHGL}		10		μs
V_{PP} hold after $\overline{\text{PROG}}$ 2/	t_{GSHL}		10		
$\overline{\text{PROG}}$ width 2/	t_{GLGH}		90	110	
Address to data 2/	t_{AVQV}			$48t_{CLCL}$	ns
$\overline{\text{ENABLE}}$ low to data valid 2/	t_{ELQV}			$48t_{CLCL}$	
Data float after $\overline{\text{ENABLE}}$ 2/	t_{EHQZ}			$48t_{CLCL}$	
$\overline{\text{PROG}}$ high to $\overline{\text{PROG}}$ low 2/	t_{GHGL}		10		μs

1/ For programming specifications, T_C = 21°C to 27°C, V_{CC} = 5.0 V ±10 percent, V_{SS} = 0 V.

2/ Due to test equipment limitations, actual tested values may differ from those specified, but specified limits are guaranteed.



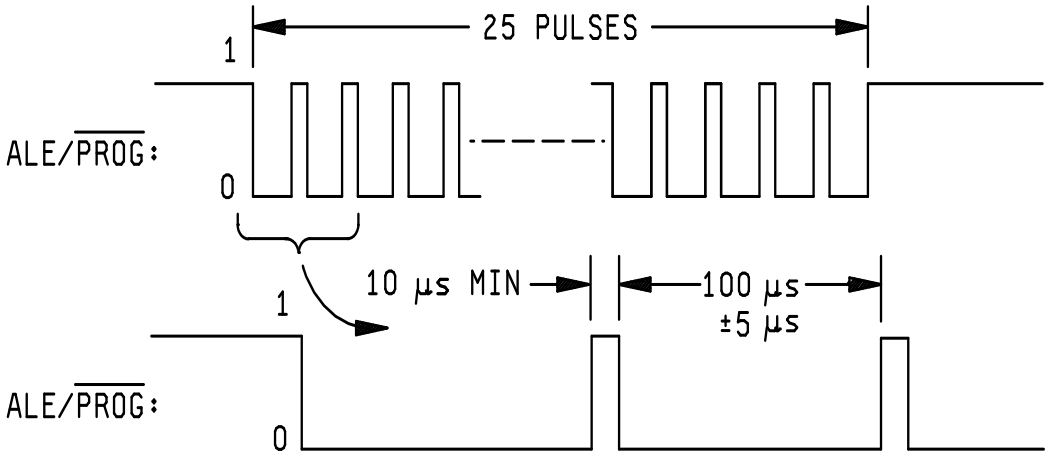
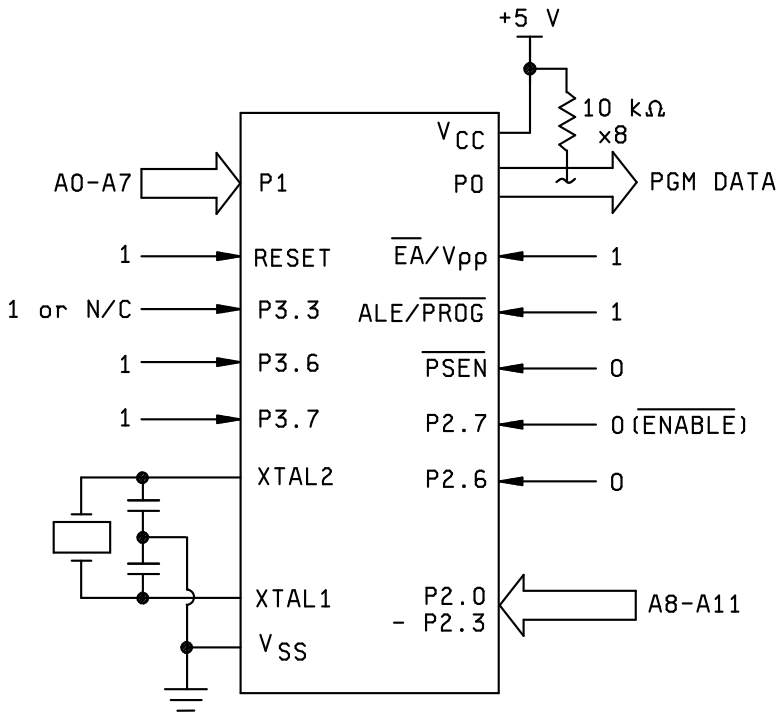


FIGURE 5. Programming waveforms.



EPROM PROGRAMMING AND VERIFICATION WAVEFORMS

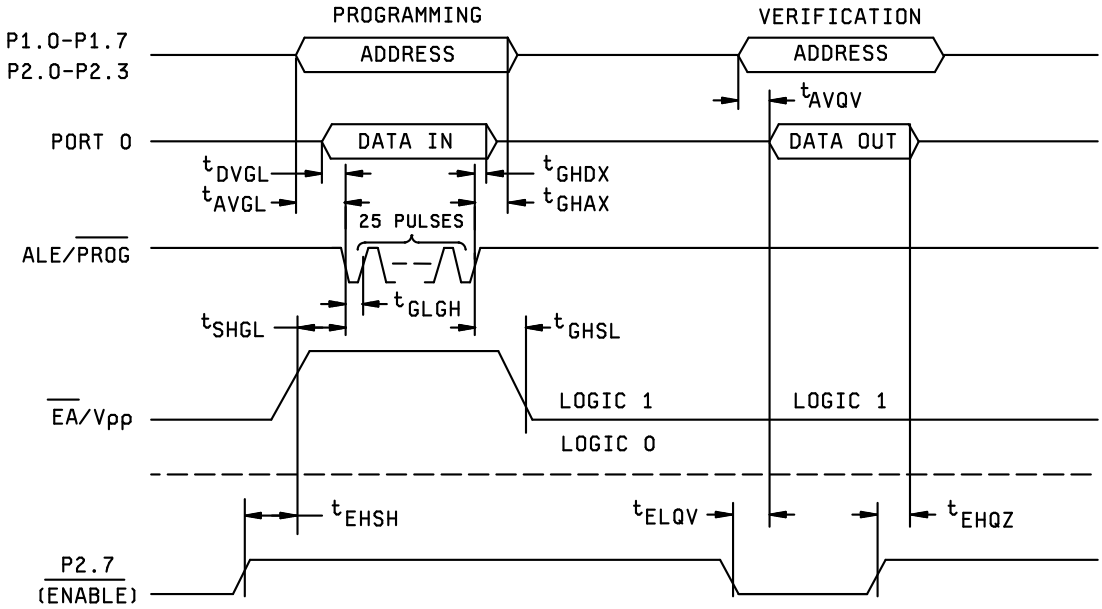


FIGURE 6. Programming verification.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0547.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and as follows:

Port 0. Port 0 is an 8-bit open drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullups when emitting 1's. Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1. Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 1 also receives the low-order address bytes during EPROM programming and program verification.

Port 2. Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX at DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external data memory that used 8-bit addresses (MOVX at Ri), Port 2 emits the contents of the P2 special function register. Port 2 also receives some control signals and the high order address bits during EPROM programming and program verification.

Port 3. Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 also serves the functions of various special features of the MCS-51 family, as listed below:

Port pin	Alternate function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

Port 3 also receives some control signals for EPROM programming and program verification.

RST. Reset input. A logic high on this pin for two machine cycles while the oscillator is running resets the device. An internal pulldown resistor permits a power-on reset to be generated using only an external capacitor to V_{CC}.

ALE/PROG. Address latch enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during EPROM programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

PSEN. Program store enable is the read strobe to external program memory. When the device is executing from internal program memory, PSEN is inactive (high). When the device is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/V_{PP}. External access enable. EA must be externally held low in order to enable the device to fetch code from external program memory locations 0000H to 0FFFH. If either of the lock bits is programmed, the logic level at EA is internally latched during reset. EA must be strapped to V_{CC} for internal program execution. This pin also receives the 12.75 V programming supply voltage (V_{PP}) during EPROM programming.

XTAL1. Output from the inverting oscillator amplifier and input to the internal block generator circuits.

XTAL2. Output from the inverting oscillator amplifier.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

6.7 Supersession Data. The PIN supersession data shall be as follows:

NEW PIN	OLD PIN
5962-8768401MQX	5962-8768401QX
5962-8768401MUX	5962-8768401UX
5962-8768402MQX	5962-8768402QX
5962-8768402MUX	5962-8768402UX

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-11-06

Approved sources of supply for SMD 5962-87684 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8768401QA	3V146	MD87C51/BQA
5962-8768401UA	3V146	MR87C51/BQA
5962-8768401MQA	3V146	87C51/BQA
5962-8768401MUA	3V146	87C51/BUA
5962-8768401MMA	3V146	87C51/BMA
5962-8768402QA	3V146	MD87C51-16/BQA
5962-8768402UA	3V146	MR87C51-16/BUA
5962-8768402MQA	3V146	87C51-16/BQA
5962-8768402MUA	3V146	87C51-16/BUA
5962-8768402MMA	3V146	87C51-16/BMA
5962-8768403NXA	3/	87C51/IN40A
5962-8768403NYA	3/	87C51/IN44A
5962-8768404NXA	3/	87C51-16/IN40A
5962-8768404NYA	3/	87C51-16/IN44A
5962-8768405NXA	3/	87C51/CN40A
5962-8768405NYA	3/	87C51/CN44A
5962-8768406NXA	3/	87C51-16/CN40A
5962-8768406NYA	3/	87C51-16/CN44A
5962-8768407MQA	0C7V7	87C51/BQA OTP
5962-8768407MUA	0C7V7	87C51/BUA OTP
5962-8768407MMA	0C7V7	87C51/BMA OTP
5962-8768408MQA	0C7V7	87C51-16/BQA OTP
5962-8768408MUA	0C7V7	87C51-16/BUA OTP
5962-8768408MMA	0C7V7	87C51-16/BMA OTP

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	e2v aerospace and defense, inc. dba QP Semiconductor, Inc. 765 Sycamore Drive Milpitas, CA 95035
3V146	Rochester Electronics, Inc. 16 Malcolm Hoyt Drive Newburyport, MA 01950