REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical changes in table I. Editorial changes throughout.	90-08-27	W. Heckman
B	Added Rochester as source of supply Vendor cage 3V146. Updated boilerplate and made editorial changes throughout. – LTG	01-01-04	Thomas M. Hess
C	Made editorial change to table I, sheet 5 on the V_{IL} test in the max column. Updated bulletin page. - LTG	01-12-13	Thomas M. Hess
D	Correct t_{CLLH} maximum limit in table I. Update boilerplate to MIL-PRF-38535 requirements. - CFS	04-05-04	Thomas M. Hess
E	Update boilerplate to current MIL-PRF-38535 requirements. - CFS	09-05-05	Thomas M. Hess

REV																				
SHEET																				
REV	E	E	E	E	E	E	E	E	E	E	E	E	E							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27							

REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles Reusing

APPROVED BY
William K. Heckman

DRAWING APPROVAL DATE
89-09-14

REVISION LEVEL
E

MICROCIRCUIT, DIGITAL, NMOS, 16-BIT MICROCONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89596**

SHEET 1 OF 27

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89596	01	Z	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	8097BH	12 MHz	16-bit microcontroller

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Y	See figure 1	68	Leaded chip carrier with unformed leads
Z	CMGA3-P68	68	Pin grid array package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Voltage on any pin with respect to V_{SS} or ANGND (except $\overline{EA}$) ..... -0.3 V dc to +7.0 V dc
Voltage from $\overline{EA}$ to V_{SS} or ANGND ..... -0.3 V dc to +13.0 V dc
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 1.5 W
Thermal resistance, junction-to-case (θ_{JC}):
Case Y ..... 9°C/W 1/
Case Z ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C
Lead temperature (soldering, 5 seconds) ..... +300°C

1.4 Recommended operating conditions.

Digital supply voltage range (V_{CC}) ..... 4.5 V dc to 5.5 V dc
Analog supply voltage range (V_{REF}) ..... 4.5 V dc to 5.5 V dc
Power down supply voltage range (V_{PD}) ..... 4.5 V dc to 5.5 V dc
Oscillator frequency range (f_{OSC}) ..... 6 MHz to 12 MHz
Case operating temperature range (T_C) ..... -55°C to +125°C 2/

1/ When a thermal resistance value is included in MIL-STD-1835, it shall supersede that value herein.
2/ Case temperatures are instant on.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the Qualifying Activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be as specified on figure 1 or in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Instruction set summary. The instruction set summary shall be as specified on figure 4.

3.2.5 Timing waveforms . The timing waveforms shall be as specified on figure 5.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a “C” as required in MIL-PRF-38535, Appendix A. For class Q product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s Quality Management (QM) Plan, the “QD” certification mark shall be used in place of the “QML” or “Q” certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.7 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = V_{PD} = 5\ V \pm 10\%$ $V_{SS} = ANGND = 0\ V$ $f_{OSC} = 6.0$ to 12 MHz unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current	I_{CC}	All outputs disconnected. 2/	1, 2, 3	All		275	mA
V_{PD} supply current	I_{PD}	Normal operation and power down. 2/	1, 2, 3	All		1	mA
V_{REF} supply current	I_{REF}	2/	1, 2, 3	All		8	mA
Input low voltage (except) $\overline{RESET}$	V_{IL}		1, 2, 3	All	-0.3	0.8	V
Input low voltage, $\overline{RESET}$	V_{IL1}		1, 2, 3	All	-0.3	0.7	V
Input high voltage (except $\overline{RESET}$, NMI and XTAL1)	V_{IH}		1, 2, 3	All	2.0	V_{CC} +0.5	V
Input high voltage $\overline{RESET}$ rising	V_{IH1}		1, 2, 3	All	2.4	V_{CC} +0.5	V
Input high voltage, $\overline{RESET}$ falling hysteresis	V_{IH2}		1, 2, 3	All	2.1	V_{CC} +0.5	V
Input high voltage, NMI, XTAL1	V_{IH3}		1, 2, 3	All	2.2	V_{CC} +0.5	V
Input leakage current to each pin of HSI, Port 3, Port 4 and P2.1	I_{LI}	$V_{IN} = 0$ to V_{CC} 2/	1, 2, 3	All		±10	µA
DC input leakage current to each pin of Port 0	I_{LI1}	$V_{IN} = 0$ to V_{CC} 2/	1, 2, 3	All		3	µA
Input high current to EA	I_{IH}	$V_{IH} = 2.4\ V$ 2/	1, 2, 3	All		100	µA
Input low current to Port 1, and P2.6, P2.7	I_{IL}	$V_{IL} = 0.45\ V$ 2/	1, 2, 3	All		-125	µA
Input low current to RESET	I_{IL1}	$V_{IL} = 0.45\ V$ 2/	1, 2, 3	All	-0.25	-2	mA
Input low current P2.2, P2.3, P2.4, READY, BUSWIDTH	I_{IL2}	$V_{IL} = 0.45\ V$ 2/	1, 2, 3	All		-50	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = V_{PD} = 5\ V \pm 10\%$ $V_{SS} = ANGND = 0\ V$ $f_{OSC} = 6.0$ to 12 MHz unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output low voltage on quasi-bidirectional port pins and Port 3, Port 4 when used as ports	V_{OL}	$I_{OL} = 0.8$ mA 2/ 3/	1, 2, 3	All		0.45	V
Output low voltage on quasi-bidirectional port pins and Port 3, Port 4 when used as ports	V_{OL1}	$I_{OL} = 2.0$ mA 2/ 3/ 4/ 5/	1, 2, 3	All		0.75	V
Output low voltage on standard output pins, $\overline{\text{RESET}}$ and Bus/control pins	V_{OL2}	$I_{OL} = 2.0$ mA 2/ 3/ 4/ 5/ 6/	1, 2, 3	All		0.45	V
Output high voltage on quasi-bidirectional pins	V_{OH}	$I_{OH} = -20\ \mu A$ 2/ 3/	1, 2, 3	All	2.4		V
Output high voltage on standard output pins and Bus/control pins	V_{OH1}	$I_{OH} = -200\ \mu A$ 2/ 3/	1, 2, 3	All	2.4		V
Output high current on $\overline{\text{RESET}}$	I_{OH3}	$V_{OH} = 2.4$ V 2/	1, 2, 3	All	-50		µA
Pin capacitance	C_S	f = 1.0 Mhz See 4.3.1c 2/	4	All		10	pF
Functional tests		See 4.3.1d 2/	7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = V_{PD} = 5\ V \pm 10\%$ $V_{SS} = ANGND = 0\ V$ $f_{OSC} = 6.0$ to 12 MHz unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
READY hold after CLKOUT edge	t_{CLYX}	Timing requirements (system components must meet these specifications). See figure 5. f_{OSC} = 10 MHz	9,10, 11	All	0		ns
End of ALE/$\overline{ADV}$ to READY valid	t_{LLYV}		9,10, 11	All		$2t_{OSC}$ - 70	ns
End of ALE/$\overline{ADV}$ to READY high	t_{LLYH}		9,10, 11	All	$2t_{OSC}$ +40	$4t_{OSC}$ - 80	ns
Non-READY time	t_{YLYH}		9,10, 11	All		1000	ns
Address valid to input data valid 7/	t_{AVDV}		9,10, 11	All		$5t_{OSC}$ - 120	ns
$\overline{RD}$ active to input data valid	t_{RLDV}		9,10, 11	All		$3t_{OSC}$ - 100	ns
Data hold after $\overline{RD}$ inactive	t_{RHDX}		9,10, 11	All	0		ns
$\overline{RD}$ inactive to input data float	t_{RHDZ}		9,10, 11	All	0	t_{OSC} - 25	ns
Address valid to BUSWIDTH valid 7/	t_{AVGV}		9,10, 11	All		$2t_{OSC}$ - 125	ns
BUSWIDTH hold after ALE/$\overline{ADV}$ low	t_{LLGX}		9,10, 11	All	t_{OSC} +40		ns
ALE/$\overline{ADV}$ low to BUSWIDTH valid	t_{LLGV}		9,10, 11	All		t_{OSC} -75	ns
Oscillator frequency	f_{OSC}	See figure 5.	9,10, 11	All	6.0	12.0	MHz
Oscillator period	t_{OSC}		9,10, 11	All	83	166	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = V_{PD} = 5\ V \pm 10\%$ V_{SS} = ANGND = 0 V f_{OSC} = 6.0 to 12 MHz unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
XTAL1 rising edge to clockout rising edge	t_{OHCH}	See figure 5 f_{OSC} = 10 MHz	9,10, 11	All	0	120	ns
CLKOUT period 8/	t_{CHCH}		9,10, 11	All	$3t_{OSC}$	$3t_{OSC}$	ns
CLKOUT high time	t_{CHCL}		9,10, 11	All	$3t_{OSC}$ -35	$3t_{OSC}$ +10	ns
CLKOUT low to ALE high	t_{CLLH}		9,10, 11	All	-30	+15	ns
ALE/$\overline{ADV}$ low to CLKOUT high	t_{LLCH}		9,10, 11	All	t_{OSC} -25	t_{OSC} +45	ns
ALE/$\overline{ADV}$ high time 9/	t_{LHLL}		9,10, 11	All	t_{OSC} -30 9/	t_{OSC} +35 9/	ns
Address setup to end of ALE/$\overline{ADV}$ 7/	t_{AVLL}		9,10, 11	All	t_{OSC} -50		ns
$\overline{RD}$ or $\overline{WR}$ low to address float 10/	t_{RLAZ}		9,10, 11	All		25	ns
End of ALE/$\overline{ADV}$ to $\overline{RD}$ or $\overline{WR}$ active	t_{LLRL}		9,10, 11	All	t_{OSC} -40		ns
Address hold after end of ALE/$\overline{ADV}$ 10/	t_{LLAX}		9,10, 11	All	t_{OSC} -40		ns
$\overline{WR}$ pulse width	t_{WLWH}		9,10, 11	All	$3t_{OSC}$ -35		ns
Output data valid to end of WR/WRL/WRH	t_{QVWH}		9,10, 11	All	$3t_{OSC}$ -60		ns
Output data hold after WR/WRL/WRH	t_{WHQX}		9,10, 11	All	t_{OSC} -50		ns
End of $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$ to ALE/$\overline{ADV}$ high	t_{WHLH}		9,10, 11	All	t_{OSC} -75		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = V_{PD} = 5\ V \pm 10\%$ $V_{SS} = ANGND = 0\ V$ $f_{OSC} = 6.0$ to 12 MHz unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{RD}$ pulse width	t_{RLRH}	See figure 5 f_{OSC} = 10 MHz	9,10, 11	All	$3t_{OSC}$ -30		ns
End of $\overline{RD}$ to ALE/$\overline{ADV}$ high	t_{RHLH}		9,10, 11	All	t_{OSC} -45		ns
CLOCKOUT low to ALE/$\overline{ADV}$ low	t_{CLLL}		9,10, 11	All	t_{OSC} -40	t_{OSC} +35	ns
$\overline{RD}$ high to INST, $\overline{BHE}$, AD8-15 inactive	t_{RHBX}		9,10, 11	All	t_{OSC} -25	t_{OSC} +30	ns
$\overline{WR}$ high to INST, $\overline{BHE}$, AD8-15 inactive	t_{WHBX}		9,10, 11	All	t_{OSC} -50	t_{OSC} +100	ns
$\overline{WRL}$, $\overline{WRH}$, low to $\overline{WRL}$, $\overline{WRH}$ high	t_{HLHH}		9,10, 11	All	$2t_{OSC}$ -35	$2t_{OSC}$ +40	ns
ALE/$\overline{ADV}$ low to $\overline{WRL}$, $\overline{WRH}$ low	t_{LLHL}		9,10, 11	All	$2t_{OSC}$ -30	$2t_{OSC}$ +55	ns
Output data valid to $\overline{WRL}$, $\overline{WRH}$ low	t_{QVHL}		9,10, 11	All	t_{OSC} -60		ns
Serial port clock period	t_{XLXL}	Serial port shift register See figure 5	9,10, 11	All	$8t_{OSC}$		ns
Serial port clock falling edge to rising edge	t_{XLXH}		9,10, 11	All	$4t_{OSC}$ -50	$4t_{OSC}$ +50	ns
Output data setup to clock rising edge	t_{QVXH}		9,10, 11	All	$3t_{OSC}$		ns
Output data hold after clock rising edge	t_{XHQX}		9,10, 11	All	$2t_{OSC}$ -70		ns
Next output data valid after clock rising edge	t_{XHQV}		9,10, 11	All		$2t_{OSC}$ +50	ns
Input data setup to clock rising edge	t_{DVXH}		9,10, 11	All	$2t_{OSC}$ +200		ns
Input data hold after clock rising edge	t_{XHDX}		9,10, 11	All	0		ns
Last clock rising to output float	t_{XHQZ}		9,10, 11	All		$5t_{OSC}$	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = V_{PD} = 5\ V \pm 10\%$ V_{SS} = ANGND = 0 V f_{OSC} = 6.0 to 12 MHz unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Oscillator frequency	$1/t_{OLOL}$	External clock drive See figure 5	9,10, 11	All	6	12	MHz
High time	t_{OHOX}		9,10, 11	All	25		ns
Low time	t_{OLOX}		9,10, 11	All	30		ns
Rise time	t_{OLOH}		9,10, 11	All		15	ns
Fall time	t_{OHOL}		9,10, 11	All		15	ns
Resolution		See figure 5 V_{REF} = 5.0 V ±10%	9,10, 11	All	1024	1024	level
					10	10	bits
Absolute error			9,10, 11	All	0	±4	LSBS
Non-linearity			9,10, 11	All	0	±4	LSBS
Differential non-linearity			9,10, 11	All	0	±2	LSBS
Channel to channel matching			9,10, 11	All	0	±1	LSBS
Off isolation 11/ 12/ 13/		See figure 5	9,10, 11	All	-60		dB

See footnotes on next sheet.

TABLE I. Electrical performance characteristics - Continued.

1/ Case temperatures are instant on.

2/ $V_{REF} = V_{EA} = 5\ V \pm 10\%$.

3/ Quasi-bidirectional pins include those on Port 1, for P2.6 and P2.7. Standard output pins include TXD, RXD (mode 0 only), PWM and HSO pins. Bus/control pins include CLKOUT, ALE, $\overline{BHE}$, $\overline{RD}$ $\overline{WR}$, INST, AND ADD-15.

4/ Maximum current per pin must be externally limited to the following value if V_{OL} is held above 0.45 V:
I_{OL} on quasi-bidirectional pins and Ports 3 and 4 when used as ports: 4.0 mA.
I_{OL} on standard output pins and $\overline{RESET}$: 8.0 mA.
I_{OL} on Bus/control pins: 2.0 mA.

5/ During normal (nontransient) operation, the following limits apply:
Total I_{OL} on Port 1 must not exceed 8.0 mA.
Total I_{OL} on P2.0, P2.6, $\overline{RESET}$ and all HSO pins must not exceed 15 mA.
Total I_{OL} on Port 3 must not exceed 10 mA.
Total I_{OL} on P2.5, P2.7, and Port 4 must not exceed 20 mA.

6/ I_{OL} on HSO.X (X = 0, 4, 5) = 1.6 mA at 0.5 V.

7/ The term "Address Valid" applies to AD0-15, $\overline{BHE}$, and INST.

8/ CLKOUT is directly generated as a divide-by-three of the oscillator. The period will be $3t_{OSC} \pm 10ns$ if t_{OSC} is constant and the rise and fall times on XTAL1 are less than 10 ns.

9/ Maximum specification applies only to ALE. Minimum specification applies to both ALE and $\overline{ADV}$.

10/ The term "Address" in this definition applies to AD0-7 for 8-bit cycles, and AD0-15 for 16-bit cycles.

11/ These values are not tested in production and are based on theoretical estimates and laboratory tests.

12/ DC to 100 kHz.

13/ Multiplexer break-before-make guaranteed.

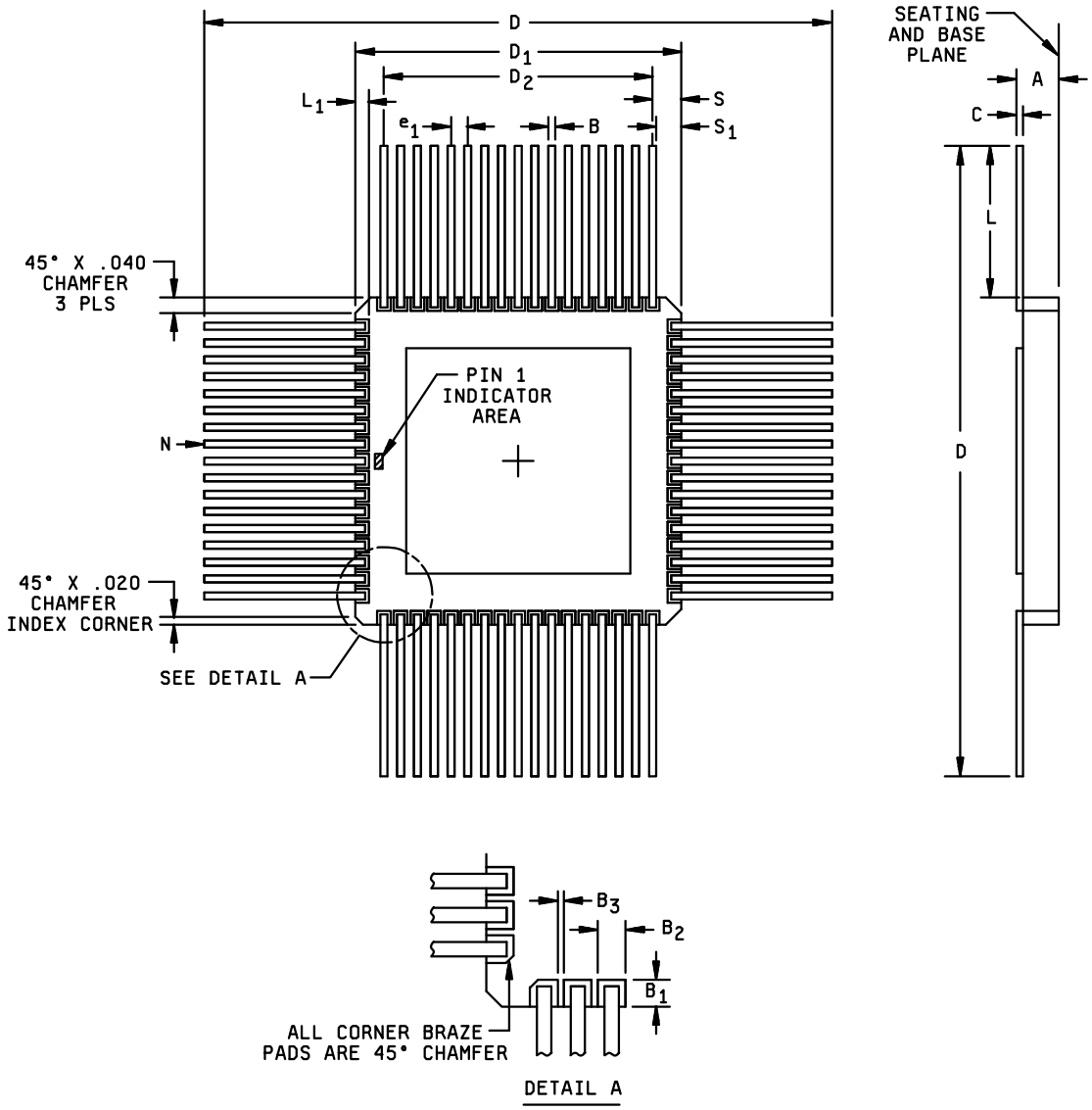


FIGURE 1. Case outline Y.

Dimensions				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.80	.106	2.03	2.69
B	.016	.020	0.41	0.51
B_1 (see note)	.040	.060	1.02	1.52
B_2 (see note)	.030	.040	0.76	1.02
B_3 (see note)	.005	.020	0.13	0.51
C	.008	.012	0.20	0.31
D	1.640	1.870	41.66	47.50
D_1	.935	.970	23.75	24.64
D_2	.800 BSC		20.32 BSC	
e_1	.050 BSC		1.27 BSC	
L	.375	.450	9.52	11.43
L_1	.040	.060	1.02	1.52
N	68		68	
S	.066	.087	1.68	2.21
S_1	.050	---	1.27	---

Note: These are typical values.

FIGURE 1. Case outline Y - Continued.

Device type	01		
Case outline	Y		
Pin number	Pin symbol	Pin number	Pin symbol
1	$\underline{V_{CC}}$	35	HSO.3
2	$\overline{EA}$	36	V_{SS}
3	NMI	37	V_{PP}
4	ACH3/P0.3	38	P2.7
5	ACH1/P0.1	39	$\underline{PWM}$/P2.5
6	ACH0/P0.0	40	$\underline{WR}/\underline{WRL}$
7	ACH2/P0.2	41	$\overline{BHE}$/WRH
8	ACH6/P0.6	42	T2RST/P2.4
9	ACH7/P0.7	43	READY
10	ACH5/P0.5	44	T2CLK/P2.3
11	ACH4/P0.4	45	AD15/P4.7
12	ANGND	46	AD14/P4.6
13	V_{REF}	47	AD13/P4.5
14	V_{PD}	48	AD12/P4.4
15	EX$\underline{TINT}$/P2.2	49	AD11/P4.3
16	$\overline{RESET}$	50	AD10/P4.2
17	RXD/P2.1	51	AD9/P4.1
18	TXD/P2.0	52	AD8/P4.0
19	P1.0	53	AD7/P3.7
20	P1.1	54	AD6/P3.6
21	P1.2	55	AD5/P3.5
22	P1.3	56	AD4/P3.4
23	P1.4	57	AD3/P3.3
24	HSI.0	58	AD2/P3.2
25	HSI.1	59	AD1/P3.1
26	HSO.4/HIS.2	60	AD0/P3.0
27	HSO.5/HIS.3	61	$\overline{RD}$
28	HSO.0	62	ALE/$\overline{ADV}$
29	HSO.1	63	INST
30	P1.5	64	BUSWIDTH
31	P1.6	65	CLKOUT
32	P1.7	66	XTAL2
33	P2.6	67	XTAL1
34	HSO.2	68	V_{SS}

FIGURE 2. Terminal connections.

Device type	01		
Case outline	Z		
Pin number	Pin symbol	Pin number	Pin symbol
1	ACH7/P0.7	35	READY
2	ACH6/P0.6	36	T2RST/P2.4
3	ACH2/P0.2	37	$\overline{BHE}$
4	ACH0/P0.0	38	$\overline{WR}$
5	ACH1/P0.1	39	PWM/P2.5
6	ACH3/P0.3	40	P2.7
7	$\overline{NMI}$	41	V_{PP}
8	$\overline{EA}$	42	V_{SS}
9	V_{CC}	43	HSO.3
10	V_{SS}	44	HSO.2
11	XTAL1	45	P2.6
12	XTAL2	46	P1.7
13	CLKOUT	47	P1.6
14	BUSWIDTH	48	P1.5
15	$\overline{INST}$	49	HSO.1
16	ALE/$\overline{ADV}$	50	HSO.0
17	$\overline{RD}$	51	HSO.5/HSI.3
18	AD0/P3.0	52	HSO.4/HSI.2
19	AD1/P3.1	53	HSI.1
20	AD2/P3.2	54	HSI.0
21	AD3/P3.3	55	P1.4
22	AD4/P3.4	56	P1.3
23	AD5/P3.5	57	P1.2
24	AD6/P3.6	58	P1.1
25	AD7/P3.7	59	P1.0
26	AD8/P4.0	60	TXD/P2.0
27	AD9/P4.1	61	RXD/P2.1
28	AD10/P4.2	62	$\overline{RESET}$
29	AD11/P4.3	63	EXTINT/P2.2
30	AD12/P4.4	64	V_{PD}
31	AD13/P4.5	65	V_{REF}
32	AD14/P4.6	66	ANGND
33	AD15/P4.7	67	ACH4/P0.4
34	T2CLK/P2.3	68	ACH5/P0.5

FIGURE 2. Terminal connections - Continued

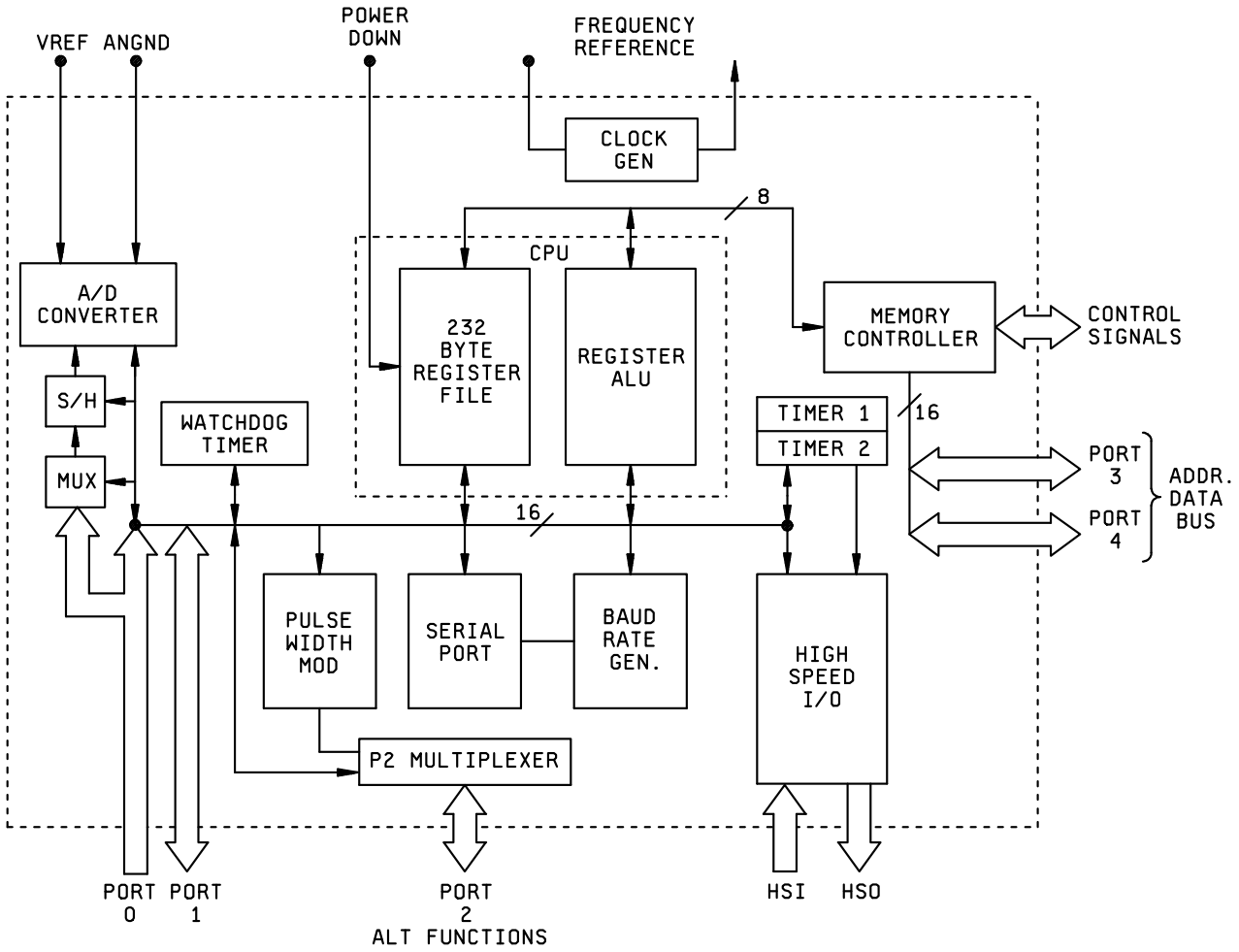


FIGURE 3. Functional block diagram.

Mnemonic	Oper-ands	Operation (note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
ADD/ADDB	2	D ← D + A	√	√	√	√	↑	---	
ADD/ADDB	3	D ← B + A	√	√	√	√	↑	---	
ADDC/ADDCB	2	D ← D + A + C	↓	√	√	√	↑	---	
SUB/SUBB	2	D ← D – A	√	√	√	√	↑	---	
SUB/SUBB	3	D ← B – A	√	√	√	√	↑	---	
SUBC/SUBCB	2	D ← D - A + C – 1	↓	√	√	√	↑	---	
CMP/CMPB	2	D – A	√	√	√	√	↑	---	
MUL/MULU	2	D, D + 2 ← D*A	---	---	---	---	---	?	2
MUL/MULU	3	D, D + 2 ← B*A	---	---	---	---	---	?	2
MULB/MULUB	2	D, D + 1 ← D*A	---	---	---	---	---	?	3
MULB/MULUB	3	D, D + 1 ← B*A	---	---	---	---	---	?	3
DIVU	2	D ← (D, D + 2)/A, D + 2 ← remainder	---	---	---	√	↑	---	2
DIVUB	2	D ← (D, D + 1)/A, D + 1 ← remainder	---	---	---	√	↑	---	3
DIV	2	D ← (D, D + 2)/A, D + 2 ← remainder	---	---	---	?	↑	---	
DIVB	2	D ← (D, D + 1)/A, D + 1 ← remainder	---	---	---	?	↑	---	
AND/ANDB	2	D ← D and A	√	√	0	0	---	---	
AND/ANDB	3	D ← B and A	√	√	0	0	---	---	
OR/ORB	2	D ← D or A	√	√	0	0	---	---	
XOR/XORB	2	D ← D (excl. or) A	√	√	0	0	---	---	
LD/LDB	2	D ← A	---	---	---	---	---	---	
ST/STB	2	A ← D	---	---	---	---	---	---	
LDBSE	2	D ← A; D + 1 ← Sign(A)	---	---	---	---	---	---	3,4
LDBZE	2	D ← A; D + 1 ← 0	---	---	---	---	---	---	3,4

FIGURE 4. Instruction set summary.

Mnemonic	Oper-ands	Operation (note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
PUSH	1	SP ← SP - 2; (SP) ← A	---	---	---	---	---	---	
POP	1	A ← (SP); SP ← SP + 2	---	---	---	---	---	---	
PUSHF	0	SP ← SP - 2; (SP) ← PSW; PSW ← 0000H I ← 0	0	0	0	0	0	0	
POPF	0	PSW ← (SP); SP ← SP + 2; I ← √	√	√	√	√	√	√	
SJMP	1	PC ← PC + 11-bit offset	---	---	---	---	---	---	5
LJMP	1	PC ← PC + 16-bit offset	---	---	---	---	---	---	5
BR (indirect)	1	PC ← (A)	---	---	---	---	---	---	
SCALL	1	SP ← SP - 2; (SP) ← PC; PC ← PC + 11-bit offset	---	---	---	---	---	---	5
LCALL	1	SP ← SP - 2; (SP) ← PC; PC ← PC + 16-bit offset	---	---	---	---	---	---	5
RET	0	PC ← (SP); SP ← SP + 2	---	---	---	---	---	---	
J (conditional)	1	PC ← PC + 8-bit offset (if taken)	---	---	---	---	---	---	5
JC	1	Jump if C = 1	---	---	---	---	---	---	5
JNC	1	Jump if C = 0	---	---	---	---	---	---	5
JE	1	Jump if Z = 1	---	---	---	---	---	---	5
JNE	1	Jump if Z = 0	---	---	---	---	---	---	5
JGE	1	Jump if N = 0	---	---	---	---	---	---	5
JLT	1	Jump if N = 1	---	---	---	---	---	---	5
JGT	1	Jump if N = 0 and Z = 0	---	---	---	---	---	---	5
JLE	1	Jump if N = 1 and Z = 1	---	---	---	---	---	---	5
JH	1	Jump if C = 1 and Z = 0	---	---	---	---	---	---	5
JNH	1	Jump if C = 0 and Z = 1	---	---	---	---	---	---	5
JV	1	Jump if V = 1	---	---	---	---	---	---	5

FIGURE 4. Instruction set summary - Continued.

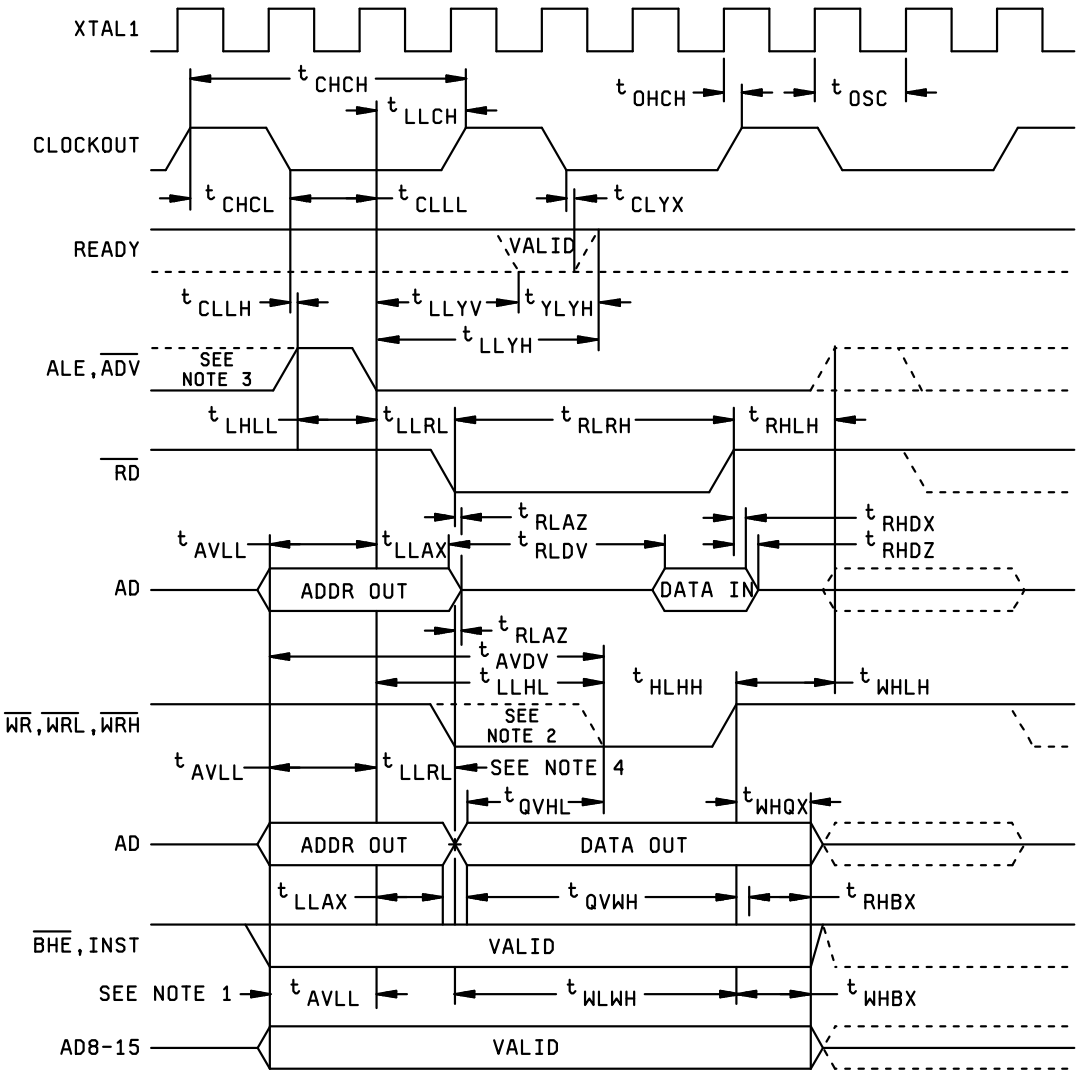
Mnemonic	Oper-ands	Operation (note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
JNV	1	Jump if V = 0	---	---	---	---	---	---	5
JVT	1	Jump if VT = 1; Clear VT	---	---	---	---	0	---	5
JNVT	1	Jump if VT = 0; Clear VT	---	---	---	---	0	---	5
JST	1	Jump if ST = 1	---	---	---	---	---	---	5
JNST	1	Jump if ST = 0	---	---	---	---	---	---	5
JBS	3	Jump if specified bit = 1	---	---	---	---	---	---	5,6
JBC	3	Jump if specified bit = 0	---	---	---	---	---	---	5,6
DJNZ	1	D ← D - 1; if D ≠ 0 then PC ← PD + 8-bit offset	---	---	---	---	---	---	5
DEC/DECB	1	D ← D – 1	√	√	√	√	↑	---	
NEG/NEGB	1	D ← 0 – D	√	√	√	√	↑	---	
INC/INCB	1	D ← D + 1	√	√	√	√	↑	---	
EXT	1	D ← D; D + 2 ← Sign (D)	√	√	0	0	---	---	2
EXTB	1	D ← D; D + 1 ← Sign (D)	√	√	0	0	---	---	3
NOT/NOTB	1	D ← Logical not (D)	√	√	0	0	---	---	
CLR/CLRB	1	D ← 0	1	0	0	0	---	---	
SHL/SHLB/SHLL	2	C ← msb ----- 1sb ← 0	√	?	√	√	↑	---	7
SHR/SHRB/SHRL	2	0 ⌠ msb ----- 1sb ⌠ C	√	?	√	0	---	√	7
SHRA/SHRAB/SHRAL	2	msb ⌠ msb ----- 1sb ⌠ C	√	√	√	0	---	√	7
SETC	0	C ← 1	---	---	1	---	---	---	
CLRC	0	C ← 0	---	---	0	---	---	---	
CLRVT	0	VT ← 0	---	---	---	---	0	---	
RST	0	PC ← 2080H	0	0	0	0	0	0	8
DI	0	Disable all interrupts (I ← 0)	---	---	---	---	---	---	
EI	0	Disable all interrupts (I ← 1)	---	---	---	---	---	---	

FIGURE 4. Instruction set summary - Continued.

Mnemonic	Oper-ands	Operation (note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
NOP	0	PC ← PC + 1	---	---	---	---	---	---	
SKIP	0	PC ← PC + 2	---	---	---	---	---	---	
NORML	2	Left shift until msb = 1; D ← shift count	√	?	0	---	---	---	7
TRAP	0	SP ← SP - 2; (SP) ← PC PC ← (2010H)	---	---	---	---	---	---	9

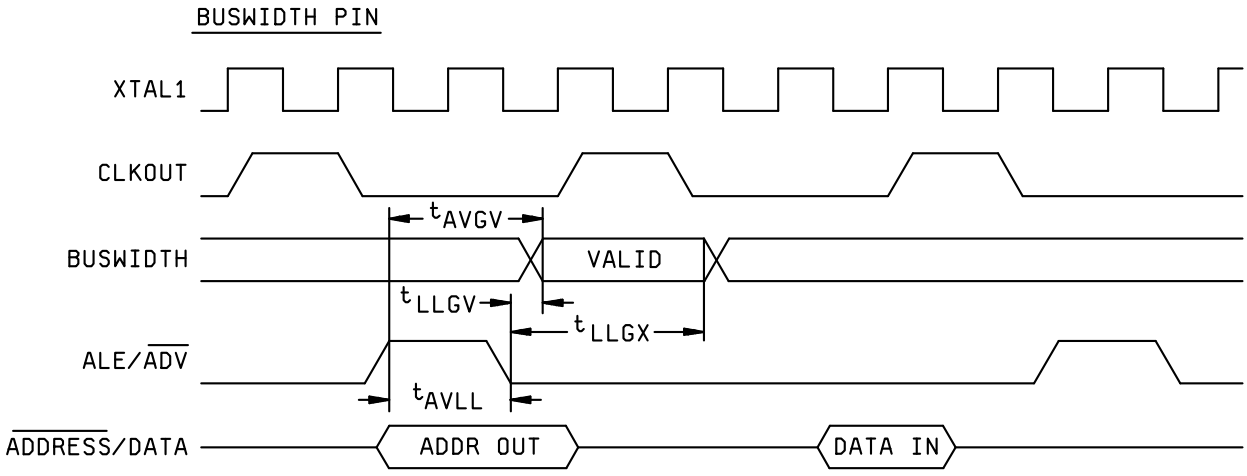
NOTES:
1. If the mnemonic ends in "B", a byte operation is performed, otherwise a word operation is done. Operands D, B, and A must conform to the alignment rules for the required operand type. D and B are locations in the register file; A can be located anywhere in memory.
2. D, D + 2 are consecutive WORDS in memory; D is DOUBLE-WORD aligned.
3. D, D + 1 are consecutive BYTES in memory; D is WORD aligned.
4. Changes a byte to a word.
5. Offset is a 2's complement number.
6. Specified bit is one of the 2048 bits in the register file.
7. The "L" (long) suffix indicates double-word operation.
8. Initiates a reset by pulling RESET low. Software should reinitialize all the necessary registers with code starting at 2080H.
9. The assembler will not accept the mnemonic.

FIGURE 4. Instruction set summary - Continued.



NOTES:
1. 8-bit bus only.
2. 8-bit bus; or when write strobe mode selected.
3. When $\overline{\text{ADV}}$ selected.
4. 8 or 16-bit bus and write strobe mode not selected.

FIGURE 5. Switching test circuit and waveforms.



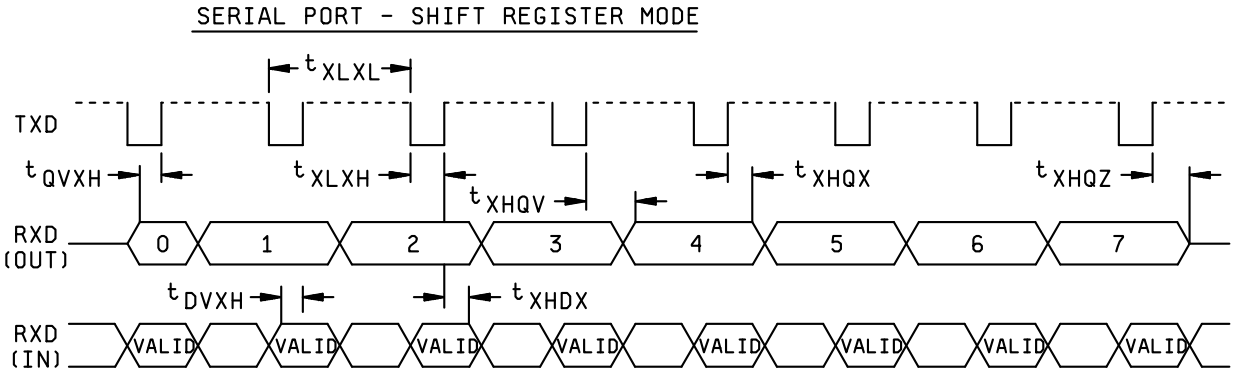
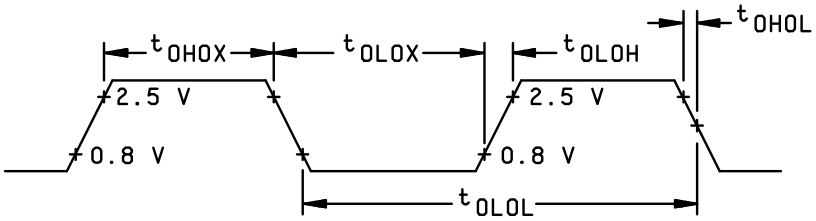
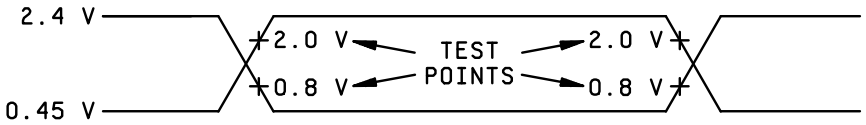


FIGURE 5. Switching test circuit and waveforms - Continued.

EXTERNAL CLOCK DRIVE WAVEFORM

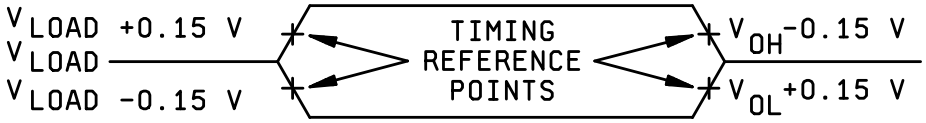


AC TESTING INPUT/OUTPUT WAVEFORM



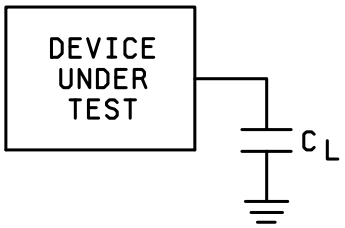
AC testing inputs are driven at 2.4 V for a logic “1” and 0.45 V for a logic “0”.
Timing measurements are made at 2.0 V for a logic “1” and 0.8 V for a logic “0”.

FLOAT WAVEFORM



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

OUTPUT LOAD CIRCUIT



C_L = 80 pF unless otherwise specified.

FIGURE 5. Switching test circuit and waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8 , 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8A, 10 or 1, 2, 3

1/ PDA applies to subgroups 1 and 7.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_S measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero failures shall be required.

d. Subgroups 7 and 8 shall include verification of the programming set. See figure 4.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Symbols, definitions and functional descriptions. The symbols, definitions, and functional descriptions for this device shall be as shown in table III.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Terminal descriptions.

Symbol	Name and function
V_{CC}	Main supply voltage (5 V).
V_{SS}	Digital circuit ground (0 V). There are two VSS pins, both of which must be connected.
V_{PD}	RAM standby supply voltage (5 V). This voltage must be present during normal operation. In a power down condition (i.e., V_{CC} drops to zero), if $\overline{\text{RESET}}$ is activated before V_{CC} drops below specification and V_{PD} continues to be held with specification, the top 16 bytes in the register file will retain their contents. $\overline{\text{RESET}}$ must be held low during the power down and should not be brought high until V_{CC} is within specification and the oscillator has stabilized.
V_{REF}	Reference voltage to the A/D converter (5 V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0.
ANGND	Reference ground for the A/D converter. Must be held at normally the same potential as V_{SS}.
V_{PP}	Used as the programming voltage for EPROM parts only. This pin has no function for the 8097BH device.
XTAL1	Input of the oscillator inverter and of the terminal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is one-third the oscillator frequency. It has a 33 percent duty cycle.
$\overline{\text{RESET}}$	Reset input to the chip, input low for at least two state times to reset the chip. The subsequent low-to-high transition resynchronizes CLKOUT and commences a 10-state-time sequence in which the PSW is cleared, a byte read from 2018H loads CCR, and a jump to location 2080H is executed. Input high for normal operation. RESET has an internal pullup.
BUSWIDTH	Input for bus width selection. If CCR bit one is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a zero an 8-bit cycle occurs. If CCR bit one is a zero, the bus is always an 8-bit bus. If this pin is left unconnected, it will rise to V_{CC}.
NMI	A positive transition causes a vector to external memory location 0000H. External memory form 00H through 0FFH is reserved for development systems.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle.
$\overline{\text{EA}}$	Input for memory select (external access). $\overline{\text{EA}}$ is tied to a TTL-low causing accesses to locations 2000H through 3FFFH to be directed to off-chip memory.
ALE/$\overline{\text{ADV}}$	Address latch enable or Address valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus cycle. ADV can be used as a chip select for external memory. ALE/ADV is activated only during external memory access.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while WRL will go low only for external writes where an even byte is being written. WR/WRL is activated only during external memory writes.

TABLE III. Terminal descriptions – Continued.

Symbol	Name and function
$\overline{BHE}$/$\overline{WRH}$	Bus high enable or Write high output to external memory, as selected by the CCR. $\overline{BHE}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects the bank of memory that is connected to the low byte of the data bus. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, BHE = 0). If the WRH function is selected, the pin will go low if the bus cycle is writing to an old memory location. BHE/WRH is activated only during external memory writes.
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition in CLKOUT occurs with READY high. The bus cycle can be lengthened by up to 1 μs. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle held not ready, is available through configuration of CCR. READY has a weak internal pullup, so it goes to one unless externally pulled low.
HIS	Inputs to high speed input unit. Four HSI pins are available: HSI.0, HSI.1, HIS.2, HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO unit.
HSO	Outputs from high speed output unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4, and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI unit.
Port 0	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port.
Port 2	8-bit multifunctional port. Six of its pins are shared with other functions, the remaining two pins are quasi-bidirectional.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 09-05-05

Approved sources of supply for SMD 5962-89596 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/ .

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8959601YA	3V146	MQ8097BH/BYA
5962-8959601YC	3V146	MQ8097BH/BYC
5962-8959601ZA	3V146	MG8097BH/BZA
5962-8959601ZC	3V146	MG8097BH/BZC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics, Inc. 16 Malcolm Hoyt Drive Newburyport, MA 01950