REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to MIL-PRF-38535 requirements. - CFS	05-11-23	Thomas M. Hess
B	To correct input capacitance (C_{IN}) and output capacitance (C_{OUT}) value in table I. Update boilerplate paragraphs to current requirements of MIL-PRF-38535. - MAA	10-05-07	Thomas M. Hess

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	B																			
SHEET	15																			
REV STATUS				REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
OF SHEETS				SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

PREPARED BY
Wanda G. Meadows

CHECKED BY
Thomas M. Hess

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
92-08-18

REVISION LEVEL
B

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, DIGITAL, CMOS, REAL TIME CLOCK, MONOLITHIC SILICON

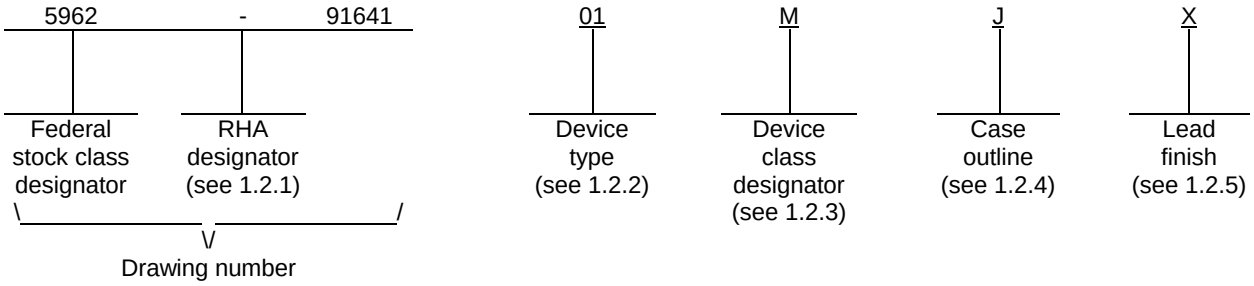
SIZE	CAGE CODE	
A	**67268**	**5962-91641**

SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	8572	Real time clock

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC})	-0.5 V to +7.0 V
DC input voltage range (V_{IN})	-0.5 V to V_{CC} + 0.5 V
DC output voltage range (V_{OUT})	-0.5 V to V_{CC} + 0.5 V
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Junction temperature (T_J)	+150°C
Power dissipation (P_D)	500 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):	
Board mount	46°C/W
Socket mount	52°C/W

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) 2/	4.5 V dc to 5.5 V dc
Supply voltage (V_{BB}) (Battery-backed mode) 2/	2.2 V to V_{CC} – 0.4 V
DC input or output voltage (V_{IN}, V_{OUT})	0.0 V to V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C
Address hold after read (t_{RAH})	3 ns (minimum)
Address hold after write strobe (t_{WAH})	3 ns (minimum)
Data hold after write strobe (t_{WDH})	3 ns (minimum)

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ For F_{OSC} = 4.194304 or 4.9152 MHz, V_{BB} minimum = 2.8 V. In battery-backed mode, $V_{BB} \leq V_{CC} - 0.4$ V. Single supply mode: Data retention voltage is 2.2 V minimum. In single supply mode (power connected to V_{CC} pin) 4.5 V $\leq V_{CC} \leq$ 5.5 V.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ $V_{\overline{PFAIL}} > V_{IH}$ $V_{BB} = 3\ V$, $C_L = 100\ pF$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input high voltage	V_{IH}	All inputs except OSC IN	1, 2, 3	All	2		V
		OSC IN with external clock			$V_{BB} - 0.1$		
Input low voltage	V_{IL}	All inputs except OSC IN				0.8	V
		OSC IN with external clock				0.1	
Output high voltage (excluding OSC OUT)	V_{OH}	$I_{OH} = -20\ \mu A$, $V_{CC} = 4.5\ V$			$V_{CC} - 0.1$		V
		$I_{OH} = -4\ mA$, $V_{CC} = 4.5\ V$			3.5		
Output low voltage (excluding OSC OUT)	V_{OL}	$I_{OL} = 20\ \mu A$, $V_{CC} = 4.5\ V$				0.1	V
		$I_{OL} = 4\ mA$, $V_{CC} = 4.5\ V$				0.25	
Input leakage current (except OSC IN)	I_I	$V_{IN} = V_{CC}$, $V_{CC} = 5.5\ V$				1	µA
		$V_{IN} = 0\ V$, $V_{CC} = 5.5\ V$				-1	
3-state leakage current	I_{OZ}	$V_{OUT} = V_{CC}$, $V_{CC} = 5.5\ V$				5	µA
		$V_{OUT} = 0\ V$, $V_{CC} = 5.5\ V$				-5	
Output high leakage current, INTR pin	I_{LKG}	$V_{OUT} = V_{CC}$, $V_{CC} = 5.5\ V$, output open drain				15	µA
		$V_{OUT} = 0\ V$, $V_{CC} = 5.5\ V$, output open drain				-15	
Quiescent current	I_{CC}	$F_{OSC} = 32.768\ KHz$, $V_{CC} = 5.5\ V$ $V_{IN} = V_{CC}$ or GND 2/ 3/				275	µA
		$F_{OSC} = 32.768\ KHz$, $V_{CC} = 5.5\ V$ $V_{IN} = V_{CC}$ or GND 2/ 4/				1	mA
		$F_{OSC} = 32.768\ KHz$, $V_{CC} = 5.5\ V$ $V_{IN} = V_{IH}$ or V_{IL} 2/ 4/				12	mA
		$F_{OSC} = 4.9152\ MHz$ or 4.194304 MHz $V_{CC} = 5.5\ V$ $V_{IN} = V_{CC}$ or GND 2/ 4/				8	mA
		$F_{OSC} = 4.9152\ MHz$ or 4.194304 MHz $V_{CC} = 5.5\ V$ $V_{IN} = V_{IH}$ or V_{IL} 2/ 4/				20	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ $V_{\overline{PFAIL}} > V_{IH}$ $V_{BB} = 3\ V$, $C_L = 100\ pF$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Quiescent supply current (single supply mode)	I_{CC}	$V_{CC} = 5.5\ V$, $V_{BB} = GND$, $V_{IN} = V_{CC}$ or GND, $F_{OSC} = 32.768\ KHz$ 2/	1, 2, 3	All		40	µA
		$V_{CC} = 5.5\ V$, $V_{BB} = GND$, $V_{IN} = V_{CC}$ or GND, $F_{OSC} = 4.9152\ MHz$ or $4.194304\ MHz$ 2/				7.5	mA
Standby mode battery supply current 2/	I_{BB}	$V_{CC} = 0\ V$, $F_{OSC} = 32.768\ KHz$				10	µA
		$V_{CC} = 0\ V$, $F_{OSC} = 4.9152\ MHz$				400	
Battery supply leakage current	I_{BLK}	$V_{CC} = 5.5\ V$,	1		-5	1.5	µA
		$2.2\ V < V_{BB} < 4.0\ V$	2, 3		-5	3.5	
Input capacitance	C_{IN}	See 4.4.1c $F = 1\ MHz$	4			8	pF
Output capacitance	C_{OUT}					9	pF
Functional testing		See 4.4.1b $V_{CC} = 4.5\ V$, $5.5\ V$	7, 8				
Address valid prior to read strobe	t_{AR}	See figure 3. $V_{\overline{PFAIL}} = 3\ V$	9, 10, 11		20		ns
Read strobe width	t_{RW}	See figure 3. $V_{\overline{PFAIL}} = 3\ V$ 5/			80		ns
Chip select to data valid time	t_{CD}	See figure 3. $V_{\overline{PFAIL}} = 3\ V$				80	ns
Read strobe to data valid time	t_{RD}					70	ns
Read or chip select to tri-state	t_{DZ}					60	ns
Chip select hold after read strobe	t_{RCH}				0		ns
Minimum inactive time between read or write accesses	t_{DS}				50		ns
Address valid before write strobe	t_{AW}				20		ns
Chip select to end of write strobe	t_{CW}				90		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ $V_{\overline{PFAIL}} > V_{IH}$ $V_{BB} = 3\ V$, $C_L = 100\ pF$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write strobe width	t_{WW}	See figure 3. $V_{\overline{PFAIL}} = 3\ V$ 6/	9, 10, 11	All	80		ns
Data valid to end of write strobe	t_{DW}	See figure 3. $V_{\overline{PFAIL}} = 3\ V$			50		ns
Chip select hold after write strobe	t_{WCH}				0		ns

1/ Unless otherwise specified, all testing shall be conducted under worst-case conditions.

2/ OSC IN driven by a signal generator. Contents of test register = 00H and MFO pin not configured as buffered oscillator output.

3/ I_{CC} tested with all power fail circuitry disabled, by setting D7 of interrupt control register 1 to 0.

4/ I_{CC} tested with all power fail circuitry enabled, by setting D7 of interrupt control register 1 to 1.

5/ Read Strobe width as used in the read timing table is defined as the period when both chip select and read inputs are low. Hence read commences when both signals are low and terminates when either signal returns high.

6/ Write Strobe width as used in the write timing table is defined as the period when both chip select and write inputs are low. Hence write commences when both signals are low and terminates when either signal returns high.

Device type:	All		
Case outline:	J		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{CS}$	13	MFO
2	$\overline{RD}$	14	INTR
3	$\overline{WR}$	15	D0
4	A0	16	D1
5	A1	17	D2
6	A2	18	D3
7	A3	19	D4
8	A4	20	D5
9	V_{BB}	21	D6
10	OSC IN	22	D7
11	OSC OUT	23	$\overline{PFAIL}$
12	GND	24	V_{CC}

FIGURE 1. Terminal connections.

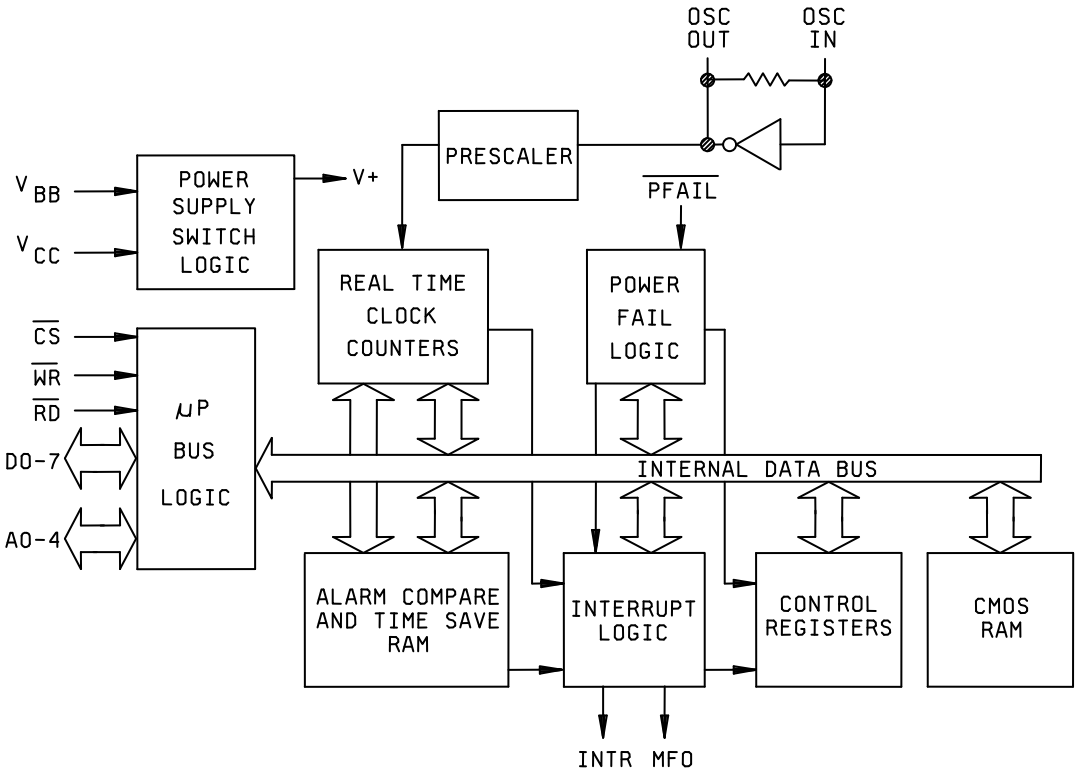


FIGURE 2. Block diagram.

READ TIMING DIAGRAM

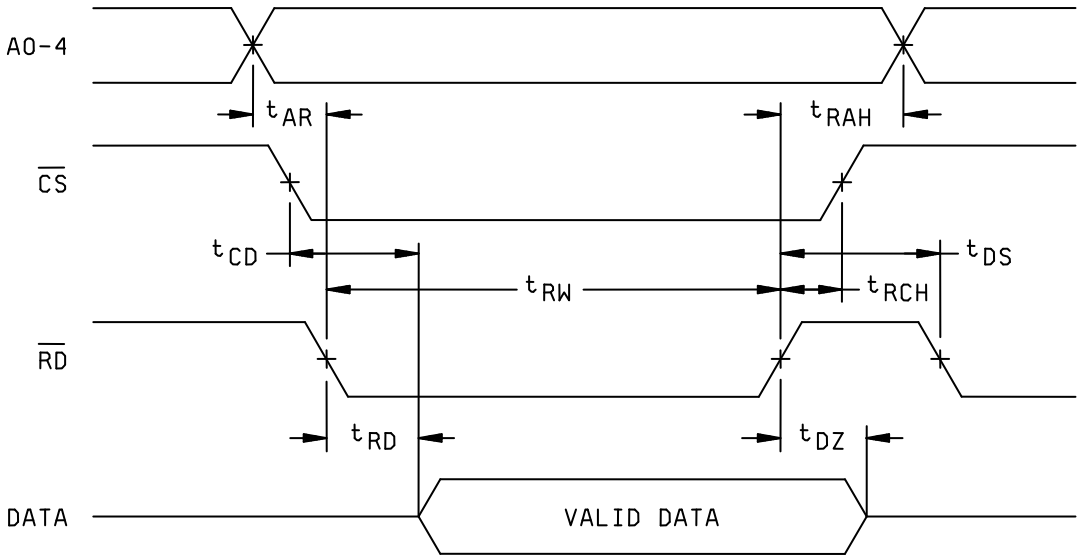
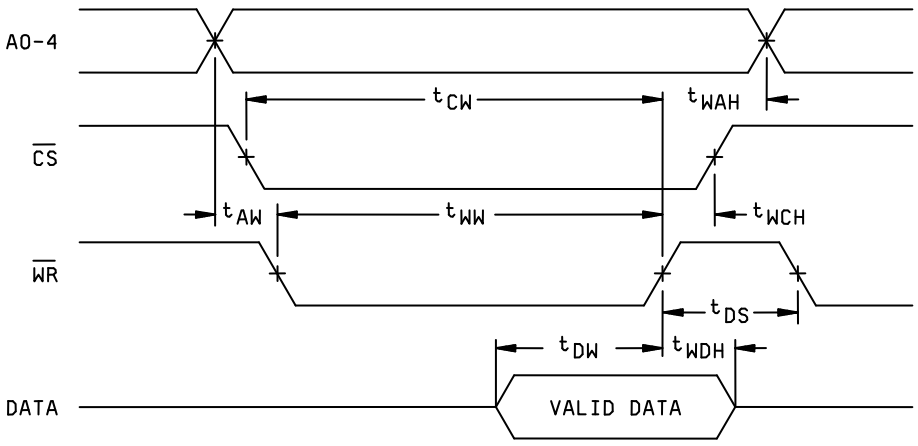
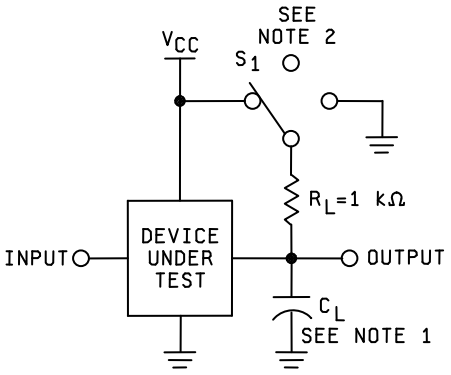


FIGURE 3. Switching waveforms and test circuit.

WRITE TIMING DIAGRAM





AC TEST CONDITIONS	
INPUT PULSE LEVELS	GND TO 3.0 V dc
INPUT RISE AND FALL TIMES	6 ns (10% TO 90%)
INPUT AND OUTPUT REFERNECE LEVELS	1.3 V dc
TRI-STATE REFERENCE LEVELS SEE NOTE 2	ACTIVE HIGH +0.5 V
	ACTIVE LOW -0.5 V

NOTES:
1. C_L = 100 pF, includes jig and scope capacitance.
2. S_1 = V_{CC} for active low to high impedance measurements.
   S_1 = GND for active high to high impedance measurements.
   S_1 = Open for all other timing measurements.

FIGURE 3. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and in table III herein.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Pin descriptions.

Symbol	Name and function
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$ (inputs)	These pins interface to microprocessor control lines. The CS pin is an active low enable for the read and write operations. Read and write pins are also active low and enable reading or writing to the device. All three pins are disabled when power failure is detected. However, if a read or write is in progress at this time, it will be allowed to complete its cycle.
A0 - A4 (inputs)	These five pins are for register selection. They individually control which location is to be accessed. These inputs are disabled when power failure is detected.
OSC IN (input), OSC OUT (output)	These two pins are used to connect the crystal to the internal parallel resonant oscillator. The oscillator is always running when power is applied to V_{BB} and V_{CC}, and the correct crystal select bits in the Real Time Mode Register have been set.
MFO (output)	The multi-function output can be used as a second interrupt output for interrupting the microprocessor. This pin can also provide an output for the oscillator. The MFO is configured as push-pull, active high for normal or single power supply operation and as an open drain during standby mode. If in battery-backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.
INTR (output)	The interrupt output is used to interrupt the processor when a timing event or power fail has occurred and the respective interrupt has been enabled. The INTR output is permanently configured active low, open drain. If in battery-backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.
D0 – D7 (input/output)	These eight bidirectional pins connect to the host microprocessor's data bus and are used to read from and write to the device. When the PFAIL pin goes low and a write is not in progress, these pins are at tri-state.
$\overline{PFAIL}$	In battery-backed mode, this pin can have a digital signal applied to it via some external power detection logic. When $\overline{PFAIL}$ = logic 0 the device goes into a lockout mode, in a minimum of 30 microseconds or a maximum of 63 microseconds unless lockout delay is programmed. In the single power supply mode, this pin is not usable as an input and should be tied to V_{CC}.
V_{BB} (battery power pin)	This pin is connected to a back-up power supply. The power supply is switched to the internal circuitry when V_{CC} becomes lower than V_{BB}. Utilizing this pin eliminates the need for external logic to switch in and out the back-up power supply. If this feature is not to be used then this pin must be tied to ground, the device programmed for single power supply only, and power applied to the V_{CC} pin.
V_{CC}, GND	V_{CC} is the main system power pin. GND is the common ground pin for V_{BB} and V_{CC}.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-05-07

Approved sources of supply for SMD 5962-91641 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9164101MJA	3V146	DP8572AMD/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics Inc. 16 Malcolm Hoyt Drive Newburyport, MA 01950