# 100182

## *9-Bit Wallace Tree Adder*

The 100182 is a 9-bit Wallace tree adder. It is designed to assist in performing high-speed hardware multiplication. The device is designed to add 9 bits of data 1-bit-slice wide and handle the carry-ins from the previous slices. The 100182 is easily expanded and still maintains four levels of delay regardless of input string length. In conjunction with the 100183 Recode Multiplier, the 100179 Carry Lookahead, and the 100180 High-speed Adder, the 100182 assists in performing parallel multiplication of two signed numbers to produce a signed twos complement product. All inputs have 50 kΩ pull-down resistors.

## Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

## Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

**National** Semiconductor

## 100182
# 9-Bit Wallace Tree Adder

## General Description

The 100182 is a 9-bit Wallace tree adder. It is designed to assist in performing high-speed hardware multiplication. The device is designed to add 9 bits of data 1-bit-slice wide and handle the carry-ins from the previous slices. The 100182 is easily expanded and still maintains four levels of delay regardless of input string length. In conjunction with the 100183 Recode Multiplier, the 100179 Carry Lookahead, and the 100180 High-speed Adder, the 100182 assists in performing parallel multiplication of two signed numbers to produce a signed twos complement product. See 100183 data sheet for additional information. All inputs have 50 kΩ pull-down resistors.
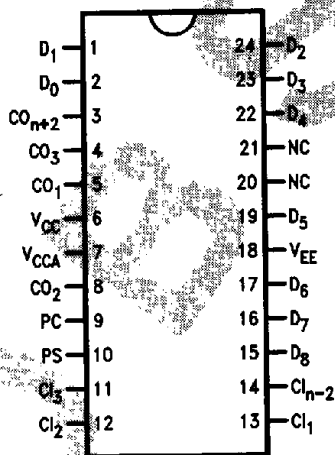
## Ordering Code: See Section 6

## Logic Symbol
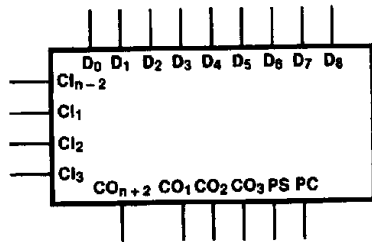


| Pin Names | Description |
|---|---|
| $D_0-D_8$ | Data Inputs |
| $CI_1-CI_3$, $CI_{n-2}$ | Carry Inputs |
| $CO_1-CO_3$, $CO_{n+2}$ | Carry Outputs |
| PS | Partial Sum Output |
| PC | Partial Carry Output |

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## Connection Diagrams

### 24-Pin DIP



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### 24-Pin Quad Cerpak



TL/F/9874-2

## Logic Diagram



DATA INPUTS

$D_0$ $D_4$ $D_6$    $D_1$ $D_2$ $D_3$    $D_5$ $D_7$ $D_8$

CARRY OUTPUTS

$CO_1$
$CO_{n+2}$
$CO_2$
$CO_3$

CARRY INPUTS

$CI_1$
$CI_{n-2}$
$CI_2$
$CI_3$
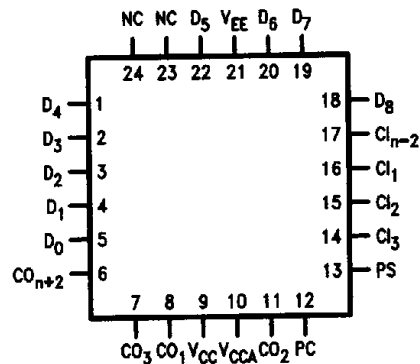
PC PARTIAL CARRY    PS PARTIAL SUM
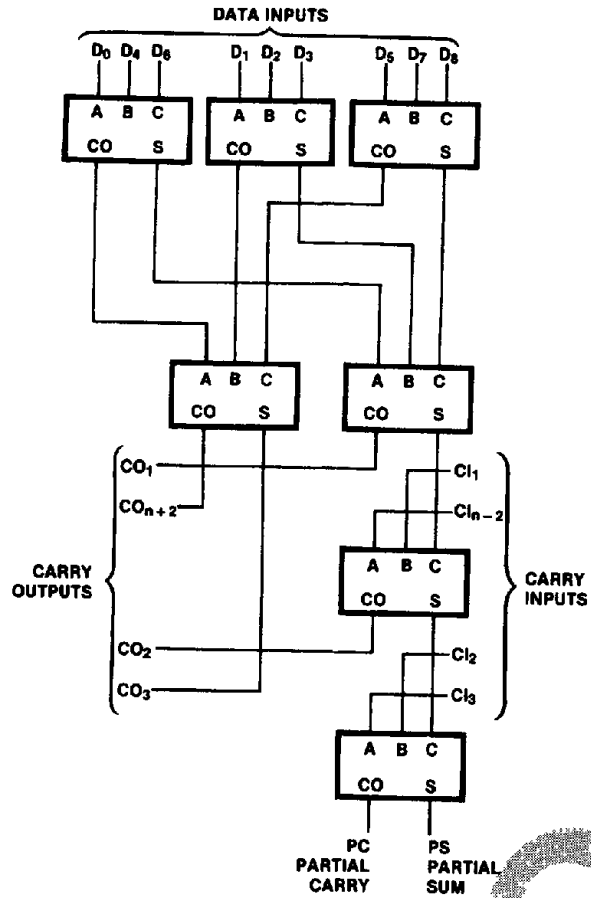
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## Adder Logic Diagram
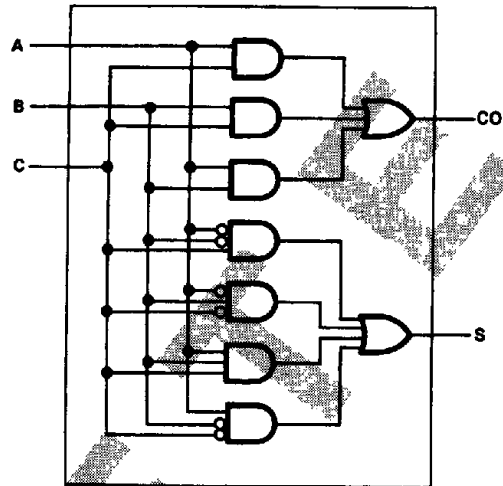


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### Adder Truth Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **A** | **B** | **C** | **S** | **CO** |
| L | L | L | L | L |
| L | L | H | H | L |
| L | H | L | H | L |
| L | H | H | L | H |
| H | L | L | H | L |
| H | L | H | L | H |
| H | H | L | L | H |
| H | H | H | H | H |

## Absolute Maximum Ratings
Above which the useful life may be impaired. (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Maximum Junction Temperature ($T_J$) | +150°C |
| Case Temperature under Bias ($T_C$) | 0°C to +85°C |
| $V_{EE}$ Pin Potential to Ground Pin | −7.0V to +0.5V |
| Input Voltage (DC) | $V_{EE}$ to +0.5V |
| Output Current (DC Output HIGH) | −50 mA |
| Operating Range (Note 2) | −5.7V to −4.2V |

## DC Electrical Characteristics
$V_{EE}$ = −4.5V, $V_{CC}$ = $V_{CCA}$ = GND, $T_C$ = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1025 | −955 | −880 | mV | $V_{IN}$ = $V_{IH}$ (Max) or $V_{IL}$ (Min) | Loading with 50Ω to −2.0V |
| $V_{OL}$ | Output LOW Voltage | −1810 | −1705 | −1620 | | | |
| $V_{OHC}$ | Output HIGH Voltage | −1035 | | | mV | $V_{IN}$ = $V_{IH}$ (Min) or $V_{IL}$ (Max) | Loading with 50Ω to −2.0V |
| $V_{OLC}$ | Output LOW Voltage | | | −1610 | | | |
| $V_{IH}$ | Input HIGH Voltage | −1165 | | −880 | mV | Guaranteed HIGH Signal for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | −1810 | | −1475 | mV | Guaranteed LOW Signal for All Inputs | |
| $I_{IL}$ | Input LOW Current | 0.50 | | | μA | $V_{IN}$ = $V_{IL}$ (Min) | |

## DC Electrical Characteristics
$V_{EE}$ = −4.2V, $V_{CC}$ = $V_{CCA}$ = GND, $T_C$ = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1020 | | −870 | mV | $V_{IN}$ = $V_{IH}$ (Max) or $V_{IL}$ (Min) | Loading with 50Ω to −2.0V |
| $V_{OL}$ | Output LOW Voltage | −1810 | | −1605 | | | |
| $V_{OHC}$ | Output HIGH Voltage | −1030 | | | mV | $V_{IN}$ = $V_{IH}$ (Min) or $V_{IL}$ (Max) | Loading with 50Ω to −2.0V |
| $V_{OLC}$ | Output LOW Voltage | | | −1595 | | | |
| $V_{IH}$ | Input HIGH Voltage | −1150 | | −870 | mV | Guaranteed HIGH Signal for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | −1810 | | −1475 | mV | Guaranteed LOW Signal for All Inputs | |
| $I_{IL}$ | Input LOW Current | 0.50 | | | μA | $V_{IN}$ = $V_{IL}$ (Min) | |

## DC Electrical Characteristics
$V_{EE}$ = −4.8V, $V_{CC}$ = $V_{CCA}$ = GND, $T_C$ = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1035 | | −880 | mV | $V_{IN}$ = $V_{IH}$ (Max) or $V_{IL}$ (Min) | Loading with 50Ω to −2.0V |
| $V_{OL}$ | Output LOW Voltage | −1830 | | −1620 | | | |
| $V_{OHC}$ | Output HIGH Voltage | −1045 | | | mV | $V_{IN}$ = $V_{IH}$ (Min) or $V_{IL}$ (Max) | Loading with 50Ω to −2.0V |
| $V_{OLC}$ | Output LOW Voltage | | | −1610 | | | |
| $V_{IH}$ | Input HIGH Voltage | −1165 | | −880 | mV | Guaranteed HIGH Signal for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | −1830 | | −1490 | mV | Guaranteed LOW Signal for All Inputs | |
| $I_{IL}$ | Input LOW Current | 0.50 | | | μA | $V_{IN}$ = $V_{IL}$ (Min) | |

**Note 1:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Parametric values specified at −4.2V to −4.8V.

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

**Note 4:** Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|--------|-----------|-----|-----|-----|-------|------------|
| $I_{IH}$ | Input HIGH Current $CI_1 - CI_3$, $CI_{n-2}$ $D_1$, $D_3$, $D_4$, $D_5$, $D_6$, $D_8$ | | | 300 | $\mu A$ | $V_{IN} = V_{IH (Max)}$ |
| | $D_0$, $D_2$, $D_7$ | | | 250 | | |
| $I_{EE}$ | Power Supply Current | $-260$ | $-180$ | $-125$ | mA | Inputs Open |

## Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0°C$ | | $T_C = +25°C$ | | $T_C = +85°C$ | | Units | Conditions |
|--------|-----------|-----|-----|-----|-----|-----|-----|-------|------------|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $D_n$ to $CO_{n+2}$ | 1.40 | 4.50 | 1.40 | 4.50 | 1.50 | 4.70 | ns | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $D_n$ to $CO_1$ | 1.30 | 4.80 | 1.30 | 4.70 | 1.50 | 5.00 | ns | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $D_n$ to $CO_2$ | 2.20 | 6.20 | 2.20 | 6.10 | 2.30 | 6.40 | ns | Figures 1 and 2 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $D_n$ to $CO_3$ | 1.30 | 4.70 | 1.40 | 4.70 | 1.50 | 5.00 | ns | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $D_n$ to PS, PC | 2.50 | 7.20 | 2.50 | 7.20 | 2.70 | 7.40 | ns | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $CI_{n-2}$, $CI_1$ to $CO_2$ | 1.00 | 3.50 | 1.00 | 3.40 | 1.10 | 3.70 | ns | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $CI_{n-2}$, $CI_1$ to PS, PC | 1.50 | 4.50 | 1.50 | 4.45 | 1.60 | 4.60 | ns | Figures 1 and 2 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $CI_3$, $CI_2$ to PS, PC | 0.80 | 3.30 | 0.80 | 3.20 | 0.90 | 3.60 | ns | |
| $t_{TLH}$ $t_{THL}$ | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | Figures 1 and 2 |

## Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0°C$ | | $T_C = +25°C$ | | $T_C = +85°C$ | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $D_n$ to $CO_{n+2}$ | 1.40 | 4.30 | 1.40 | 4.30 | 1.50 | 4.50 | ns | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $D_n$ to $CO_1$ | 1.30 | 4.60 | 1.30 | 4.50 | 1.50 | 4.80 | ns | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $D_n$ to $CO_2$ | 2.20 | 6.00 | 2.20 | 5.90 | 2.30 | 6.20 | ns | Figures 1 and 2 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $D_n$ to $CO_3$ | 1.30 | 4.50 | 1.40 | 4.50 | 1.50 | 4.80 | ns | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $D_n$ to PS, PC | 2.50 | 7.00 | 2.50 | 7.00 | 2.70 | 7.20 | ns | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $CI_{n-2}$, $CI_1$ to $CO_2$ | 1.00 | 3.30 | 1.00 | 3.20 | 1.10 | 3.50 | ns | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $CI_{n-2}$, $CI_1$ to PS, PC | 1.50 | 4.30 | 1.50 | 4.25 | 1.60 | 4.40 | ns | Figures 1 and 2 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $CI_3$, $CI_2$ to PS, PC | 0.80 | 3.10 | 0.80 | 3.00 | 0.90 | 3.40 | ns | |
| $t_{TLH}$ $t_{THL}$ | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.50 | 0.45 | 1.50 | ns | Figures 1 and 2 |

**Notes:**

$V_{CC}$, $V_{CCA}$ = +2V, $V_{EE}$ = −2.5V

L1 and L2 = equal length 50Ω impedance lines

$R_T$ = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to $V_{CC}$ and $V_{EE}$

All unused outputs are loaded with 50Ω to GND

$C_L$ = Fixture and stray capacitance ≤ 3 pF

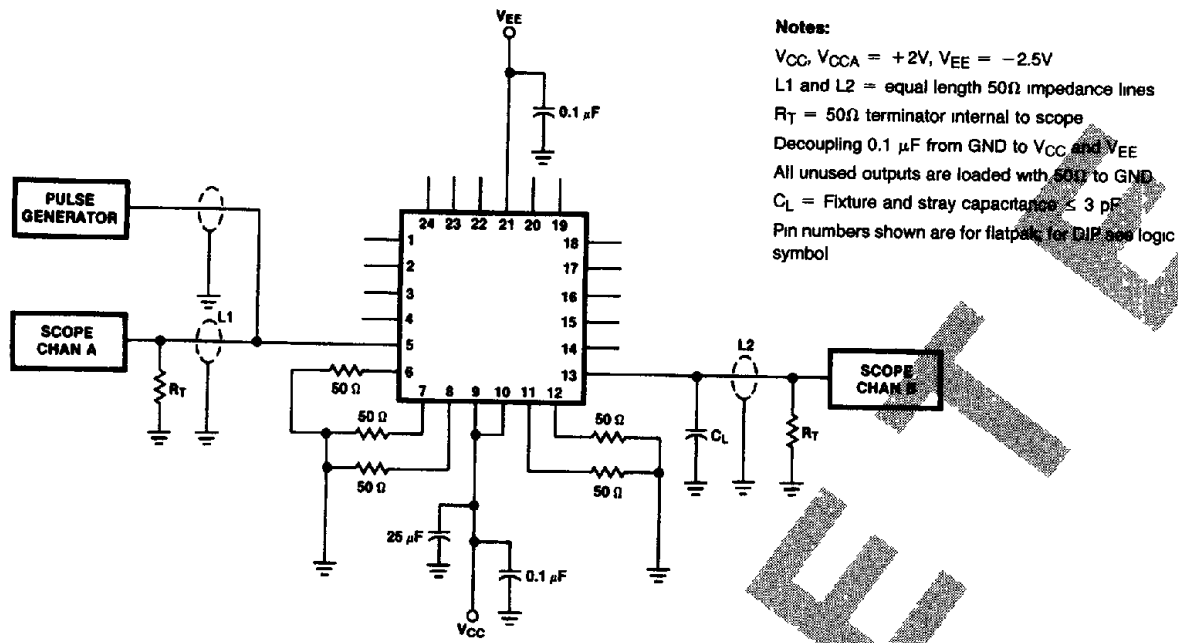Pin numbers shown are for flatpak; for DIP see logic symbol

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**FIGURE 1. AC Test Circuit**

TL/F/9874−8
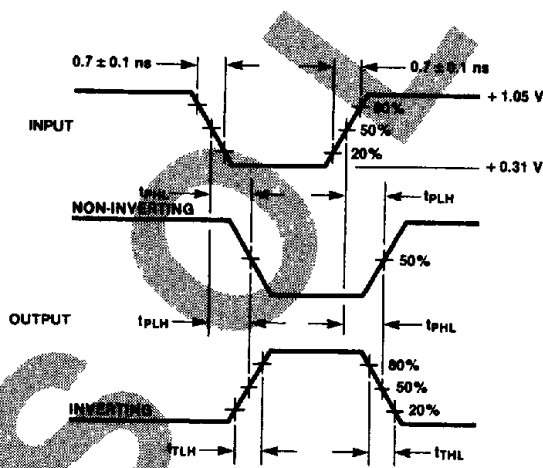
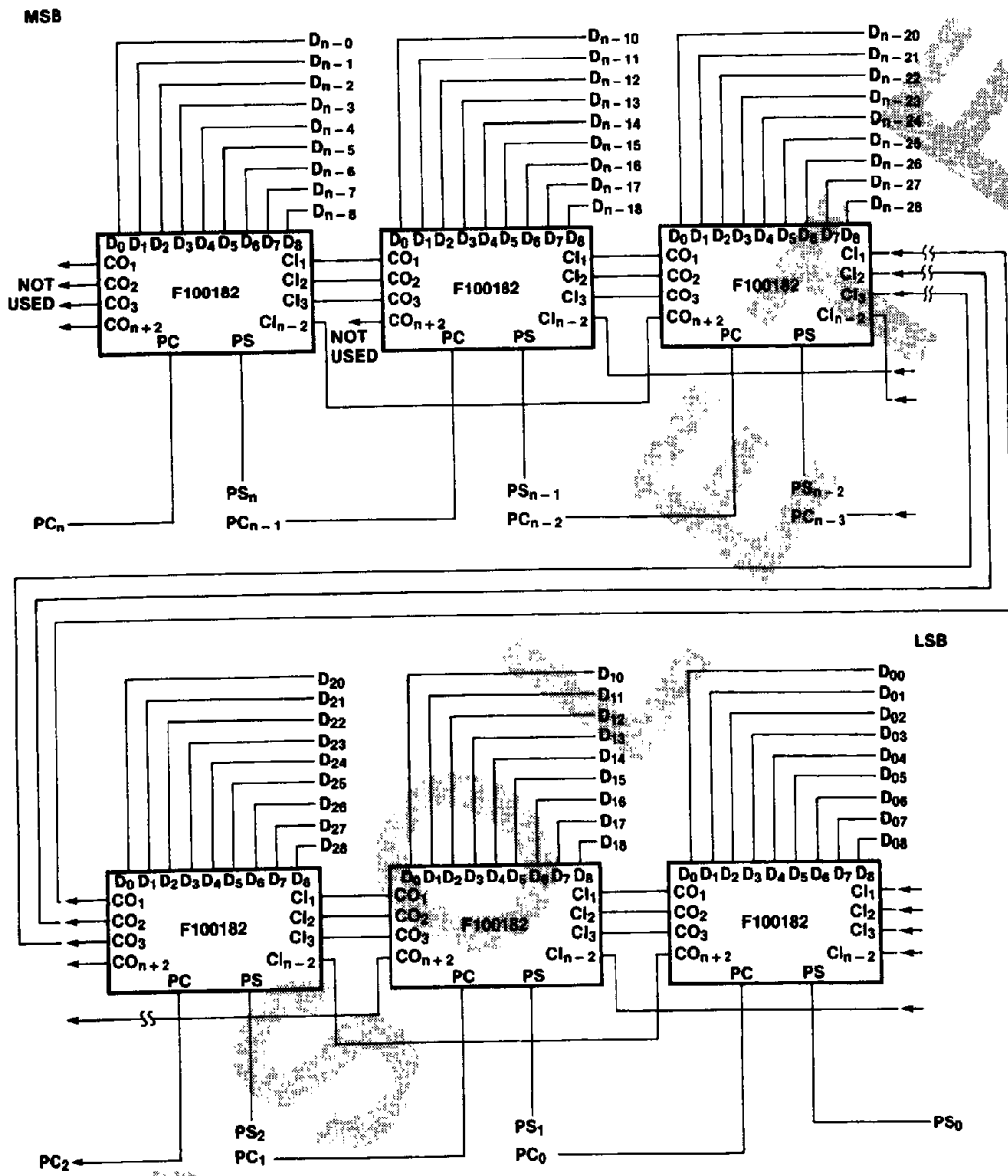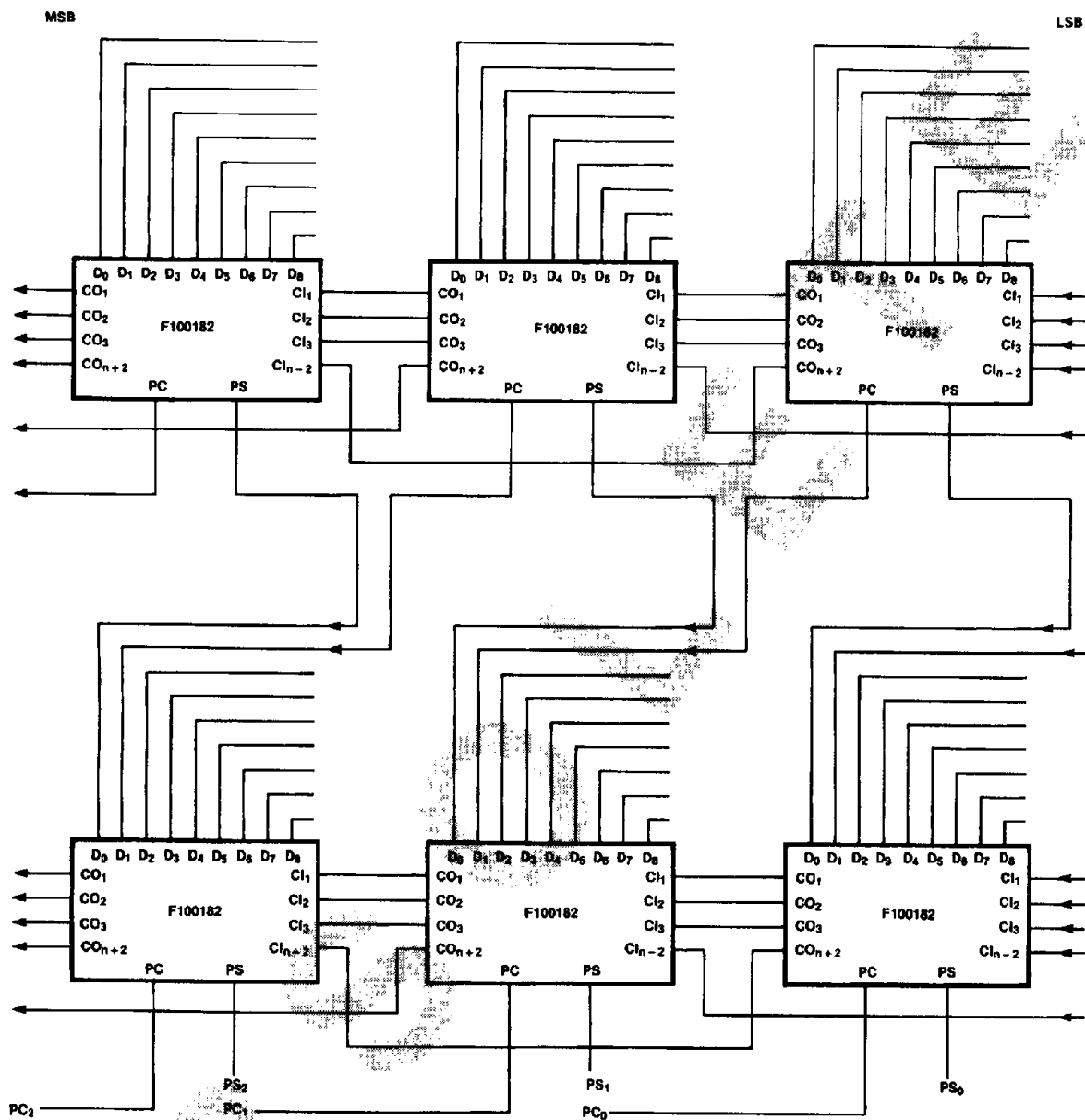**FIGURE 2. Propagation Delay and Transition Times**

# Application

### Typical Horizontal Interconnection of 9-Bit Wallace Tree Adders F100182



TL/F/9874–9

## 16-Bit Vertical Expansion of Wallace Tree Adders

MSB

LSB

TL/F/9874-10