

## 54164, DM74164

### 8-Bit Serial In/Parallel Out Shift Registers

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either serial input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

#### Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

#### Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

## 54164/DM74164 8-Bit Serial In/Parallel Out Shift Registers

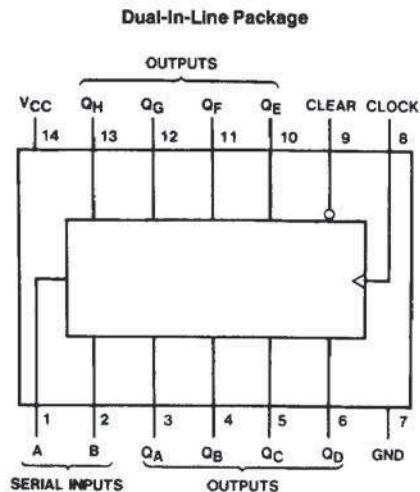
### General Description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either serial input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

### Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 185 mW

### Connection Diagram



Order Number 54164DMQB, 54164FMQB or DM74164N  
See NS Package Number J14A, N14A or W14B

### Function Table

Inputs				Outputs			
Clear	Clock	A	B	Q <sub>A</sub>	Q <sub>B</sub>	...	Q <sub>H</sub>
L	X	X	X	L	L	...	L
H	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	...	Q <sub>H0</sub>
H	↑	H	H	H	Q <sub>An</sub>	...	Q <sub>Gn</sub>
H	↑	L	X	L	Q <sub>An</sub>	...	Q <sub>Gn</sub>
H	↑	X	L	L	Q <sub>An</sub>	...	Q <sub>Gn</sub>

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

Q<sub>A0</sub>, Q<sub>B0</sub>, Q<sub>H0</sub> = The level of Q<sub>A</sub>, Q<sub>B</sub>, or Q<sub>H</sub>, respectively, before the indicated steady-state input conditions were established.

Q<sub>An</sub>, Q<sub>Gn</sub> = The level of Q<sub>A</sub> or Q<sub>G</sub> before the most recent ↑ transition of the clock; indicates a one-bit shift.

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	54164			DM74164			Units
		Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			2			V
V <sub>IL</sub>	Low Level Input Voltage			0.8			0.8	V
I <sub>OH</sub>	High Level Output Current			−0.4			−0.4	mA
I <sub>OL</sub>	Low Level Output Current			8			8	mA
f <sub>CLK</sub>	Clock Frequency (Note 4)			25	0		25	MHz
t <sub>w</sub>	Pulse Width (Note 4)	Clock	20		20			ns
		Clear	20		20			
t <sub>SU</sub>	Data Setup Time (Note 4)	15			15			ns
t <sub>H</sub>	Data Hold Time (Note 4)	0			5			ns
T <sub>A</sub>	Free Air Operating Temperature	−55		125	0		70	°C

**Electrical Characteristics** over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = −14 mA			−1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	2.4	3.2		V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IH</sub> = Min, V <sub>IL</sub> = Max		0.2	0.4	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.4V			40	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V			−1.6	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max	54	−10	−27.5	mA
		(Note 2) DM74		−9	−27.5	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 3)		37	54	mA

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time.

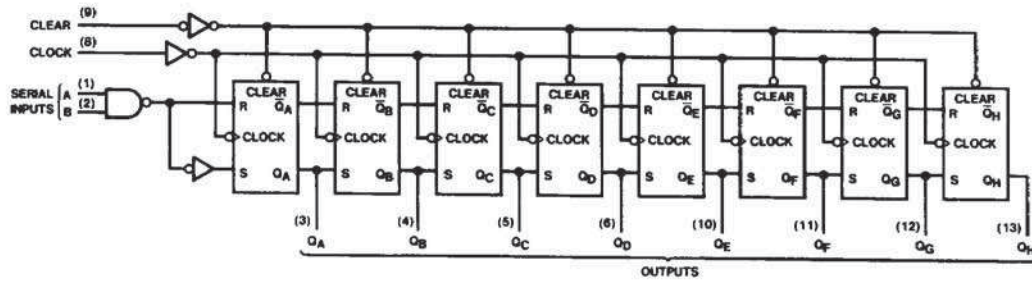
Note 3: I<sub>CC</sub> is measured with all outputs open, SERIAL inputs grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to the CLEAR input.

Note 4: T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

**Switching Characteristics** at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$  (See Section 1 for Test Waveforms and Output Load)

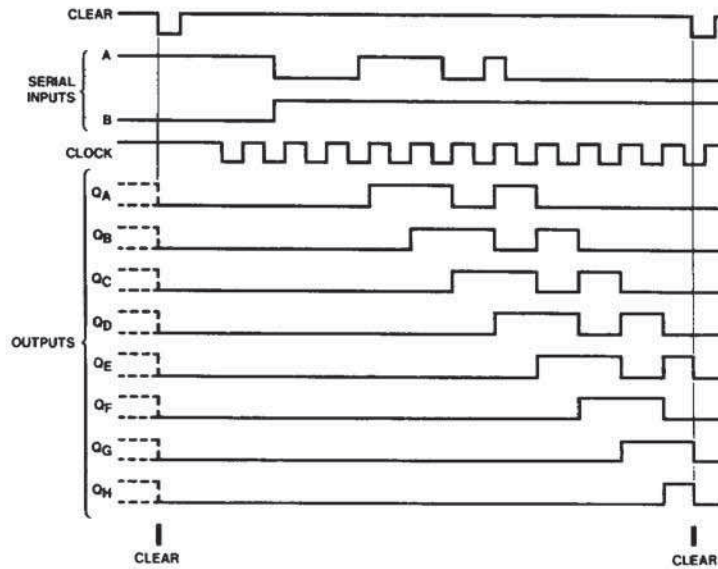
Symbol	Parameter	From (Input) To (Output)	$R_L = 800\Omega$				Units
			$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
			Min	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency		25				MHz
$t_{PLH}$	Propagation Delay Time Low to High Level Output	Clock to Output		27		30	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	Clock to Output		32		37	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	Clear to Output		36		42	ns

**Logic Diagram**



TL/F/6552-2

**Timing Diagram**



TL/F/6552-3