

54LS256, DM74LS256

Dual 4-Bit Addressable Latch

The 'LS256 is a dual 4-bit addressable latch with common control inputs; these include two Address inputs (A0, A1), an active LOW enable input (\overline{E}) and an active LOW Clear input (\overline{CL}). Each latch has a data input (D) and four outputs (Q0-Q3).

When the Enable (\overline{E}) is HIGH and the Clear input (\overline{CL}) is LOW, all outputs (Q0-Q3) are LOW. Dual 4-channel demultiplexing occurs when the \overline{CL} and \overline{E} are both LOW. When \overline{CL} is HIGH and \overline{E} is LOW, the selected output (Q0-Q3), determined by the Address inputs, follows D. When \overline{E} goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E} = \text{LOW}$, $\overline{CL} = \text{HIGH}$), changing more than one bit of the Address (A0, A1) could impose a transient wrong address. Therefore, this should be done only while in the memory mode ($\overline{E} = \overline{CL} = \text{HIGH}$).

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.



54LS256/DM74LS256 Dual 4-Bit Addressable Latch

General Description

The 'LS256 is a dual 4-bit addressable latch with common control inputs; these include two Address inputs (A0, A1), an active LOW enable input (\bar{E}) and an active LOW Clear input (\bar{CL}). Each latch has a Data input (D) and four outputs (Q0-Q3).

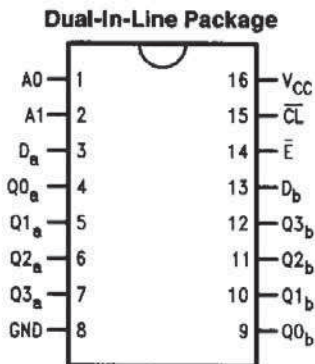
When the Enable (\bar{E}) is HIGH and the Clear input (\bar{CL}) is LOW, all outputs (Q0-Q3) are LOW. Dual 4-channel demultiplexing occurs when the \bar{CL} and \bar{E} are both LOW. When \bar{CL} is HIGH and \bar{E} is LOW, the selected output (Q0-Q3), determined by the Address inputs, follows D. When the \bar{E} goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode (\bar{E} = LOW, \bar{CL} = HIGH), changing more than one bit of the Address (A0, A1)

could impose a transient wrong address. Therefore, this should be done only while in the memory mode (\bar{E} = \bar{CL} = HIGH).

Features

- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Active low common clear

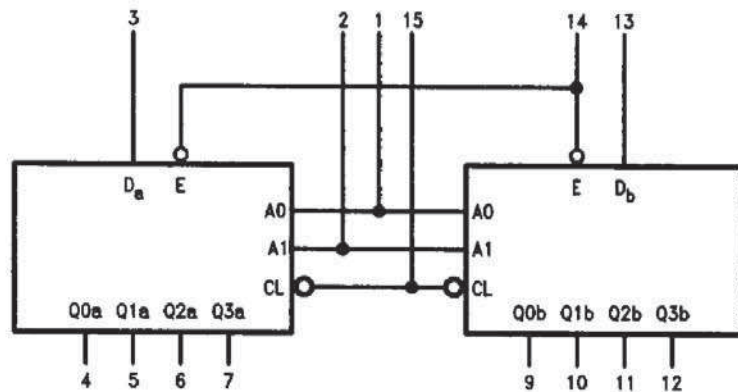
Connection Diagram



TL/F/9823-1

**Order Number 54LS256DMQB,
54LS256FMQB or DM74LS256N
See NS Package Number J16A,
N16E or W16A**

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

TL/F/9823-2

| Pin Names | Description |
|----------------------------------|--------------------------------------|
| A0, A1 | Common Address Inputs |
| D _a , D _b | Data Inputs |
| \bar{E} | Common Enable Input (Active LOW) |
| \bar{CL} | Conditional Clear Input (Active LOW) |
| Q0 _a -Q3 _a | Side A Latch Outputs |
| Q0 _b -Q3 _b | Side B Latch Outputs |

Truth Table

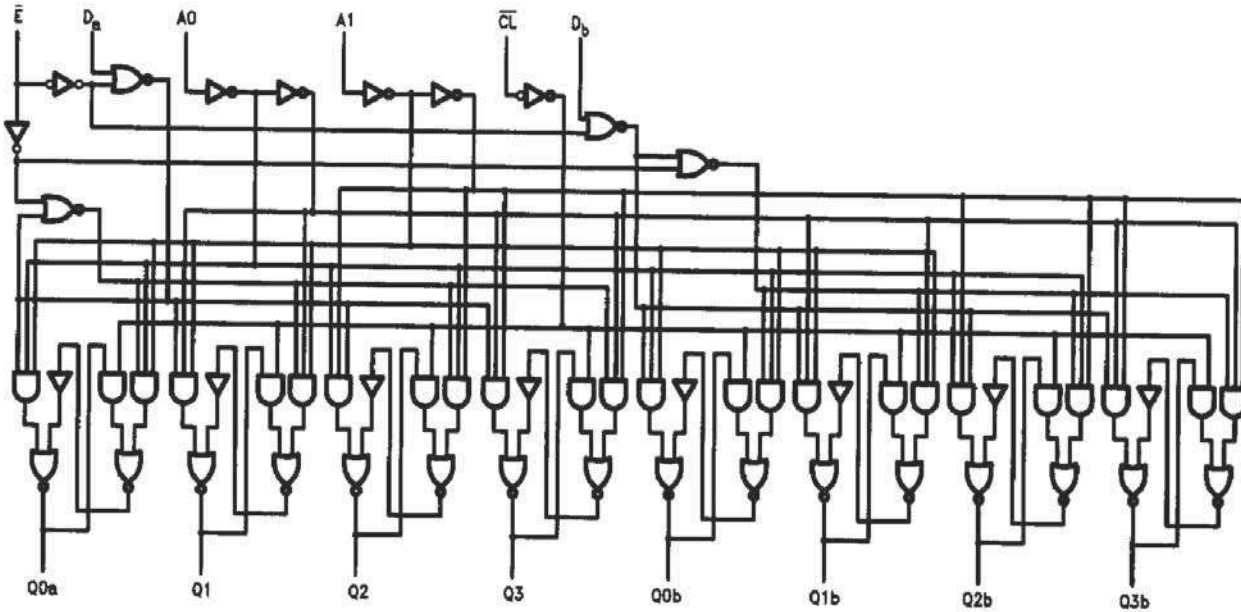
| Inputs | | | | Outputs | | | | Mode |
|-----------------|----------------|----|----|-----------|-----------|-----------|-----------|-------------------|
| \overline{CL} | \overline{E} | A0 | A1 | Q0 | Q1 | Q2 | Q3 | |
| L | H | X | X | L | L | L | L | Clear |
| L | L | L | L | D | L | L | L | Demultiplex |
| L | L | H | L | L | D | L | L | |
| L | L | L | H | L | L | D | L | |
| L | L | H | H | L | L | L | D | |
| H | H | X | X | Q_{t-1} | Q_{t-1} | Q_{t-1} | Q_{t-1} | Memory |
| H | L | L | L | D | Q_{t-1} | Q_{t-1} | Q_{t-1} | Addressable Latch |
| H | L | H | L | Q_{t-1} | D | Q_{t-1} | Q_{t-1} | |
| H | L | L | H | Q_{t-1} | Q_{t-1} | D | Q_{t-1} | |
| H | L | H | H | Q_{t-1} | Q_{t-1} | Q_{t-1} | D | |

$t-1$ = Bit time before address change or rising edge of E
 H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

Mode Selection

| E | \overline{CL} | Mode |
|---|-----------------|--------------------------------------|
| L | H | Addressable Latch |
| H | H | Memory |
| L | L | Active HIGH 4-Channel Demultiplexers |
| H | L | Clear |

Logic Diagram



TU/F/9823-3

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | |
| 54LS | -55°C to +125°C |
| DM74LS | 0°C to +70°C |
| Storage Temperature Range | -65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter | 54LS256 | | | DM74LS256 | | | Units |
|--|---|---------|-----|------|-----------|-----|------|-------|
| | | Min | Nom | Max | Min | Nom | Max | |
| V _{CC} | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} | High Level Input Voltage | 2 | | | 2 | | | V |
| V _{IL} | Low Level Input Voltage | | | 0.7 | | | 0.8 | V |
| I _{OH} | High Level Output Current | | | -0.4 | | | -0.4 | mA |
| I _{OL} | Low Level Output Current | | | 4 | | | 8 | mA |
| T _A | Free Air Operating Temperature | -55 | | 125 | 0 | | 70 | °C |
| t _s (H) | Setup Time HIGH, D _n to \bar{E} | 20 | | | 20 | | | ns |
| t _h (H) | Hold Time HIGH, D _n to \bar{E} | 0 | | | 0 | | | ns |
| t _s (L) | Setup Time LOW, D _n to \bar{E} | 15 | | | 15 | | | ns |
| t _h (L) | Hold Time LOW, D _n to \bar{E} | 0 | | | 0 | | | ns |
| t _s (H) t _s (L) | Setup Time HIGH or LOW, A _n to \bar{E} | 0 | | | 0 | | | ns |
| t _w (L) | \bar{E} Pulse Width LOW | 17 | | | 17 | | | ns |

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | | Min | Typ (Note 1) | Max | Units |
|-----------------|-----------------------------------|---|-----------|---|-----------------|------|-------|
| V _I | Input Clamp Voltage | V _{CC} = Min, I _I = -18 mA | | | | -1.5 | V |
| V _{OH} | High Level Output Voltage | V _{CC} = Min, I _{OH} = Max V _{IL} = Max | 54LS | 2.5 | | | V |
| | | | DM74 | 2.7 | 3.4 | | |
| V _{OL} | Low Level Output Voltage | V _{CC} = Min, I _{OL} = Max V _{IH} = Min | 54LS | | | 0.4 | V |
| | | | DM74 | | 0.35 | 0.5 | |
| | | | DM74 | I _{OL} = 4 mA, V _{CC} = Min | | 0.25 | |
| I _I | Input Current @ Max Input Voltage | V _{CC} = Max, V _I = 10V | Inputs | | | 0.1 | mA |
| | | | \bar{E} | | | 0.2 | |
| I _{IH} | High Level Input Current | V _{CC} = Max, V _I = 2.7V | Inputs | | | 20 | μA |
| | | | \bar{E} | | | 40 | |
| I _{IL} | Low Level Input Current | V _{CC} = Max, V _I = 0.4V | Inputs | | | -0.4 | mA |
| | | | \bar{E} | | | -0.8 | |
| I _{OS} | Short Circuit Output Current | V _{CC} = Max (Note 2) | 54LS | -20 | | -100 | mA |
| | | | DM74 | -20 | | -100 | |
| I _{CC} | Supply Current | V _{CC} = Max | | | | 25 | mA |

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25^{\circ}C$ (See Section 1 for waveforms and load configurations)

| Symbol | Parameter | $R_L = 2\text{ k}\Omega$ $C_L = 15\text{ pF}$ | Units |
|------------------------|--|--|-------|
| | | Max | |
| t_{PLH} t_{PHL} | Propagation Delay E to Q_n | 27 24 | ns |
| t_{PLH} t_{PHL} | Propagation Delay D_n to Q_n | 30 20 | ns |
| t_{PLH} t_{PHL} | Propagation Delay A_n to Q_n | 30 29 | ns |
| t_{PLH} | Propagation Delay $\bar{C}L$ to Q_n | 18 | ns |