74F433

First-In First-Out (FIFO) Buffer Memory

The 74F433 is an expandable fall-through type high-speed First-In First-Out (FIFO) Buffer Memory that is optimized for high-speed disk or tape controller and communication buffer applications. It is organized as 64-words by 4-bits and may be expanded to any number of words or any number of bits in multiples of four. Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The 74F433 has 3-STATE outputs that provide added versatility, and is fully compatible with all TTL families.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FAIRCHILD
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General Description

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The 74F433 has 3-STATE outputs that provide added versatility, and is fully compatible with all TTL families.

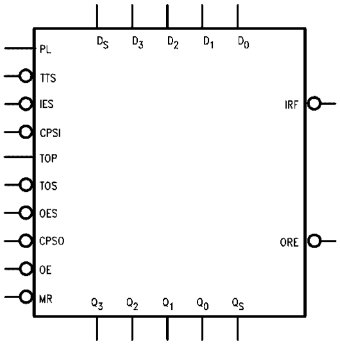
Features

- Serial or parallel input
- Serial or parallel output
- Expandable without additional logic
- 3-STATE outputs
- Fully compatible with all TTL families
- Slim 24-pin package
- 9423 replacement

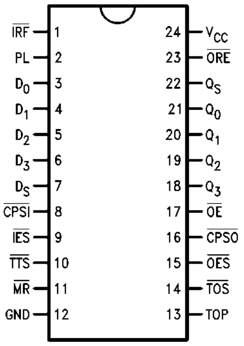
Ordering Code:

Order Number	Package Number	Package Description
74F433SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Logic Symbol



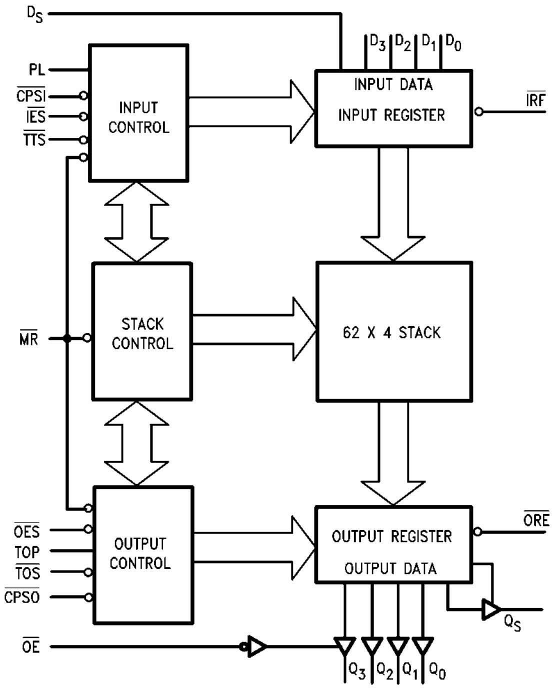
Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
PL	Parallel Load Input	1.0/0.66	20 µA/400 µA
$\overline{\text{CPSI}}$	Serial Input Clock	1.0/0.66	20 µA/400 µA
$\overline{\text{IES}}$	Serial Input Enable	1.0/0.66	20 µA/400 µA
$\overline{\text{TTS}}$	Transfer to Stack Input	1.0/0.66	20 µA/400 µA
$\overline{\text{MR}}$	Master Reset	1.0/0.66	20 µA/400 µA
$\overline{\text{OES}}$	Serial Output Enable	1.0/0.66	20 µA/400 µA
TOP	Transfer Out Parallel	1.0/0.66	20 µA/400 µA
$\overline{\text{TOS}}$	Transfer Out Serial	1.0/0.66	20 µA/400 µA
$\overline{\text{CPSO}}$	Serial Output Clock	1.0/0.66	20 µA/400 µA
$\overline{\text{OE}}$	Output Enable	1.0/0.66	20 µA/400 µA
D_0–D_3	Parallel Data Inputs	1.0/0.66	20 µA/400 µA
D_S	Serial Data Input	1.0/0.66	20 µA/400 µA
Q_0–Q_3	Parallel Data Outputs	285/10	5.7 mA/16 mA
Q_S	Serial Data Output	285/10	5.7 µA/16 mA
$\overline{\text{IRF}}$	Input Register Full	20/5	400 µA/8 mA
$\overline{\text{ORE}}$	Output Register Empty	20/5	400 µA/8 mA

Block Diagram



Functional Description

As shown in the block diagram, the 74F433 consists of three sections:

1. An Input Register with parallel and serial data inputs, as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit-wide, 62-word-deep fall-through stack with self-contained control logic.
3. An Output Register with parallel and serial data outputs, as well as control inputs and outputs for output handshaking and expansion.

These three sections operate asynchronously and are virtually independent of one another.

Input Register (Data Entry)

The Input Register can receive data in either bit-serial or 4-bit parallel form. It stores this data until it is sent to the fall-through stack, and also generates the necessary status and control signals.

This 5-bit register (see Figure 1) is initialized by setting flip-flop F_3 and resetting the other flip-flops. The $\overline{Q}$-output of the last flip-flop (FC) is brought out as the Input Register Full (IRF) signal. After initialization, this output is HIGH.

Parallel Entry—A HIGH on the Parallel Load (PL) input loads the D_0–D_3 inputs into the F_0–F_3 flip-flops and sets the FC flip-flop. This forces the $\overline{IRF}$ output LOW, indicating that the input register is full. During parallel entry, the Serial Input Clock ($\overline{CPSI}$) input must be LOW.

Serial Entry—Data on the Serial Data (D_S) input is serially entered into the shift register (F_3, F_2, F_1, F_0, FC) on each HIGH-to-LOW transition of the $\overline{CPSI}$ input when the Serial Input Enable ($\overline{IES}$) signal is LOW. During serial entry, the PL input should be LOW.

After the fourth clock transition, the four data bits are located in flip-flops F_0–F_3. The FC flip-flop is set, forcing the $\overline{IRF}$ output LOW and internally inhibiting $\overline{CPSI}$ pulses from affecting the register. Figure 2 illustrates the final positions in an 74F433 resulting from a 256-bit serial bit train (B_0 is the first bit, B_{255} the last).

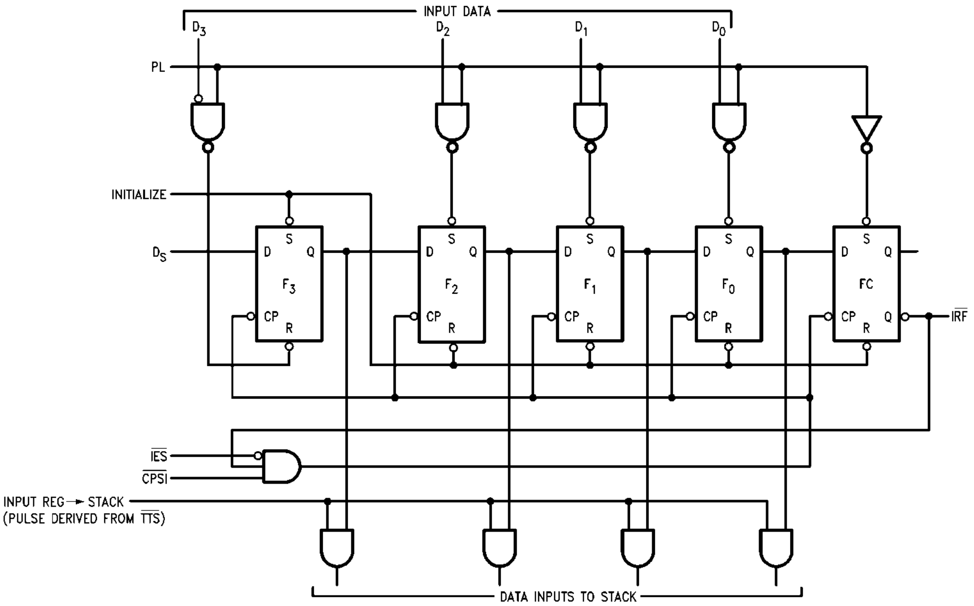


FIGURE 1. Conceptual Input Section

Functional Description (Continued)

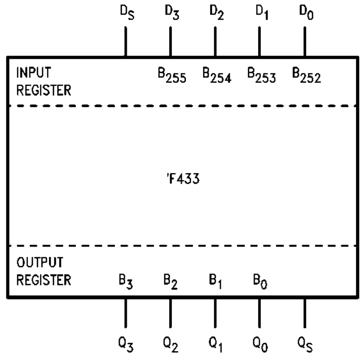


FIGURE 2. Final Positions in an 74F433 Resulting from a 256-Bit Serial Train

Fall-Through Stack—The outputs of flip-flops F_0–F_3 feed the stack. A LOW level on the Transfer to Stack ($\overline{TTS}$) input initiates a fall-through action; if the top location of the stack is empty, data is loaded into the stack and the input register is re-initialized. (Note that this initialization is delayed until PL is LOW). Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

An RS-type flip-flop (the initialization flip-flop) in the control section records the fact that data has been transferred to the stack. This prevents multiple entry of the same word into the stack even though $\overline{IRF}$ and $\overline{TTS}$ may still be LOW; the initialization flip-flop is not cleared until PL goes LOW.

Once in the stack, data falls through automatically, pausing only when it is necessary to wait for an empty next location. In the 74F433, the master reset ($\overline{MR}$) input only initializes the stack control section and does not clear the data.

Output Register

The Output Register (see Figure 3) receives 4-bit data words from the bottom stack location, stores them, and outputs data on a 3-STATE, 4-bit parallel data bus or on a 3-STATE serial data bus. The output section generates and receives the necessary status and control signals.

Parallel Extraction—When the FIFO is empty after a LOW pulse is applied to the MR input, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the output register, if the Transfer Out Parallel (TOP) input is HIGH. As a result of the data transfer, $\overline{ORE}$ goes HIGH, indicating valid data on the data outputs (provided that the 3-STATE buffer is enabled). The TOP input can then be used to clock out the next word.

When TOP goes LOW, $\overline{ORE}$ also goes LOW, indicating that the output data has been extracted; however, the data itself remains on the output bus until a HIGH level on TOP permits the transfer of the next word (if available) into the output register. During parallel data extraction, the serial output clock ($\overline{CPSO}$) line should be LOW. The Transfer Out Serial ($\overline{TOS}$) line should be grounded for single-slice operation or connected to the appropriate $\overline{ORE}$ line for expanded operation (refer to the "Expansion" section).

The TOP signal is not edge-triggered. Therefore, if TOP goes HIGH before data is available from the stack but data becomes available before TOP again goes LOW, that data is transferred into the output register. However, internal control circuitry prevents the same data from being transferred twice. If TOP goes HIGH and returns to LOW before data is available from the stack, $\overline{ORE}$ remains LOW, indicating that there is no valid data at the outputs.

Serial Extraction—When the FIFO is empty after a LOW is applied to the MR input, the $\overline{ORE}$ output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the output register, if the $\overline{TOS}$ input is LOW and TOP is HIGH. As a result of the data transfer, $\overline{ORE}$ goes HIGH, indicating that valid data is in the register.

The 3-STATE Serial Data Output (Q_S) is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{CPSO}$. To prevent false shifting, $\overline{CPSO}$ should be LOW when the new word is being loaded into the output register. The fourth transition empties the shift register, forces $\overline{ORE}$ LOW, and disables the serial output, Q_S. For serial operation, the $\overline{ORE}$ output may be tied to the $\overline{TOS}$ input, requesting a new word from the stack as soon as the previous one has been shifted out.

Expansion

Vertical Expansion—The 74F433 may be vertically expanded, without external components, to store more words. The interconnections necessary to form a 190-word by 4-bit FIFO are shown in Figure 4. Using the same technique, any FIFO of (63n+1)-words by 4-bits can be configured, where n is the number of devices. Note that expansion does not sacrifice any of the 74F433 flexibility for serial/parallel input and output.

Functional Description (Continued)

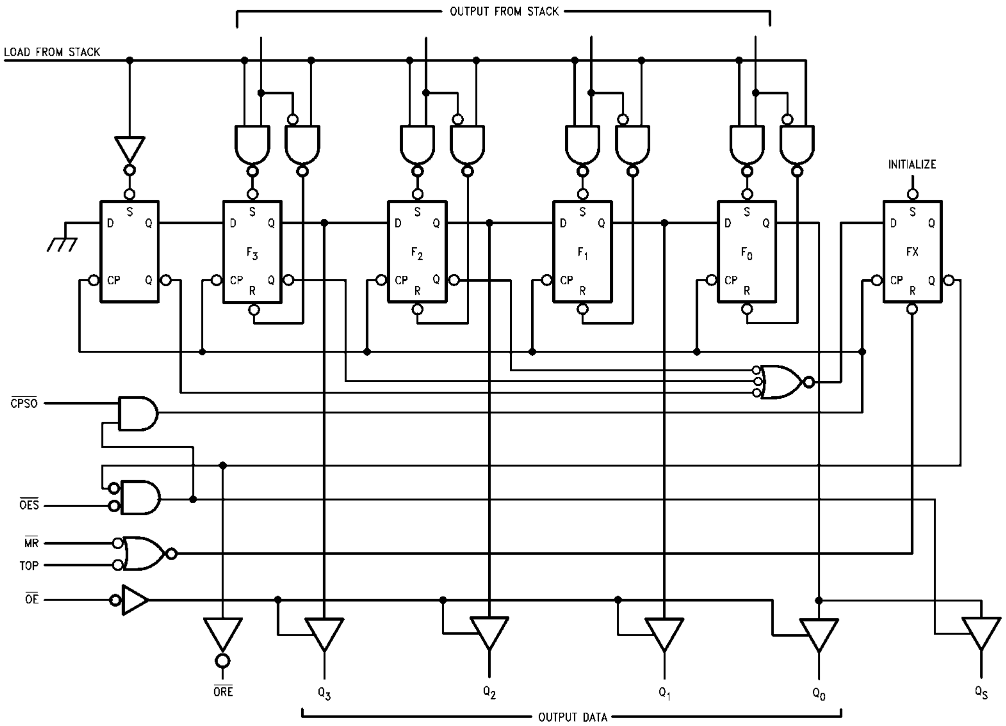


FIGURE 3. Conceptual Output Section

Functional Description (Continued)

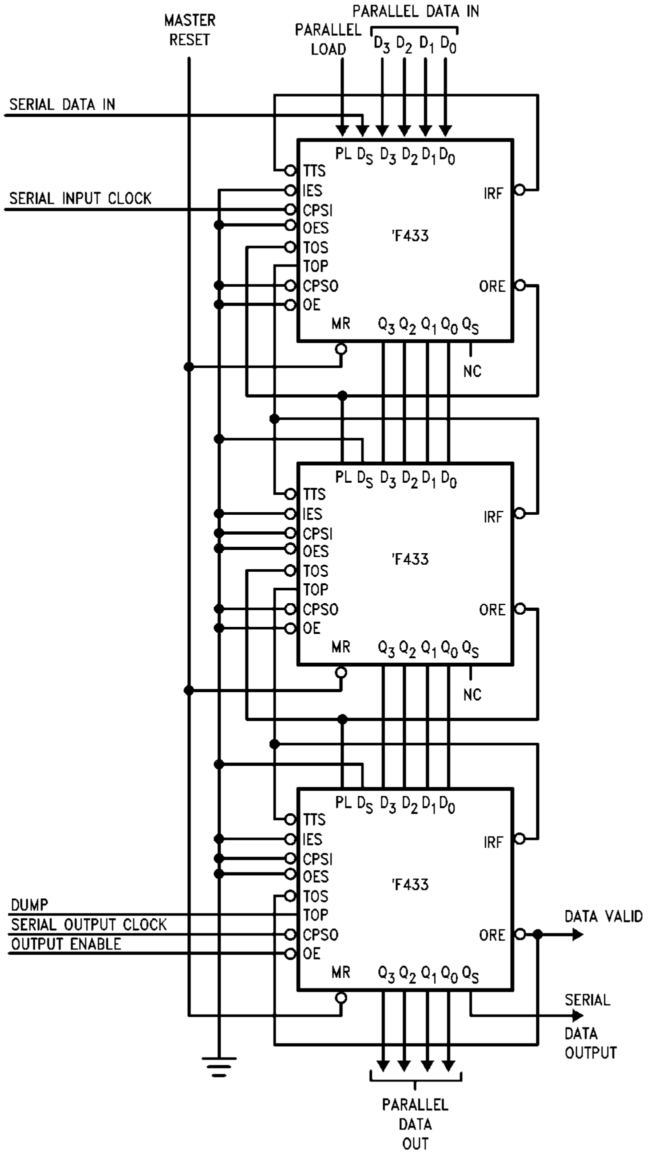


FIGURE 4. A Vertical Expansion Scheme

Horizontal Expansion—The 74F433 can be horizontally expanded, without external logic, to store long words (in multiples of 4-bits). The interconnections necessary to form a 64-word by 12-bit FIFO are shown in Figure 5. Using the same technique, any FIFO of 64-words by 4n-bits can be constructed, where n is the number of devices.

The right-most (most significant) device is connected to the TTS inputs of all devices. Similarly, the $\overline{\text{ORE}}$ output of the most significant device is connected to the $\overline{\text{TOS}}$ inputs of all devices. As in the vertical expansion scheme, horizontal expansion does not sacrifice any of the 74F433 flexibility for serial/parallel input and output.

It should be noted that the horizontal expansion scheme shown in Figure 5 exacts a penalty in speed.

Horizontal and Vertical Expansion—The 74F433 can be expanded in both the horizontal and vertical directions without any external components and without sacrificing any of its FIFO flexibility for serial/parallel input and output. The interconnections necessary to form a 127-word by 16-bit FIFO are shown in Figure 6. Using the same technique, any FIFO of (63m+1)-words by 4n-bits can be configured, where m is the number of devices in a column and n is the number of devices in a row. Figure 7 and Figure 8 illustrate the timing diagrams for serial data entry and extraction for

Functional Description (Continued)

the FIFO shown in Figure 6. Figure 9 illustrates the final positions of bits in an expanded 74F433 FIFO resulting from a 2032-bit serial bit train.

Interlocking Circuitry—Most conventional FIFO designs provide status signal analogous to $\overline{\text{IRF}}$ and $\overline{\text{ORE}}$. However, when these devices are operated in arrays, variations in unit-to-unit operating speed require external gating to ensure that all devices have completed an operation. The 74F433 incorporates simple but effective 'master/slave' interlocking circuitry to eliminate the need for external gating.

In the 74F433 array of Figure 6, devices 1 and 5 are the row masters; the other devices are slaves to the master in their rows. No slave in a given row initializes its input register until it has received a LOW on its $\overline{\text{IES}}$ input from a row master or a slave of higher priority.

Similarly, the $\overline{\text{ORE}}$ outputs of slaves do not go HIGH until their inputs have gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{\text{IRF}}$ output of the final slave in that row goes HIGH and that output data for the array may be extracted when the $\overline{\text{ORE}}$ output of the final slave in the output row goes HIGH.

The row master is established by connecting its $\overline{\text{IES}}$ input to ground, while a slave receives its $\overline{\text{IES}}$ input from the $\overline{\text{IRF}}$ output of the next-higher priority device. When an array of 74F433 FIFOs is initialized with a HIGH on the MR inputs of all devices, the $\overline{\text{IRF}}$ outputs of all devices are HIGH. Thus, only the row master receives a LOW on the $\overline{\text{IES}}$ input during initialization.

Figure 10 is a conceptual logic diagram of the internal circuitry that determines master/slave operation. When $\overline{\text{MR}}$ and $\overline{\text{IES}}$ are LOW, the master latch is set. When $\overline{\text{TTS}}$ goes LOW, the initialization flip-flop is set. If the master latch is HIGH, the input register is immediately initialized and the initialization flip-flop reset. If the master latch is reset, the input register is not initialized until $\overline{\text{IES}}$ goes LOW. In array operation, activating $\overline{\text{TTS}}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{\text{TOS}}$ or TOP input initiates a load-from-stack operation and sets the $\overline{\text{ORE}}$ request flip-flop. If the master latch is set, the last output register flip-flop is set and the $\overline{\text{ORE}}$ line goes HIGH. If the master latch is reset, the $\overline{\text{ORE}}$ output is LOW until a Serial Output Enable ($\overline{\text{OES}}$) input is received.

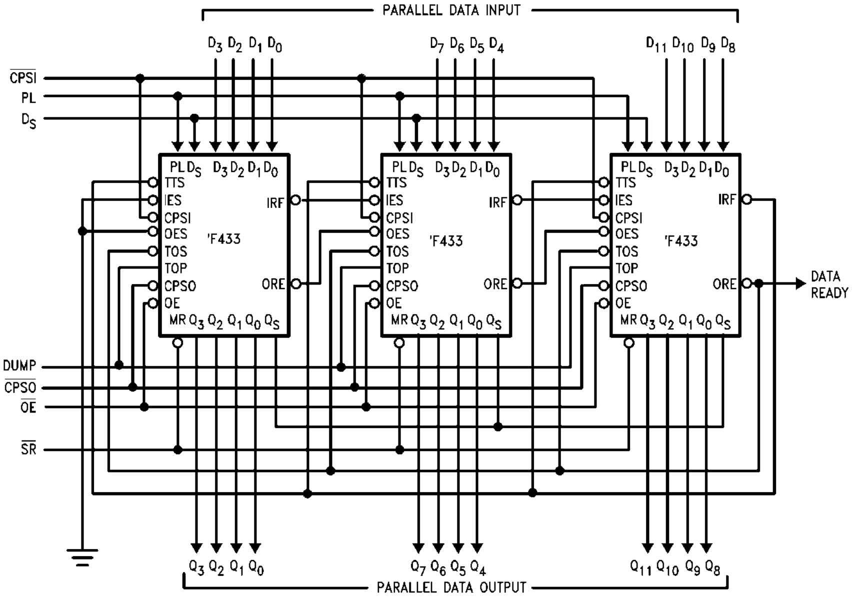


FIGURE 5. A Horizontal Expansion Scheme

Functional Description (Continued)

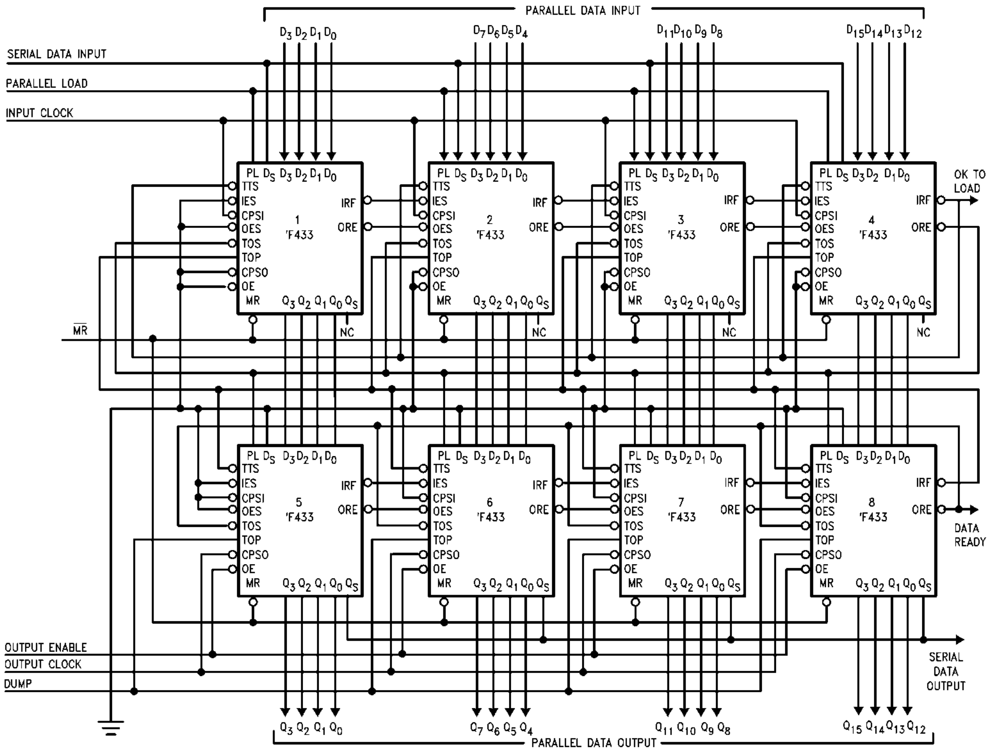


FIGURE 6. A 127 x 16 FIFO Array

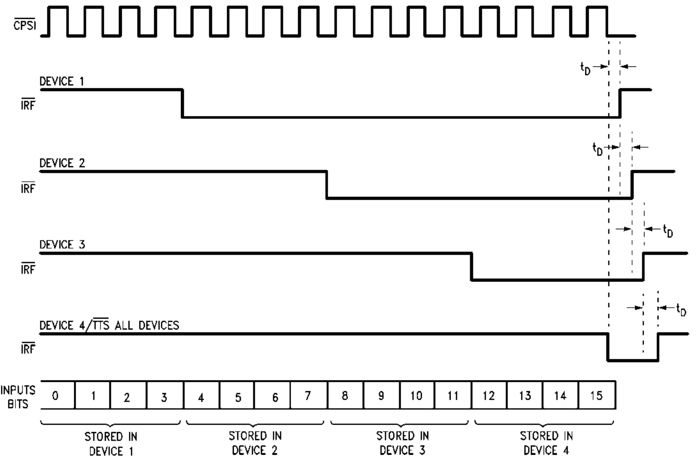


FIGURE 7. Serial Data Entry for Array of Figure

Functional Description (Continued)

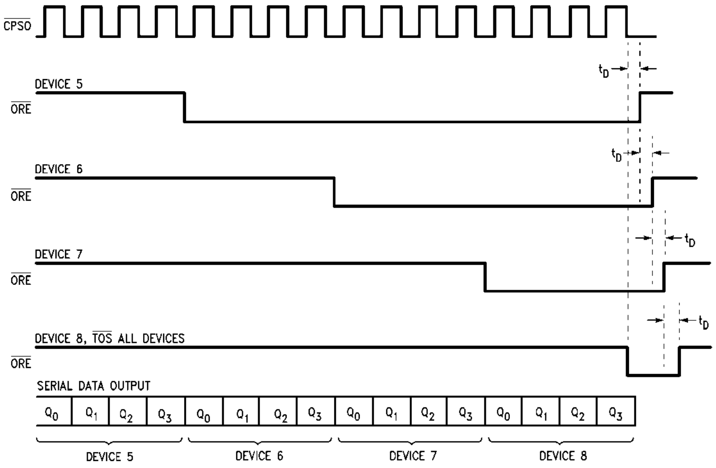


FIGURE 8. Serial Data Extraction for Array of Figure

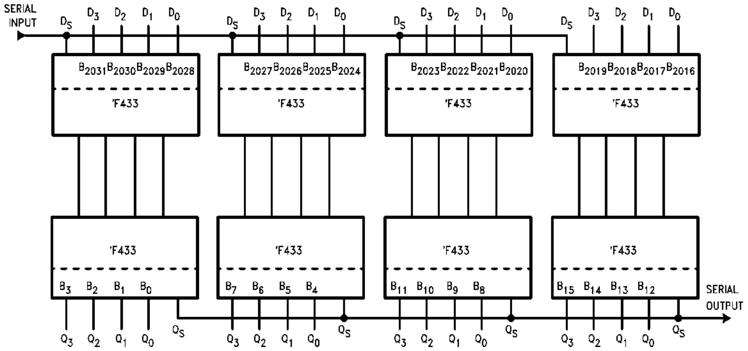


FIGURE 9. Final Position of a 2032-Bit Serial Input

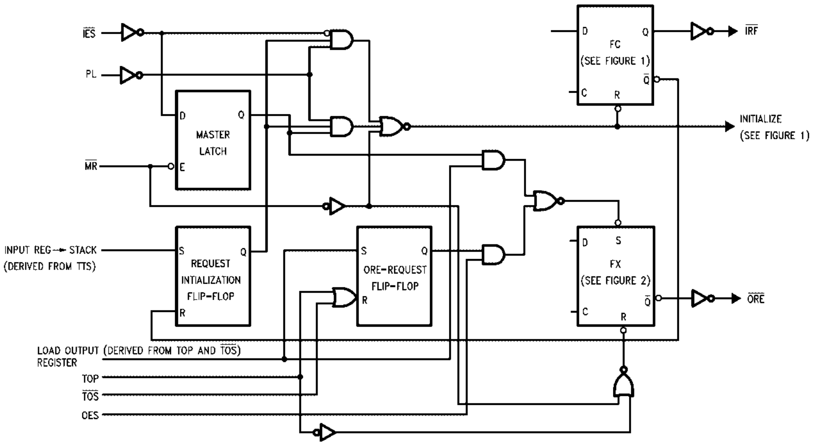


FIGURE 10. Conceptual Diagram, Interlocking Circuitry

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.5	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.4			V	Min	I_{OH} = 400 µA ($\overline{ORE}$, $\overline{IRF}$)
		10% V_{CC}	2.4					I_{OH} = 5.7 mA (Q_n, Q_s)
		5% V_{CC}	2.7					I_{OH} = 400 µA ($\overline{ORE}$, $\overline{IRF}$)
		5% V_{CC}	2.7					I_{OH} = 5.7 mA (Q_n, Q_s)
V_{OL}	Output LOW Voltage	10% V_{CC}			0.50	V	Min	I_{OL} = 16 mA (Q_n, Q_s)
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.4	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	µA	Max	V_{OUT} = 2.7V (Q_n, Q_s)
I_{OZL}	Output Leakage Current				−50	µA	Max	V_{OUT} = 0.5V (Q_n, Q_s)
I_{OS}	Output Short-Circuit Current		−20		−130	mA	Max	V_{OUT} = 0V
I_{CC}	Power Supply Current			150	215	mA	Max	

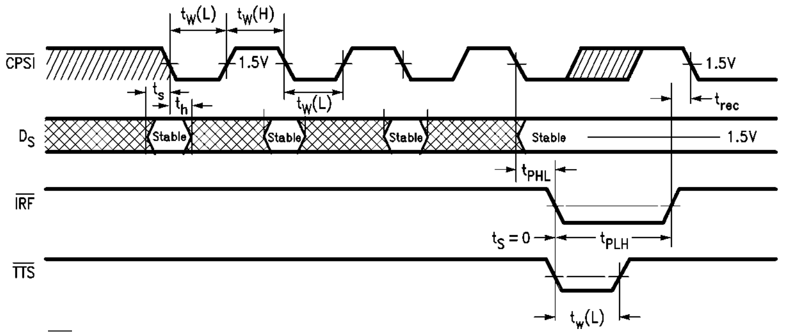
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		Units	Figure Number
		Min	Max	Min	Max		
t_{PHL}	Propagation Delay, Negative-Going CPSI to $\overline{\text{IRF}}$ Output	2.0	17.0	2.0	18.0	ns	Figures 11, 12
t_{PLH}	Propagation Delay, Negative-Going $\overline{\text{TTS}}$ to $\overline{\text{IRF}}$	9.0	34.0	8.0	38.0		
t_{PLH}	Propagation Delay, Negative-Going $\overline{\text{CPSO}}$ to Q_S Output	4.0	25.0	3.0	27.0	ns	Figures 13, 14
t_{PHL}		5.0	20.0	5.0	21.0		
t_{PLH}	Propagation Delay, Positive-Going TOP to Q_0–Q_3 Outputs	8.0	35.0	7.0	38.0	ns	Figure 15
t_{PHL}		7.0	30.0	7.0	32.0		
t_{PHL}	Propagation Delay, Negative-Going $\overline{\text{CPSO}}$ to $\overline{\text{ORE}}$	7.0	25.0	6.0	28.0	ns	Figures 13, 14
t_{PHL}	Propagation Delay, Negative-Going TOP to $\overline{\text{ORE}}$	6.0	26.0	6.0	28.0	ns	Figure 15
t_{PLH}	Propagation Delay, Positive-Going TOP to $\overline{\text{ORE}}$	13.0	48.0	12.0	51.0		
t_{PLH}	Propagation Delay, Negative-Going $\overline{\text{TOS}}$ to Positive-Going $\overline{\text{ORE}}$	13.0	45.0	12.0	50.0	ns	Figures 13, 14
t_{PHL}	Propagation Delay, Positive-Going PL to Negative-Going $\overline{\text{IRF}}$	4.0	22.0	4.0	23.0	ns	Figures 17, 18
t_{PLH}	Propagation Delay, Negative-Going PL to Positive-Going $\overline{\text{IRF}}$	7.0	31.0	6.0	35.0		
t_{PLH}	Propagation Delay, Positive-Going $\overline{\text{OES}}$ to $\overline{\text{ORE}}$	9.0	38.0	8.0	44.0	ns	
t_{PLH}	Propagation Delay Positive-$\overline{\text{IRF}}$ Going $\overline{\text{IES}}$ to Positive-Going	5.0	25.0	5.0	27.0	ns	Figure 18
t_{PHL}	Propagation Delay MR to $\overline{\text{ORE}}$	7.0	28.0	7.0	31.0	ns	
t_{PLH}	Propagation Delay MR to $\overline{\text{IRF}}$	5.0	27.0	5.0	30.0	ns	
t_{PZH}	Enable Time $\overline{\text{OE}}$ to Q_0–Q_3	1.0	16.0	1.0	18.0	ns	
t_{PZL}		1.0	14.0	1.0	16.0		
t_{PHZ}	Disable Time $\overline{\text{OE}}$ to Q_0–Q_3	1.0	10.0	1.0	12.0		
t_{PLZ}		1.0	23.0	1.0	30.0		
t_{PZH}	Enable Time Negative-Going $\overline{\text{OES}}$ to Q_S	1.0	10.0	1.0	12.0	ns	
t_{PZL}		1.0	14.0	1.0	15.0		
t_{PHZ}	Disable Time Negative-Going $\overline{\text{OES}}$ to Q_S	1.0	10.0	1.0	12.0		
t_{PLZ}		1.0	14.0	1.0	16.0		
t_{PZH}	Enable Time $\overline{\text{TOS}}$ to Q_S	1.0	35.0	1.0	42.0	ns	
t_{PZL}		1.0	35.0	1.0	39.0		
t_{DFT}	Fall-Through Time	0.2	0.9	0.2	1.0	ns	Figure 16
t_{AP}	Parallel Appearance Time $\overline{\text{ORE}}$ to Q_0–Q_3	–20.0	–2.0	–20.0	–2.0	ns	
t_{AS}	Serial Appearance Time $\overline{\text{ORE}}$ to Q_S	–20.0	5.0	–20.0	5.0		

AC Operating Requirements

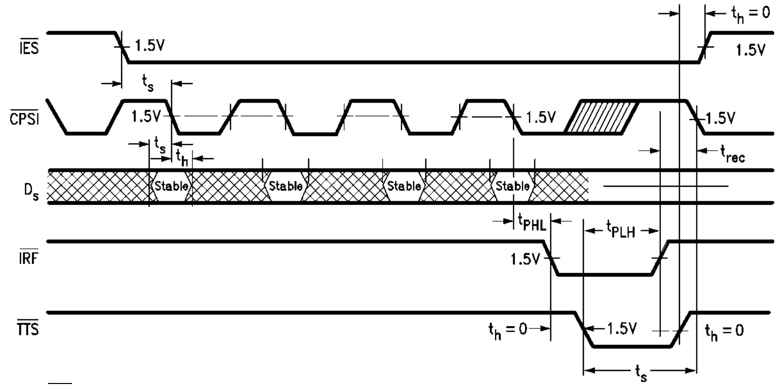
Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$		Units	Figure Number
		Min	Max	Min	Max		
t_S(H)	Setup Time, HIGH or LOW	7.0		7.0		ns	Figures 11, 12
t_S(L)	D_S to Negative $\overline{\text{CPSI}}$	7.0		7.0			
t_H(H)	Hold Time, HIGH or LOW	2.0		2.0			
t_H(L)	D_S to $\overline{\text{CPSI}}$	2.0		2.0			
t_S(L)	Setup Time, LOW $\overline{\text{TTS}}$ to $\overline{\text{IRF}}$, Serial or Parallel Mode	0.0		0.0		ns	Figures 11, 12, 17, 18
t_S(L)	Setup Time, LOW Negative-Going $\overline{\text{ORE}}$ to Negative-Going $\overline{\text{TOS}}$	0.0		0.0		ns	Figures 13, 14
t_S(L)	Setup Time, LOW Negative-Going $\overline{\text{IES}}$ to $\overline{\text{CPSI}}$	8.0		9.0		ns	Figure 12
t_S(L)	Setup Time, LOW Negative-Going $\overline{\text{TTS}}$ to $\overline{\text{CPSI}}$	30.0		33.0			
t_S(H)	Setup Time, HIGH or LOW	0.0		0.0		ns	
t_S(L)	Parallel Inputs to PL	0.0		0.0			
t_H(H)	Hold Time, HIGH or LOW	4.0		4.0			
t_H(L)	Parallel Inputs to PL	4.0		4.0			
t_W(H)	$\overline{\text{CPSI}}$ Pulse Width	10.0		11.0		ns	Figures 11, 12
t_W(L)	HIGH or LOW	5.0		6.0			
t_W(H)	PL Pulse Width, HIGH	7.0		9.0		ns	Figures 17, 18
t_W(L)	$\overline{\text{TTS}}$ Pulse Width, LOW Serial or Parallel Mode	7.0		9.0		ns	Figures 11, 12, 13, 14
t_W(L)	$\overline{\text{MR}}$ Pulse Width, LOW	7.0		9.0		ns	Figure 16
t_W(H)	TOP Pulse Width	14.0		16.0		ns	Figure 15
t_W(L)	HIGH or LOW	7.0		7.0			
t_W(H)	$\overline{\text{CPSO}}$ Pulse Width	14.0		16.0		ns	Figures 13, 14
t_W(L)	HIGH or LOW	7.0		7.0			
t_{REC}	Recovery Time $\overline{\text{MR}}$ to Any Input	8.0		15.0		ns	Figure 16

Timing Waveforms



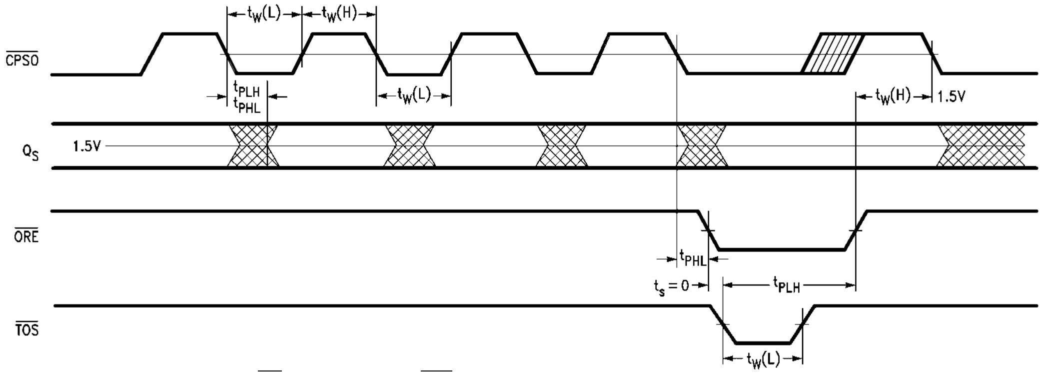
Conditions: Stack not full, $\overline{\text{IES}}$, PL LOW

FIGURE 11. Serial Input, Unexpanded or Master Operation



Conditions: Stack not full, $\overline{\text{IES}}$ HIGH when initiated, PL LOW

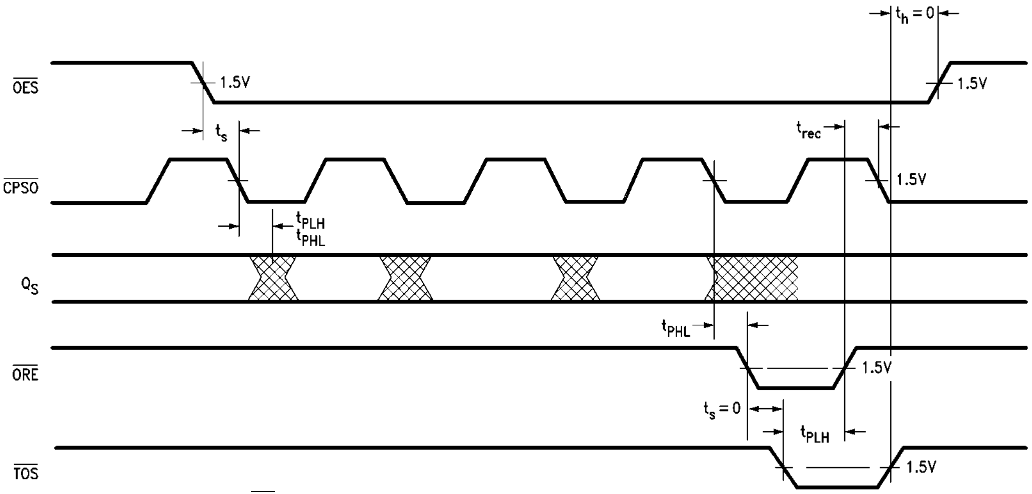
FIGURE 12. Serial Input, Expanded Slave Operation



Conditions: Data in stack, TOP HIGH, $\overline{\text{IES}}$ LOW when initiated, $\overline{\text{OES}}$ LOW

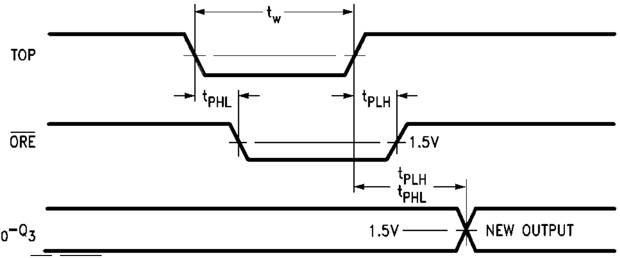
FIGURE 13. Serial Output, Unexpanded or Master Operation

Timing Waveforms (Continued)



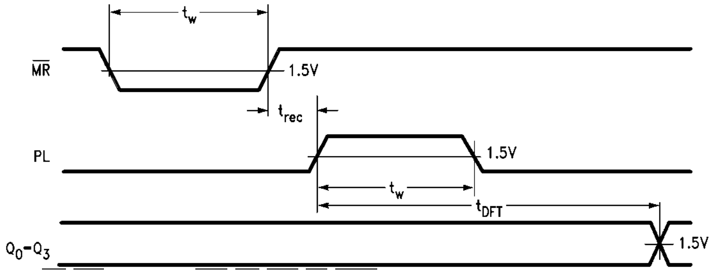
Conditions: Data in stack, TOP HIGH, $\overline{\text{IES}}$ HIGH when initiated

FIGURE 14. Serial Output, Slave Operation



Conditions: $\overline{\text{IES}}$ LOW when initiated, $\overline{\text{OE}}$, $\overline{\text{CPSO}}$ LOW; data available in stack

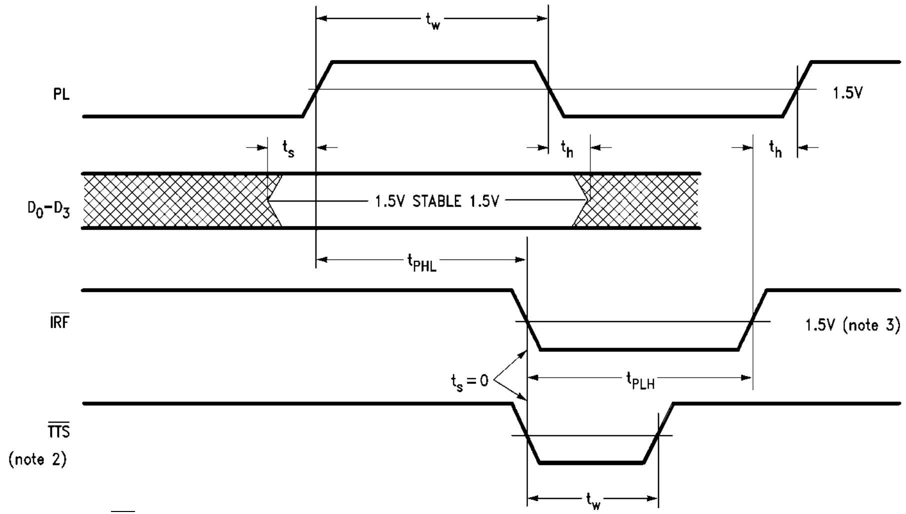
FIGURE 15. Parallel Output, 4-Bit Word or Master in Parallel Expansion



Conditions: $\overline{\text{TTS}}$ connected to $\overline{\text{IRF}}$, $\overline{\text{TOS}}$ connected to $\overline{\text{ORE}}$, $\overline{\text{IES}}$, $\overline{\text{OES}}$, $\overline{\text{OE}}$, $\overline{\text{CPSO}}$ LOW, TOP HIGH

FIGURE 16. Fall Through Time

Timing Waveforms (Continued)

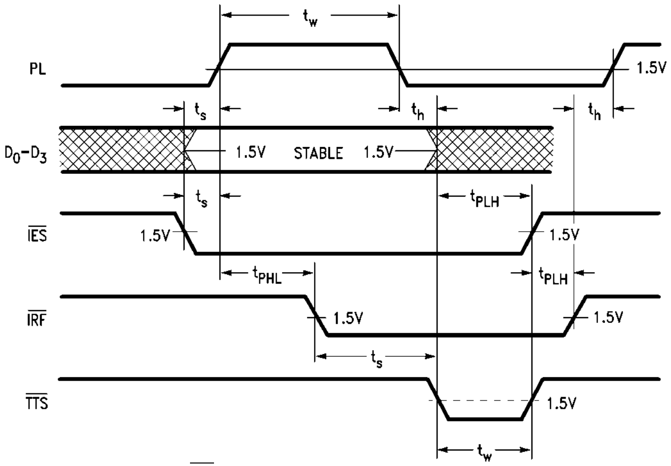


Conditions: Stack not full, $\overline{IES}$ LOW when initialized

NOTE A: $\overline{TTS}$ normally connected to $\overline{IRF}$.

NOTE B: If stack is full, $\overline{IRF}$ will stay LOW.

FIGURE 17. Parallel Load Mode, 4-Bit Word (Unexpanded) or Master in Parallel Expansion

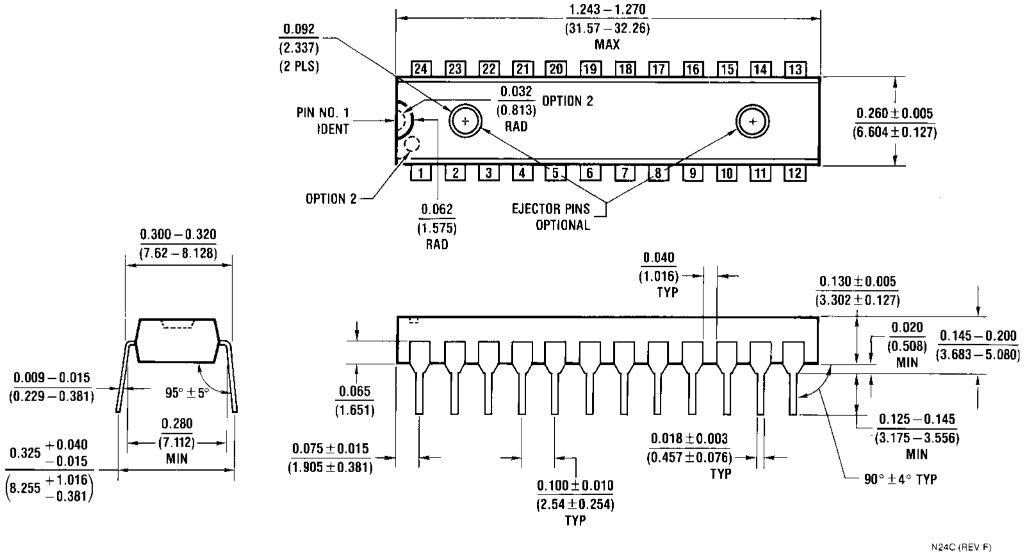


Conditions: Stack not full, device initialized (Note 3) with $\overline{IES}$ HIGH

Note 3: Initialization requires a master reset to occur after power has been applied.

FIGURE 18. Parallel Load, Slave Mode

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N24C

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