82050

Asynchronous Communications Controller

The Intel CHMOS 82050 Asynchronous Communications Controller is a low cost, higher performance alternative to the INS 16450 - it emulates the INS 16450 and provides 100% compatibility with IBM PC software. Its 28-lead package provides all the functionality necessary for an IBM PC environment while substantially decreasing board space requirements. The 82050's simpler system interface reduces TTL glue - especially for higher frequency PC bus designs. The 82050 provides a low cost, high-performance integrated modem solution when combined with Intel's 89024 modem chip set. The compact 28-pin 82050 is fabricated using CHMOS III technology for decreased power consumption and increased reliability.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

82050
ASYNCHRONOUS COMMUNICATIONS CONTROLLER

- **Asynchronous Operation**
  - **— 5- to 8-Bit Character Format**
  - **— Odd-, Even-, or No-Parity Generation and Detection**
  - **— Serial Bit Rate: DC to 56 Kb/s**
- **Programmable, 16-Bit Baud Rate Generator**
- **System Clock**
  - **— On-Chip Crystal Oscillator**
  - **— Externally Generated Clock**
- **28-Lead DIP and PLCC Packages**
- **IBM PC (INS 16450/8250A) Software Compatible**
- **Seven I/O Pins**
  - **— Dedicated Modem I/O**
  - **— General Purpose I/O**
- **No-TTL Interface to Most Intel Processors**
- **Internal Diagnostics with Local Loopback**
- **Complete Interrupt and Status Reporting**
- **CHMOS III Technology Provides Increased Reliability and Reduced Power Consumption**
- **Line Break Generation and Detection**

The Intel CHMOS 82050 Asynchronous Communications Controller is a low cost, higher performance alternative to the INS 16450—it emulates the INS 16450 and provides 100% compatibility with IBM PC software. Its 28-lead package provides all the functionality necessary for an IBM PC environment while substantially decreasing board space requirements. The 82050's simpler system interface reduces TTL glue—especially for higher frequency PC bus designs. The 82050 provides a low cost, high-performance integrated modem solution when combined with Intel's 89024 modem chip set. The compact 28-pin 82050 is fabricated using CHMOS III technology for decreased power consumption and increased reliability.

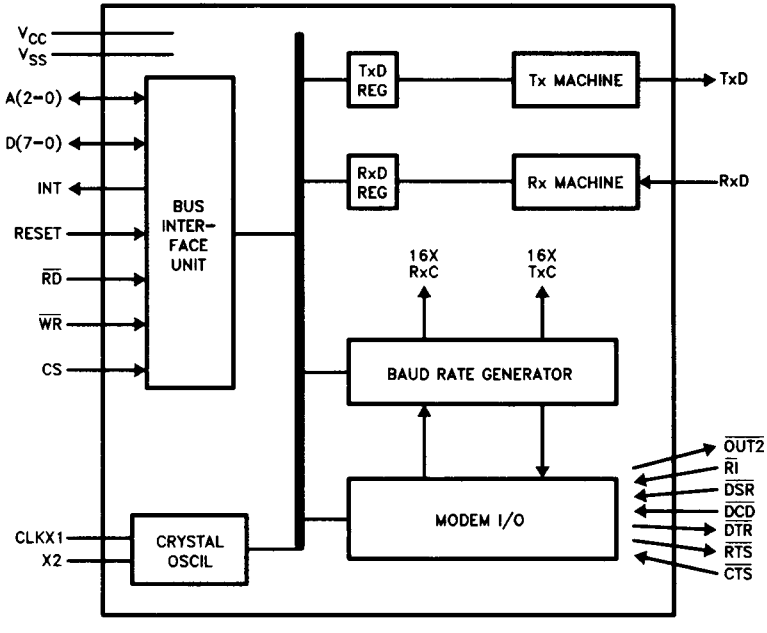


Figure 1. Block Diagram

August 1990
Order Number: 290137-004

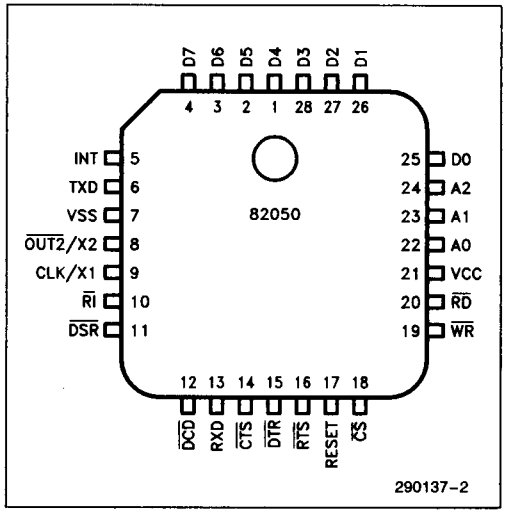


Figure 2. PLCC Pinout

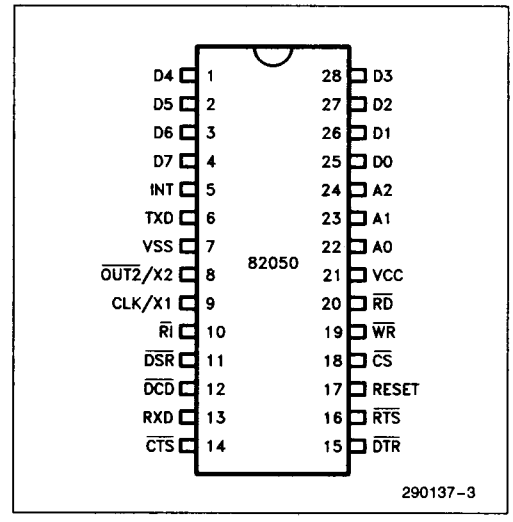


Figure 3. DIP Pinout

2

82050 PINOUT DEFINITION

Symbol	Pin No.	Type	Name and Description
RESET	17	I	**RESET:** A high on this input pin resets the 82050.
$\overline{CS}$	18	I	**CHIP SELECT:** A low on this input pin enables the 82050 and allows read or write operations.
A2–A0	24–22	I	**ADDRESS PINS:** These inputs interface with three bits of the system address bus to select one of the internal registers for read or write.
D7–D0	1–4 25–28	I/O	**DATA BUS:** Bi-directional, three state, 8-Bit Data Bus. These pins allow transfer of bytes between the CPU and the 82050.
$\overline{RD}$	20	I	**READ:** A low on this input pin allows the CPU to read data or status bytes from the 82050.
$\overline{WR}$	19	I	**WRITE:** A low on this input allows the CPU to write data or control bytes to the 82050.
INT	5	O	**INTERRUPT:** A high on this output pin signals an interrupt request to the CPU. The CPU may determine the particular source and cause of the interrupt by reading the 82050 status registers.
CLK/X1	9	I	**MULTIFUNCTION:** This input pin serves as a source for the internal system clock. The clock may be asynchronous to the serial clocks and to the processor clock. This pin may be used in one of two modes: CLK-in this mode an externally generated clock should be used to drive this input pin; X1-in this mode the clock is generated by a crystal to be connected between this pin (X1) and the X2 pin. (See system clock generation.)
$\overline{OUT2}$/X2	8	O	**MULTIFUNCTION:** This is a dual-function pin which may be configured to one of the following functions: $\overline{OUT2}$—a general purpose output pin controlled by the CPU is only available when the CLK/X1 pin is driven by an externally generated clock; X2—this pin serves as an output pin for the crystal oscillator. Note: The configuration of pin is done during hardware reset. For more details refer to the system clock generation.

82050 PINOUT DEFINITION (Continued)

Symbol	Pin No.	Type	Name and Description
TXD	6	O	**TRANSMIT DATA:** Serial data is transmitted via this output pin starting at the least significant bit.
RXD	13	I	**RECEIVE DATA:** Serial data is received on this input pin starting at the least significant bit.
$\overline{RI}$	10	I	**RING INDICATION:** RI - Ring indicator—input, active low. This is a general purpose input accessible by the CPU.
$\overline{DTR}$	15	O	**$\overline{DTR}$—DATA TERMINAL READY:** Output, active low. This is a general purpose output pin controlled by the CPU. During hardware reset, this pin is an input used to determine the system clock mode. (See System Clock Generation.)
$\overline{DSR}$	11	I/O	**$\overline{DSR}$—DATA SET READY:** Input, active low. This is a general purpose input pin accessible by the CPU.
$\overline{RTS}$	16	O	**$\overline{RTS}$—REQUEST TO SEND:** Output, active low. This is a general purpose output pin controlled by the CPU. During hardware reset, this pin is an input used to determine the system clock mode. (See system clock generation)
$\overline{CTS}$	14	I	**CLEAR TO SEND:** Input active low. This is a general purpose input pin accessible by the CPU.
$\overline{DCD}$	12	I/O	**$\overline{DCD}$—DATA CARRIER DETECTED:** Input, active low. This is a general purpose input pin accessible by the CPU.
VCC	21	P	**VCC:** Device power supply.
VSS	7	P	**VSS:** Ground.

SYSTEM INTERFACE

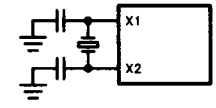
The 82050 has a simple demultiplexed bus interface which consists of a bidirectional, three-state, 8-bit data bus and a 3-bit address bus. The Reset, Chip Select, Read, and Write pins, along with the Interrupt pin, provide the remaining signals necessary to interface to the CPU. The 82050's system clock can be generated externally and provided through the CLK pin; or its on-chip crystal oscillator can be used by attaching a crystal to the X1 and X2 pins. For compatibility with IBM PC software, a system clock of 18.432 MHz (with divide by two enabled) is recommended. The 82050, along with a transceiver, address decoder, and a crystal, complete the interface to the IBM PC Bus.

SYSTEM CLOCK OPTIONS

The 82050 has two modes of system clock operation. It can accept an externally generated clock, or use a crystal to internally generate its system clock by using the on-chip oscillator.

The 82050 has an on-chip oscillator which can be used to generate its system clock. The oscillator will take the input from a crystal attached to the X1 and X2 pins. The oscillator frequency is divided by two before being inputted into the chip circuitry. If an 18.432 MHz crystal is used, then the actual system clock frequency of the 82050 will be 9.216 MHz. This mode is configured via a strapping option on the $\overline{RTS}$ pin.

CRYSTAL OSCILLATOR



290137-4

Parallel Resonant Crystal Freq. Max = 18.432 MHz (Divided by 2)

Figure 4. Crystal Oscillator

It is very important to distinguish between the clock frequency being supplied into the 82050 and the system clock frequency. The term system clock refers to the clock frequency being supplied to the 82050 circuitry (divided or undivided). The following examples delineate the three options for clock usage and their effect on the 82050 system clock as well as on the BRG source frequency:

1. **Crystal Oscillator:** (Maximum 18.432 MHz)
   - — System Clock Frequency = Crystal Frequency/2
   - — BRG Source Clock Frequency = Crystal Frequency/10
2. **External Clock (Divide by Two Enabled):** (Maximum 18.432 MHz)
   - — System Clock Frequency = External Clock Frequency/2
   - — BRG Source Clock Frequency = External Clock Frequency/10
3. **External Clock (Divide by Two Disabled):** (Maximum 9.216 MHz)
   - — System Clock Freq. = External Clock Frequency
   - — BRG Source Clock Freq. = External Clock Frequency/5

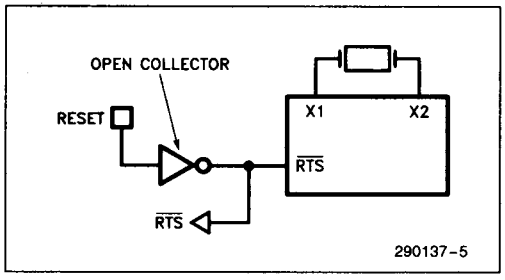


Figure 5. Strapping

During the power up or reset the $\overline{RTS}$ pin is an input; it is weakly pulled high internally and sampled by the falling edge of reset. If it is driven low externally, then the 82050 is configured for a crystal oscillator; otherwise an externally generated clock is expected.

EXTERNALLY GENERATED SYSTEM CLOCK

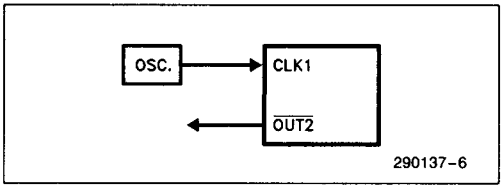


Figure 7. External Clock

This is the default mode of system clock operation. The system clock is divided by two; however, the user may disable the divide by two by a hardware strapping option on the $\overline{DTR}$ pin. The strapping option is similar to the one used on the $\overline{RTS}$ pin.

NOTE:
The use of the Divide by Two strapping option in the crsytal oscillator mode is forbidden.

BAUD RATE GENERATION

The 82050 has a programmable 16-bit Baud Rate Generator (BRG). The 16X baud rate is generated by dividing the source clock with the divisor count from the BRG divisor registers (BAL, BAH). The BRG source clock is the 82050 system clock divided by five. If using an actual 82050 system clock of 9.216 MHz, then the BRG source clock will be 9.216 MHz/5 = 1.8432 MHz, which is compatible with the BRG source clock fed into the IBM PC serial port BRG. This allows the 82050, while using a faster system clock, to maintain full compatibility with software divisor calculations based on the 1.8432 MHz clock used in the IBM PC.

2

RESET

The 82050 can be reset by asserting the RESET pin. The RESET pin must be held high for at least 8 system clock cycles. If using crystal oscillator, a reset pulse at least 1 ms should be used to ensure oscillator start up. Upon reset, all 82050 registers (except TXD and RXD) are returned to their default states. During reset, the 82050's system clock mode of operation is also selected by strapping options on the RTS and DTR pins (see system clock generation).

INTERRUPTS

The INT pin will go high, or active, whenever one of the following conditions occurs provided it is enabled in the interrupt enable register (IER):

a. Receive Machine Error or Break Condition
b. Receive Data Available
c. Transmit Data Register Empty
d. Change in the State of the Modem Input Pins

The INT pin will be reset (low) when the interrupt source is serviced. The Interrupt Identification Register (IIR) along with the Line Status Register (LSR) and the Modem Status Register (MSR) can be used to identify the source requesting service. The IIR register identifies one of the four conditions listed above. The particular event or status, which triggers the interrupt mechanism, can be identified by reading either the Line Status Register or the Modem Status register. If multiple interrupt sources become active at any one time, then highest priority interrupt source is reflected in the IIR register when the interrupt pin becomes active. Once the highest priority interrupt is serviced, then the next highest priority

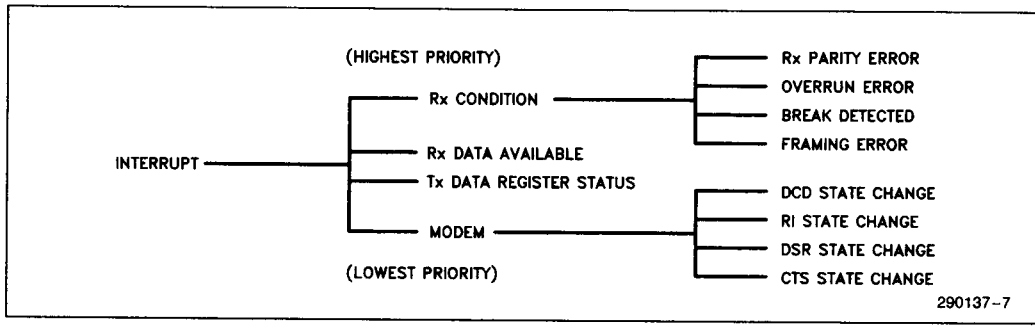


Figure 8. Interrupt Structure

interrupt source is decoded into the IIR register; the whole procedure is repeated until there are no more pending interrupt sources.

TRANSMIT

The 82050 transmission mechanism involves the TX Machine and the TXD Register. The TX Machine reads characters from the TXD Register, serializes the bits, and transmits them over the TXD pin according to signals provided for transmission by the Baud Rate Generator. It also generates parity, and break transmissions upon CPU request.

RECEIVE

The 82050 reception mechanism involves the RX Machine and the RXD Register. The RX Machine assembles the incoming characters, and loads them onto the RXD Register. The RX Machine synchronizes the data, passes it through a digital filter to filter out spikes, and then uses three samples to generate the bit polarity.

The falling edge of the start bit triggers the RX Machine, which then starts sampling the RXD input (3 samples). If the samples do not indicate a start bit, then a false start bit is determined and the RX Machine returns to the start bit search mode. Once a start bit is detected, the RX Machine starts sampling for data bits.

If the RXD input is low for the entire character time, including stop bits, then the RX Machine sets Break Detect and Framing Error bits in the Line Status Register (LSR). It loads a NULL character into the RXD register. The RX Machine then enters the idle state. When it detects a MARK it resumes normal operation.

SOFTWARE INTERFACE

Like other I/O based peripherals, the 82050 is programmed through its registers to support a variety of functions. The 82050 register set is identical to the 16450 register set to provide compatibility with software written for the IBM PC. The 82050 register set occupies eight addresses and includes control, status, and data registers. The three address lines and the Divisor Latch Access Bit are used to select the 82050 registers.

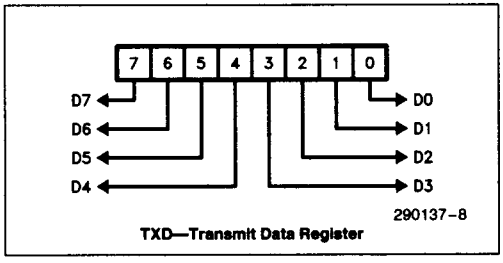
REGISTER DESCRIPTION

Register Map										
Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Address**	**Default**
TxD	Tx Data Bit 7	Tx Data Bit 6	Tx Data Bit 5	Tx Data Bit 4	Tx Data Bit 3	Tx Data Bit 2	Tx Data Bit 1	Tx Data Bit 0	0	—
RxD	Rx Data Bit 7	Rx Data Bit 6	Rx Data Bit 5	Rx Data Bit 4	Rx Data Bit 3	Rx Data Bit 2	Rx Data Bit 1	Rx Data Bit 0	0	—
BAL	BRGA LSB Divide Count (DLAB = 1)								0	02H
BAH	BRGA MSB Divide Count (DLAB = 1)								1	00H
IER	0	0	0		Modem Interrupt Enable	Rx Machine Interrupt Enable	Tx Data Interrupt Enable	Rx Data Interrupt Enable	1	00H
IIR	0	0	0	0	0	Active Interrupt Bit 1	Active Interrupt Bit 0	Interrupt Pending	2	01H
LCR	DLAB Divisor Latch Access Bit	Set Break	Parity Mode Bit 2	Parity Mode Bit 1	Parity Mode Bit 0	Stop Bit Length Bit 0	Character Length Bit 1	Character Length Bit 0	3	00H
MCR	0	0	0	Loopback Control Bit	OUT2 Complement	0	RTS Complement	DTR Complement	4	00H
LSR	0	TxM Status	TxD Empty	Break Detected	Framing Error	Parity Error	Overrun Error	Rx Data Available	5	60H
MSR	DCD Input Inverted	RI Input Inverted	DSR Input Inverted	CTS Input Inverted	State Change in DCD	State (H → L) Change in RI	State Change in DSR	State Change in CTS	6	00H
SCR	Scratch-Pad Register								7	00H

Figure 9. Register Description Table

TRANSMIT DATA REGISTER (TXD)

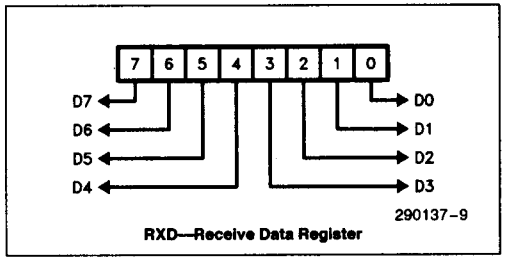
This register holds the next data byte to be transmitted. When the transmit shift register becomes empty, the contents of the Transmit Data Register are loaded into the shift register and the Transmit Data Register Empty condition becomes true.



TXD—Transmit Data Register

RECEIVE DATA REGISTER (RXD)

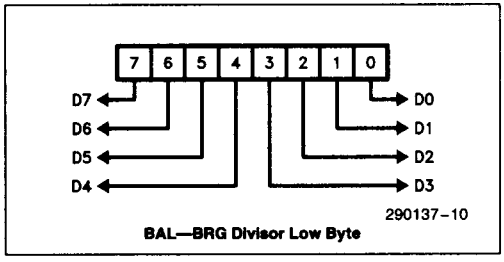
This register holds the last character received by the RX Machine. The character is right justified and the leading bits are zeroed. Reading the register empties the register and resets the Received Character Available condition.



RXD—Receive Data Register

BRG DIVISOR LOW BYTE (BAL)

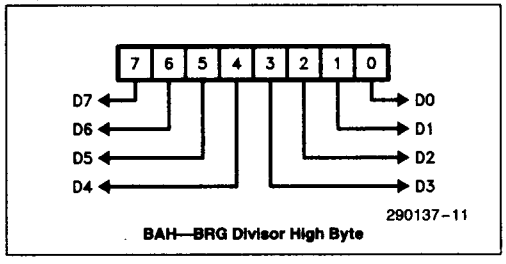
This register contains the least significant byte of the Baud Rate Generator's 16-bit divisor. This register is accessible only when the DLAB bit is set in the LCR register.



BAL—BRG Divisor Low Byte

BRG DIVISOR HIGH BYTE (BAH)

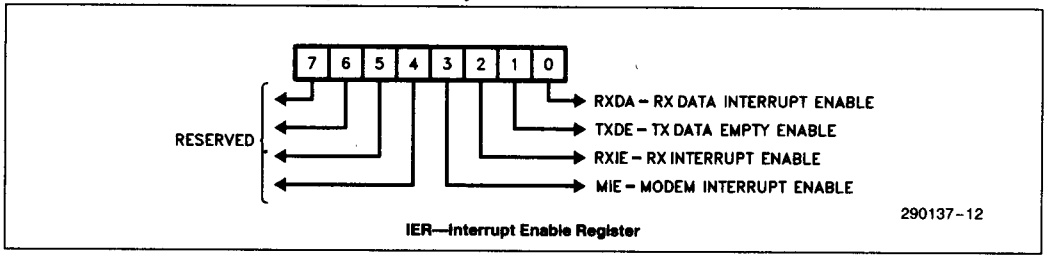
This register contains the most significant byte of the Baud Rate Generator's 16-bit divisor. This register is accessible ony when the DLAB bit is set in the LCR register.



BAH—BRG Divisor High Byte

INTERRUPT ENABLE REGISTER (IER)

This register enables four types of interrupts which independently activate the INT pin. Each of the four interrupt types can be disabled by resetting the appropriate bit of the IER register. Similarly by setting the appropriate bits, selected interrupts can be enabled. If all interrupts are disabled, then the interrupt requests are inhibited from the IIR register and the INT pin. All other functions, including Status Register and the Line Status Register bits continue to operate normally.



IER—Interrupt Enable Register

MIE—MODEM Interrupt Enable

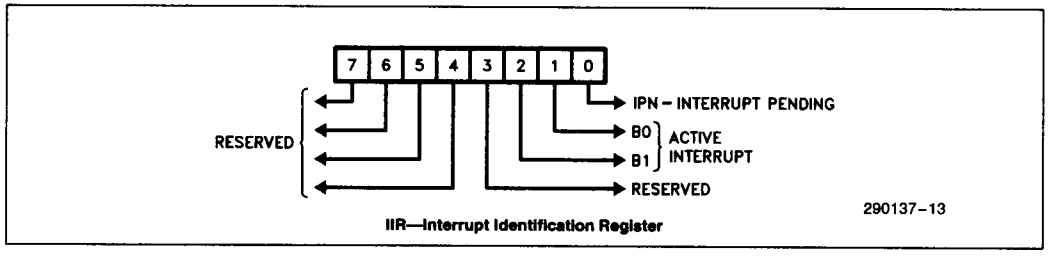
RXIE—RX Machine Interrupt Enable

TXDE—TX Data Register Empty

RXDA—RX Data Available

INTERRUPT IDENTIFICATION REGISTER (IIR)

This register holds the highest priority enabled and active interrupt request. The source of the interrupt request can be identified by reading bits 2-1.



IIR—Interrupt Identification Register

B1, B0—Interrupt Bits, 2-1. These two bits reflect the highest priority, enabled and pending interrupt request.

11: RX Error Condition (Highest Priority)

10: RX Character Available

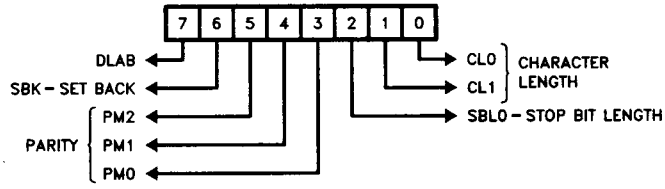
01: TXD Register Empty

00: Modem Interrupt (Lowest Priority)

IPN—Interrupt Pending—This bit is active low, and indicates that there is an interrupt pending. The interrupt logic asserts the INT pin as soon as this bit goes active (NOTE: the IIR register is continuously updated; so while the user is serving one interrupt source, a new interrupt with higher priority may enter IIR and replace the older interrupt vector).

LINE CONTROL REGISTER (LCR)

This is a read/write register which defines the basic configuration of the serial link.



LCR-Line Configure Register

DLAB—Divisor Latch Access Bit—This bit, when set, allows access to the Divisor Count Registers BAL and BAH.

SBK—Set Break—This will force the TXD pin low. The TXD pin will remain low until this bit is reset.

PM2—PM0—Parity Mode Bits—These three bits are used to select the various parity modes of the 82050.

PM0	PM2	PM1	Function
0	X	X	No Parity
1	0	0	Odd Parity
1	0	1	Even Parity
1	1	0	High Parity
1	1	1	Low Parity

SBL—Stop Bit Length—This bit defines the Stop Bit lengths for transmission. The RX Machine can identify 3/4 stop bit or more.

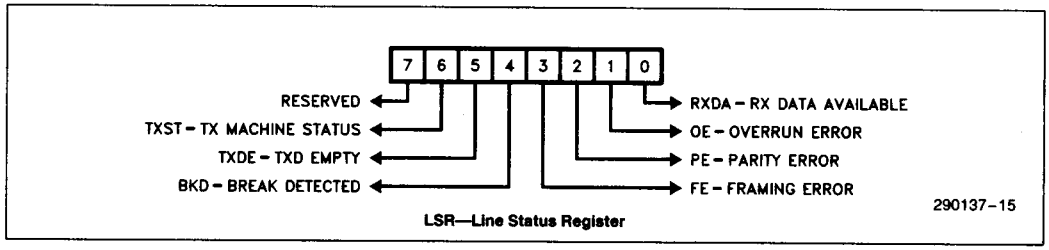
SBL	Character Length	Stop Bit Length
0	X	1
1	5-Bit	1 1/2
1	(6, 7, or 8-Bit)	2

CL0—CL1—Character Length—These bits define the character length used on the serial link.

CL1	CL0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

LINE STATUS REGISTER (LSR)

This register holds the status of the serial link. When read, all bits of the register are reset to zero.



LSR—Line Status Register

RXDA—RX Data Available—This bit, indicates that the RXD register has data available for the CPU to read.

OE—Overrun Error—Indicates that a received character was lost because the RXD register was not empty.

PE Parity Error—Indicates that a received character had a parity error.

FE—Framing Error—Indicates that a received character had a framing error.

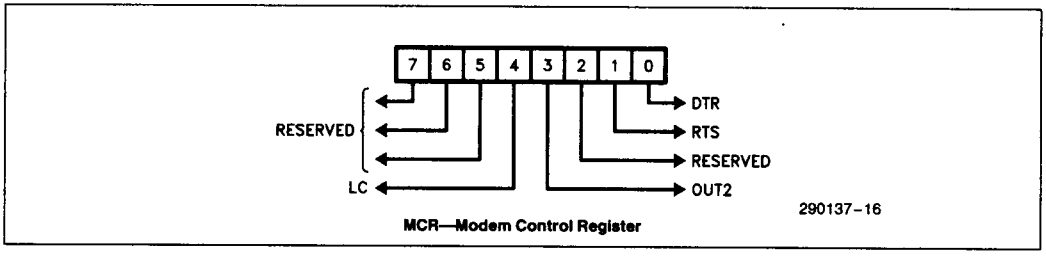
BkD—Break Detected—This bit indicates that a break condition was detected, i.e., RxD input was held low for two character times.

TXDE—TXD Empty—This indicates that the 82050 is ready to accept a new character for transmission. In addition, this bit causes an interrupt request to be generated if the TXD register Empty interrupt is enabled.

TXST—TX Machine Status—When set, this bit indicates that the TX Machine is Empty, i.e., both the TXD register and the TX Shift Register are empty.

MODEM CONTROL REGISTER (MCR)

This register controls the modem output pins. All the outputs invert the data, i.e., their output will be the complement of the data written into this register.



MCR—Modem Control Register

LC—Loopback Control—This bit puts the 82050 into a Local Loopback mode.

OUT2—OUT2 Output—This bit controls the $\overline{OUT2}$ pin. The output signal is the complement of this bit.

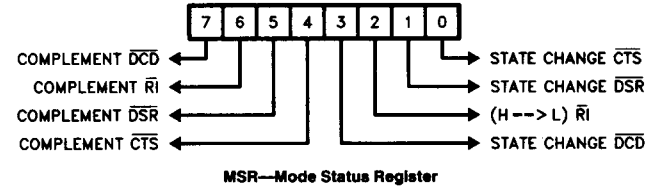
NOTE:
This bit is only effective when the 82050 is being used with an externally generated clock.

RTS—RTS Output Bit—This bit controls the $\overline{RTS}$ pin. The output signal is the complement of this bit.

DTR—DTR Output Bit—This bit controls the $\overline{DTR}$ pin. The output signal is the complement of this bit.

MODEM STATUS REGISTER (MSR)

This register holds the status of the modem input pins ($\overline{CTS}$, DCD, DSR, RI). It is the source of Modem interrupts (bits 3–0) when enabled in the IER register. If any of the above input pins change levels, then the appropriate bit in MSR is set. Reading MSR will clear the status bits.



MSR—Mode Status Register

DCDC—DCD Complement—Holds the complement of the $\overline{DCD}$ pin.

DRIC—RI Complement—Holds the complement of the $\overline{RI}$ pin.

DSRC—DSR Complement—Holds the complement of the $\overline{DSR}$ pin.

CTSC—CTS Complement—Holds the complement of the $\overline{CTS}$ pin.

DDCD—Delta DCD—Indicates that the $\overline{DCD}$ pin has changed state since this register was last read.

DRI—Delta RI—Indicates that the $\overline{RI}$ pin has changed state from high to low since this register was last read.

DDSR—Delta DSR—Indicates that the $\overline{DSR}$ pin has changed state since this register was last read.

DCTS—Delta CTS—Indicates that the $\overline{CTS}$ pin has changed state since this register was last read.

SCRATCHPAD REGISTER (SCR)

The 8-bit Read/Write register does not control the ACC. It is intended as a scratch pad register for use by the programmer.

SPECIFICATIONS

D.C. SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias .....0°C to 70°C
Storage Temperature .....−65°C to +150°C
Voltage on any Pin (w.r.t. V_{SS} . −0.5V to V_{CC} + 0.5V
Voltage on V_{CC} Pin (w.r.t. V_{SS}).....−0.5V to +7V
Power Dissipation.....300 mW

D.C. CHARACTERISTICS (T_A = 0° TO 70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Notes	Min	Max	Units
V_{IL}	Input Low Voltage	(1)	−0.5	0.8	V
V_{IH}	Input High Voltage	(1), (7)	2.0	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	(2), (9)		0.45	V
V_{OH}	Output High Voltage	(3), (9)	2.4		V
I_{LI}	Input Leakage Current	(4)		±10	μA
I_{LO}	3-State Leakage Current	(5)		±10	μA
I_{OHR}	Input High for $\overline{DTR}$, $\overline{RTS}$	(10)		0.4	mA
I_{OLR}	Input Low for $\overline{DTR}$, $\overline{RTS}$	(10)	11		mA
L_{XTAL}	X1, X2 Load			10	pF
I_{CC}	Power Supply Current	(6)		3.8 35	mA/MHz mA (max)
C_{in}	Input Capacitance	(8)		10	pF
C_{io}	I/O Capacitance	(8)		10	pF
C_{XTAL}	X_1, X_2 Load			10	pF

NOTES:
1. Does not apply to CLK/X1 pin, when configured as crystal oscillator input (X1).
2. @ I_{ol} = 2 mA.
3. @ I_{oh} = −0.4 mA.
4. $0 < V_{in} < V_{CC}$.
5. $0.45V < V_{out} < (V_{CC} - 0.45)$.
6. V_{CC} = 5.5V; V_{il} = 0.5V (max); $V_{ih} = V_{CC} - 0.5V$ (min); $I_{ol} = I_{oh} = 0$; 9.2 MHz (max).
7. V_{IH} = 2.4V on $\overline{RD}$ and RXD pins.
8. Freq = 1 MHz.
9. Does not apply OUT2/X2 pin, when configured as crystal oscillator output (X2).
10. Input current for $\overline{DTR}$, $\overline{RTS}$ pins during Reset for Clock Mode Configuration.

A.C. SPECIFICATIONS

Testing Conditions:

- All AC output parameters are under output load of 20 to 100 pF, unless otherwise specified.
- AC testing inputs are driven at 2.4 for logic '1', and 0.45V for logic '0'. Output timing measurements are made at 1.5V for both a logical '0' and '1'.
- In the following tables, the units are ns, unless otherwise specified.

System Interface Specification—System Clock Specification:

The 82050 system clock is supplied via the CLK pin or generated by on-chip crystal oscillator. The clock is optionally divided by two. The CLK parameters are given separately for internal divide-by-two option ACTIVE and INACTIVE.

The system clock (after division by two, if active) must be at least 16X the Tx or Rx baud rate (the faster of the two).

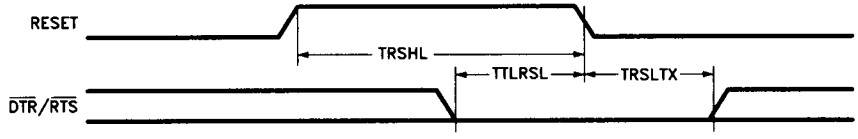
SYSTEM CLOCK SPECIFICATIONS

Symbol	Parameter	Min	Max	Notes
DIVIDE BY TWO OPTION—ACTIVE				
Tcy/2	CLK Period	54	250	(2)
TCLCH	CLK Low Time	25		
TCHCL	CLK High Time	25		
TCH1CH2	CLK Rise Time		10	(1)
TCL2CL1	CLK Fall Time		10	(1)
FXTAL	External Crystal Frequency Rating	4.0	18.432 MHz	
DIVIDE BY TWO OPTION—INACTIVE				
Tcy	CLK Period	108		
TCLCH	CLK Low Time	54		
TCHCL	CLK High Time	44	250	
TCH1CH2	CLK Rise Time		15	(1)
TCL2CL1	CLK Fall Time		15	(1)

NOTES:
1. Rise/fall times are measured between 0.8 and 2.0V.
2. Tcy in ACTIVE divide by two option is TWICE the input clock period.

RESET SPECIFICATION

Symbol	Parameter	Min	Max	Notes
TRSHL	Reset Width—CLK/X1 Configured to CLK	8 Tcy		(1)
TTLRSL	RTS/DTR LOW Setup to Reset Inactive	6 Tcy		(2)
TRSLTX	RTS/DTR Low Hold after Reset Inactive	0	Tcy − 20	(2)



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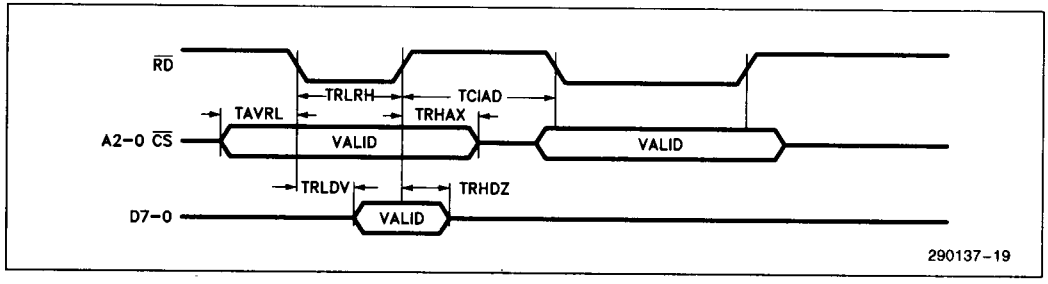
NOTES:
1. In case of CLK/X1 configured as X1, additional time is required to guarantee crystal oscillator wake-up.
2. RTS/DTR are internally driven HIGH during RESET active time. The pin should be either left OPEN or externally driven LOW during RESET according to the required configuration of the system clock. These parameters specify the timing requirements on these pins, in case they are externally driven LOW during RESET. The maximum spec on TRSLTX requires that the RTS/DTR pins not be forced later than TRSLTX maximum.

READ CYCLE SPECIFICATIONS

Symbol	Parameter	Min	Max	Notes
TRLRH	$\overline{RD}$ Active Width	2 Tcy + 65		
TAVRL	Address/$\overline{CS}$ Setup Time to $\overline{RD}$ Active	7		
TRHAX	Address/$\overline{CS}$ Hold Time after $\overline{RD}$ Inactive	0		
TRLDV	Data Out Valid after $\overline{RD}$ Active		2Tcy + 65	(1)
TCIAD	Command Inactive to Active Delay	Tcy + 15		(2)
TRHDZ	Data Out Float Delay after $\overline{RD}$ Inactive		40	

NOTES:
1. C1 = 20 pF to 100 pF.
2. Command refers to either Read or Write signals.



WRITE CYCLE SPECIFICATION

Symbol	Parameter	Min	Max	Notes
TWLWH	$\overline{WR}$ Active Width	2Tcy + 15		
TAVWL	Address $\overline{CS}$ Setup Time to $\overline{WR}$ Active	7		
TWHAX	Address and $\overline{CS}$ Hold Time after $\overline{WR}$	0		
TDVWH	Data in Setup Time to $\overline{WR}$ Inactive	90		
TWHDX	Data in Hold Time after $\overline{WR}$ Inactive	12