

93L422

256 x 4-Bit Static RAM

The 93L422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits. It is designed for high speed cache, control and buffer storage applications. The 93L422 is available in two speeds, “standard” speed and an “A” grade. The device includes full on-chip decoding, separate Data inputs and non-inverting Data outputs, as well as two Chip Select lines.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer’s datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. ‘Typical’ values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

93L422 256 x 4-Bit Static Random Access Memory

Memory and High Speed Logic

Description

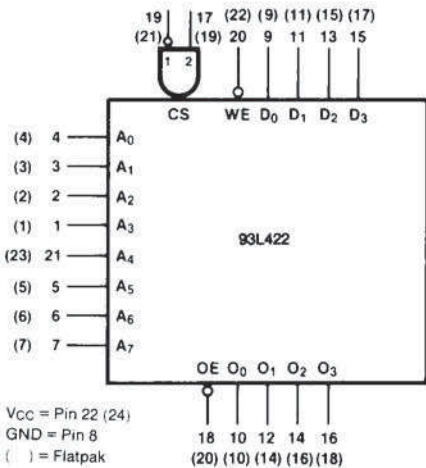
The 93L422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits. It is designed for high speed cache, control and buffer storage applications. The 93L422 is available in two speeds, "standard" speed and an "A" grade. The device includes full on-chip decoding, separate Data inputs and non-inverting Data outputs, as well as two Chip Select lines.

- **Commercial Address Access Time**
 93L422 — 60 ns Max
 93L422A — 45 ns Max
- **Military Address Access Time**
 93L422 — 75 ns Max
 93L422A — 55 ns Max
- **Fully TTL Compatible**
- **Features Three State Outputs**
- **Power Dissipation — 0.25 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

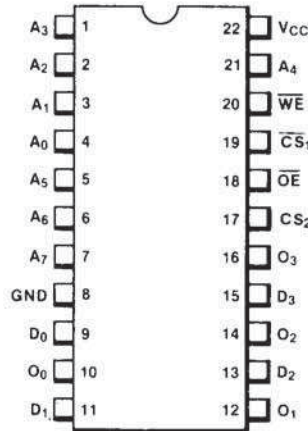
Pin Names

| | |
|--------------------------------|----------------------------------|
| A ₀ -A ₇ | Address Inputs |
| D ₀ -D ₃ | Data Inputs |
| CS ₁ | Chip Select Input (Active LOW) |
| CS ₂ | Chip Select Input (Active HIGH) |
| WE | Write Enable Input (Active LOW) |
| OE | Output Enable Input (Active LOW) |
| O ₀ -O ₃ | Data Outputs |

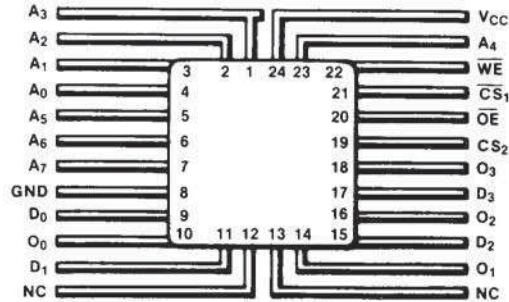
Logic Symbol



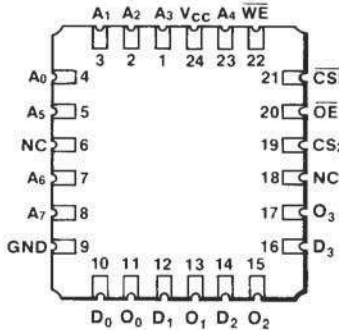
Connection Diagrams
22-Pin DIP (Top View)



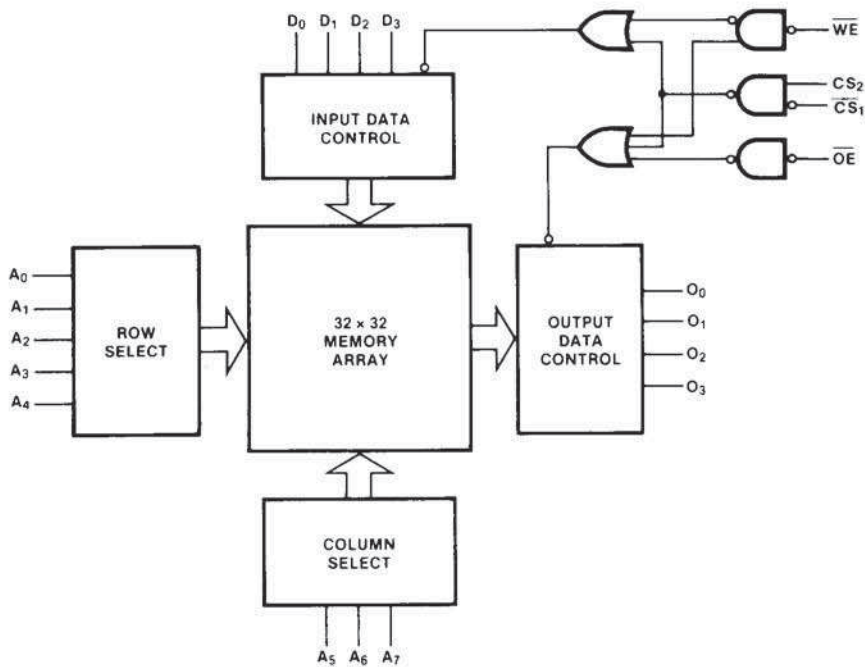
24-Pin Flatpak (Top View)



24-Pin Leadless Chip Carrier (Top View)



Logic Diagram

**Functional Description**

The 93L422 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 through A_7 .

Two Chip Select inputs, inverting and non-inverting, are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of the chip selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable (\overline{WE}) input. When \overline{WE} is

held LOW and the chip is selected, the data at D_0 - D_3 is written into the addressed location. Since the write function is level-triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, \overline{WE} is held HIGH and the chip selected. Non-inverted data is then presented at the outputs (O_0 - O_3).

The 93L422 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

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Truth Table

| Inputs | | | | Outputs | Mode |
|-----------------|-------------------|--------|-----------------|-----------|-----------------|
| \overline{OE} | \overline{CS}_1 | CS_2 | \overline{WE} | 3-State | |
| X | H | X | X | HIGH Z | Not Selected |
| X | X | L | X | HIGH Z | Not Selected |
| L | L | H | H | D_{OUT} | READ |
| X | L | H | L | HIGH Z | WRITE |
| H | X | X | X | HIGH Z | Output Disabled |

H = HIGH Voltage Level (2.4 V)
 L = LOW Voltage Level (.5 V)
 X = Don't Care (HIGH or LOW)
 High Z = High-Impedance

DC Performance Characteristics: Over operating temperature ranges (Note 1)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|------------------------|--|-----|------|-----------|---------------|--|
| V_{OL} | Output LOW Voltage | | 0.3 | 0.45 | V | $V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$ |
| V_{IH} | Input HIGH Voltage | 2.1 | 1.6 | | V | Guaranteed Input HIGH Voltage for All Inputs ⁵ |
| V_{IL} | Input LOW Voltage | | 1.5 | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs ⁵ |
| V_{OH} | Output HIGH Voltage | 2.4 | | | V | $V_{CC} = \text{Min}, I_{OH} = -5.2 \text{ mA}$ |
| I_{IL} | Input LOW Current | | -150 | -300 | μA | $V_{CC} = \text{Max}, V_{IN} = 0.4 \text{ V}$ |
| I_{IH} | Input HIGH Current | | 1.0 | 40 | μA | $V_{CC} = \text{Max}, V_{IN} = 4.5 \text{ V}$ |
| I_{IHB} | Input Breakdown Current | | | 1.0 | mA | $V_{CC} = \text{Max}, V_{IN} = V_{CC}$ |
| V_{IC} | Input Diode Clamp Voltage | | -1.0 | -1.5 | V | $V_{CC} = \text{Max}, I_{IN} = -10 \text{ mA}$ |
| I_{OZH} I_{OZL} | Output Current (HIGH Z) | | | 50 -50 | μA | $V_{CC} = \text{Max}, V_{OUT} = 2.4 \text{ V}$ $V_{CC} = \text{Max}, V_{OUT} = 0.5 \text{ V}$ |
| I_{OS} | Output Current Short Circuit to Ground | -10 | | -70 | mA | $V_{CC} = \text{Max}, \text{Note 3}$ |
| I_{CC} | Power Supply Current | | | 80 90 | mA | Commercial Military $V_{CC} = \text{Max}$ All Inputs GND All Outputs Open |

Notes

- Typical values are at $V_{CC} = 5.0 \text{ V}$, $T_C = +25^\circ\text{C}$ and maximum loading.
- The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
- Short circuit to ground not to exceed one second.
- t_W measured at $t_{WSA} = \text{Min}$, t_{WSA} measured at $t_W = \text{Min}$.
- Static condition only.

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Commercial

AC Performance Characteristics: $V_{CC} = 5.0\text{ V} \pm 5\%$, $GND = 0\text{ V}$, $T_C = 0^\circ\text{C to } +75^\circ\text{C}$

| Symbol | Characteristic | A | | Std | | Unit | Condition |
|---------------------|---|-----|-----|-----|-----|------|--------------------|
| | | Min | Max | Min | Max | | |
| Read Timing | | | | | | | |
| tACS | Chip Select Access Time | | 30 | | 35 | ns | Figures 3a, 3b, 3c |
| tzRCS | Chip Select to HIGH Z | | 30 | | 35 | ns | |
| tAOS | Output Enable Access Time | | 30 | | 35 | ns | |
| tzROS | Output Enable to HIGH Z | | 30 | | 35 | ns | |
| tAA | Address Access Time ² | | 45 | | 60 | ns | |
| Write Timing | | | | | | | |
| tw | Write Pulse Width to Guarantee Writing ⁴ | 30 | | 45 | | ns | Figure 4 |
| twSD | Data Setup Time Prior to Write | 5 | | 5 | | ns | |
| tWHD | Data Hold Time after Write | 5 | | 5 | | ns | |
| tWSA | Address Setup Time Prior to Write ⁴ | 5 | | 5 | | ns | |
| tWHA | Address Hold Time after Write | 5 | | 5 | | ns | |
| twSCS | Chip Select Setup Time Prior to Write | 5 | | 5 | | ns | |
| tWHCS | Chip Select Hold Time after Write | 5 | | 5 | | ns | |
| tzWS | Write Enable to HIGH Z | | 35 | | 40 | ns | |
| tWR | Write Recovery Time | | 40 | | 45 | ns | |

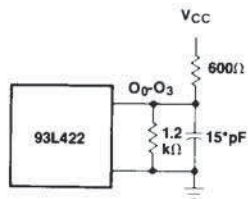
Military

AC Performance Characteristics: $V_{CC} = 5.0\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_C = -55^\circ\text{C to } +125^\circ\text{C}$

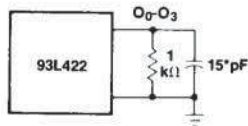
| Symbol | Characteristic | A | | Std | | Unit | Condition |
|---------------------|---|-----|-----|-----|-----|------|--------------------|
| | | Min | Max | Min | Max | | |
| Read Timing | | | | | | | |
| tACS | Chip Select Access Time | | 40 | | 45 | ns | Figures 3a, 3b, 3c |
| tzRCS | Chip Select to HIGH Z | | 40 | | 45 | ns | |
| tAOS | Output Enable Access Time | | 40 | | 45 | ns | |
| tzROS | Output Enable to HIGH Z | | 40 | | 45 | ns | |
| tAA | Address Access Time ² | | 55 | | 75 | ns | |
| Write Timing | | | | | | | |
| tw | Write Pulse Width to Guarantee Writing ⁴ | 40 | | 55 | | ns | Figure 4 |
| twSD | Data Setup Time Prior to Write | 5 | | 5 | | ns | |
| tWHD | Data Hold Time after Write | 5 | | 5 | | ns | |
| tWSA | Address Setup Time Prior to Write ⁴ | 5 | | 5 | | ns | |
| tWHA | Address Hold Time after Write | 5 | | 5 | | ns | |
| twSCS | Chip Select Setup Time Prior to Write | 5 | | 5 | | ns | |
| tWHCS | Chip Select Hold Time after Write | 5 | | 5 | | ns | |
| tzWS | Write Enable to HIGH Z | | 45 | | 45 | ns | |
| tWR | Write Recovery Time | | 50 | | 50 | ns | |

Notes on preceding page

Fig. 1 AC Test Output Load



LOAD A



LOAD B

*Includes jig and probe capacitance
 Note: Load A is used for all production testing.

Fig. 2 AC Test Input Levels

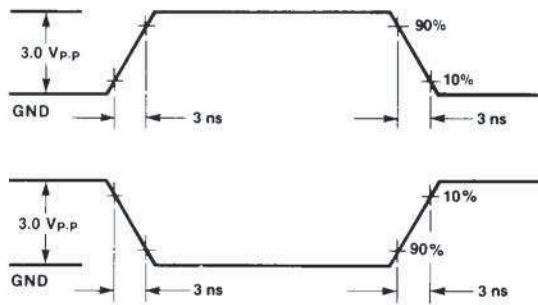
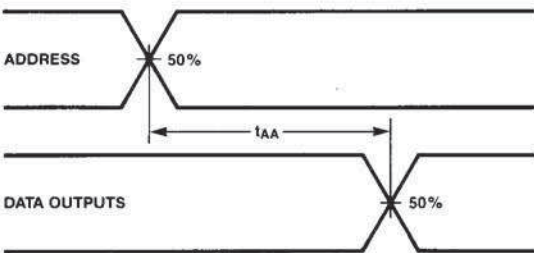
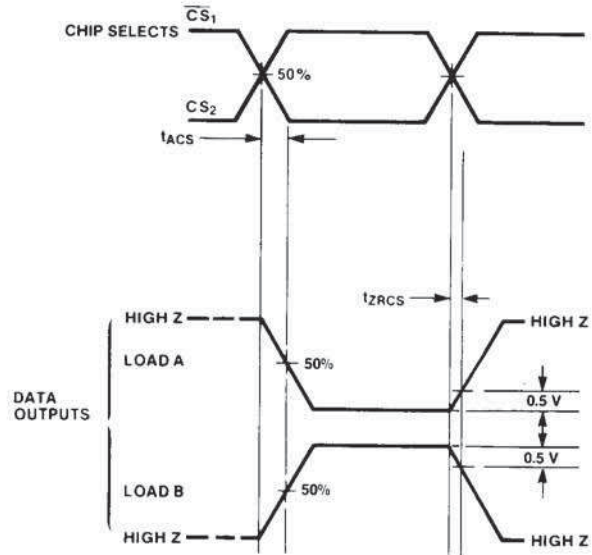


Fig. 3 Read Mode Timing

3a Read Mode Propagation Delay from Address

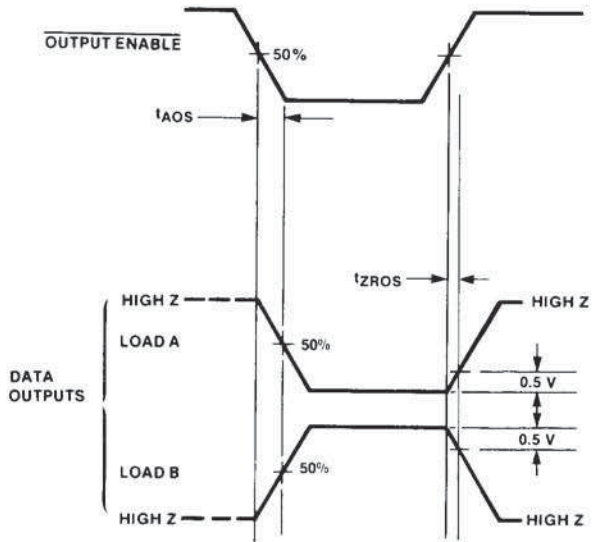


3b Read Mode Propagation Delay from Chip Select



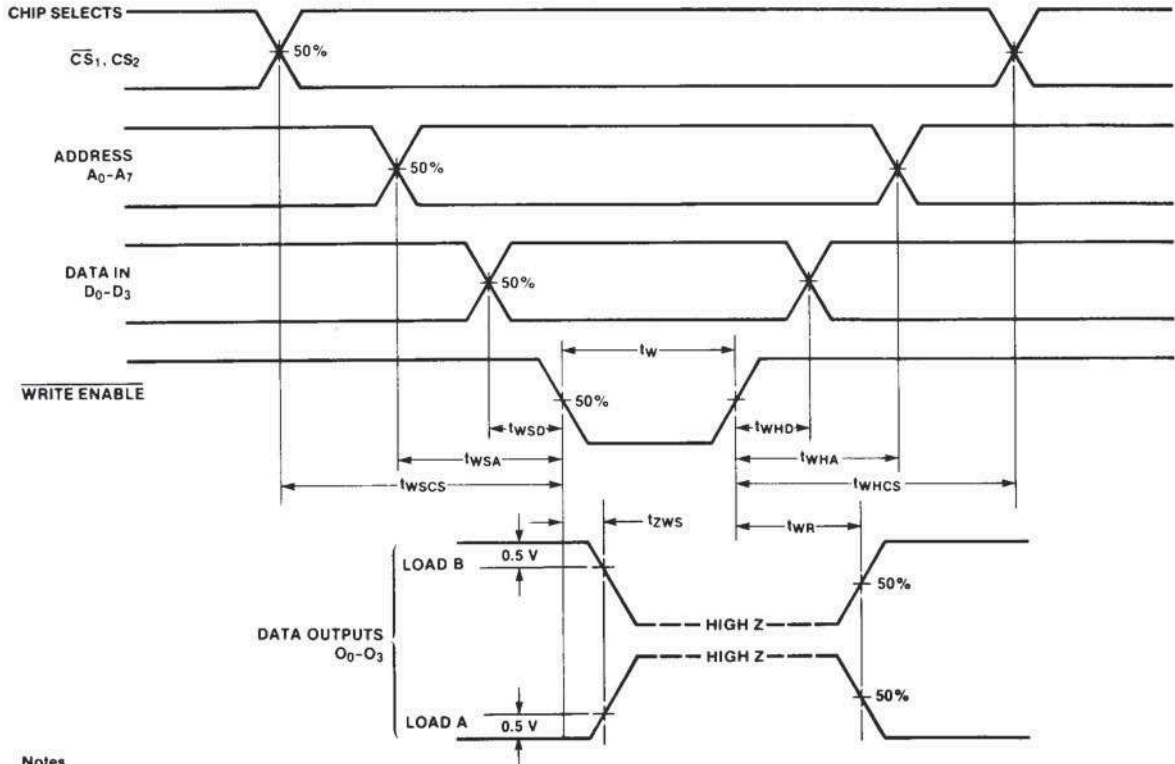
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3c Read Mode Propagation Delay from Output Enable



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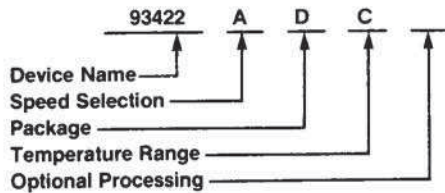
Fig. 4 Write Mode Timing



Notes

1. Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.
2. Input voltage levels for worst case AC test are 3.0/0.0 V.

Ordering Information



Speed Selection

- Blank = Standard Speed
- A = 'A' Grade

Packages and Outlines (See Section 9)

- D = Ceramic DIP
- F = Flatpak
- L = Leadless Chip Carrier
- P = Plastic DIP

Temperature Range

- C = 0°C to +75°C
- M = -55°C to +125°C

Optional Processing

- QB = Mil Std 883
Method 5004 and 5005, Level B
- QR = Commercial Device with
160 Hour Burn In or Equivalent