AM25LS22

8-Bit Serial/Parallel Register with Sign Extend

The AM25LS22 is an eight-bit serial/parallel register built using advanced Low-Power Schottky processing. The device features an eight-bit parallel multiplexed input/output port to provide improved bit density in a 20-pin package. Data may also be loaded into the device in a serial manner from either input D_A or D_B. A serial output, Q_0, is also provided.

The AM25LS22 is specifically designed for operation with the AM25LS14 serial/parallel two's complement multiplier and provides the sign extended function required for this device.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am25LS22

8-Bit Serial/Parallel Register with Sign Extend

DISTINCTIVE CHARACTERISTICS

- Three-state outputs with multiplexed input
- Multiplexed serial data input
- Sign extend function
- Second sourced by T.I. as Am54LS/74LS322

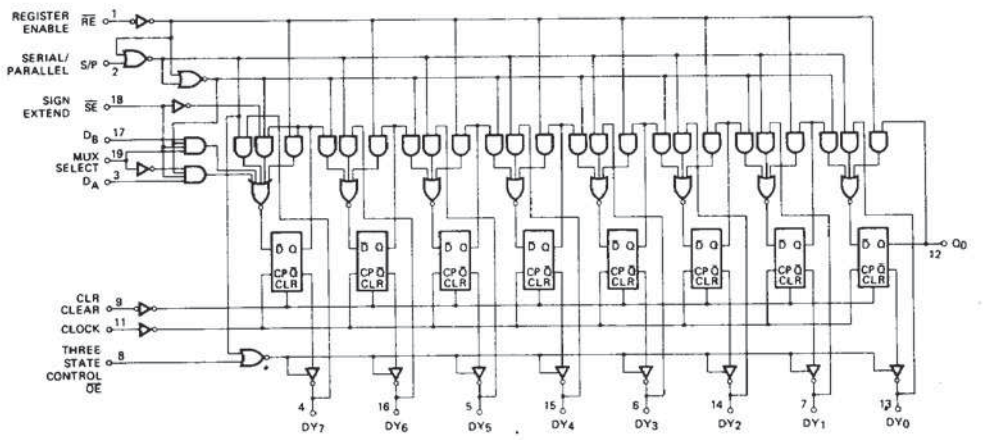
GENERAL DESCRIPTION

The Am25LS22 is an eight-bit serial/parallel register built using advanced Low-Power Schottky processing. The device features an eight-bit parallel multiplexed input/output port to provide improved bit density in a 20-pin package. Data may also be loaded into the device in a serial manner from either input D_A or D_B. A serial output, Q_0 is also provided.

The Am25LS22 is specifically designed for operation with the Am25LS14 serial/parallel two's complement multiplier and provides the sign extended function required for this device.

When the Register Enable ($\overline{RE}$) input is HIGH, the register will retain its current contents. Synchronous parallel loading is accomplished by applying a LOW to $\overline{RE}$ and applying a LOW to the Serial/Parallel (S/P) input. This places the three-state outputs in the high-impedance state independent of $\overline{OE}$ and allows data that is applied on the input/output lines (DY_i) to be clocked into the register. When the S/P input is HIGH, the device will shift right. The Sign Extend ($\overline{SE}$) input is used to repeat the sign in the Q_7 flip-flop. This occurs whenever $\overline{SE}$ is LOW when the SHIFT mode is selected. When $\overline{SE}$ is high, the serial two-input multiplexer is enabled. Thus, either D_A or D_B can be selected to load data serially. The register changes state on the LOW-to-HIGH transition of the clock. A clear input (CLR) is used to asynchronously reset all flip-flops when a LOW is applied.

BLOCK DIAGRAM



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RELATED PRODUCTS

Part No.	Description
Am25LS23	8-Bit Shift/Storage Register

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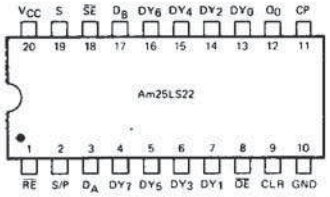
CONNECTION DIAGRAM
Top View



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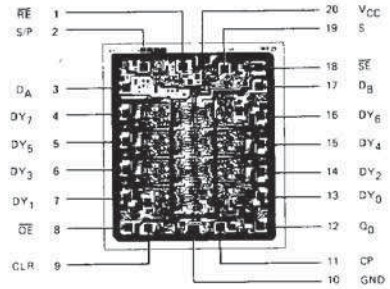
Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.096" x 0.112"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS22 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - P – 20-pin plastic DIP
  - X – Dice
- **Am25LS22** — Device type
  - 8-Bit Serial/Parallel Register with Sign Extend

Valid Combinations	
Am25LS22	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	DY_i	I/O	The multiplexed parallel input/output port to the device. Data may be parallel loaded into the register or data can be read in parallel from the register on these pins. These outputs can be forced to the high-impedance state, i = 0 through 7.
12	Q_0	O	The continuous output from the Q_0 flip-flop of the register. This output is used for serial shifting.
1	$\overline{RE}$	I	Register Enable. When $\overline{RE}$ is LOW, the register functions are enabled. When $\overline{RE}$ is HIGH, the register functions (parallel load, shift right and sign extend) are inhibited.
2	S/P	I	Serial/Parallel. When S/P is LOW, the register can be synchronously parallel loaded. This input forces the register output buffers to the high-impedance state independent of the $\overline{OE}$ input. When S/P is HIGH, the register contents are shifted right on the clock LOW-to-HIGH transition.
18	$\overline{SE}$	I	Sign Extend. When the $\overline{SE}$ input is LOW, the contents of the Q_7 flip-flop will be repeated in the Q_7 flip-flop as the register is shifted right. When $\overline{SE}$ is HIGH, the two-input multiplexer (D_A and D_B) is enabled to enter data during the serial shift right. The Q_7 flip-flop (DY_7) is normally considered the MSB of the register for arithmetic definitions.
3, 17	D_A, D_B	I	The serial inputs to the device.
19	S	I	Multiplexer Select. When S is LOW, the D_A serial input is selected. When S is HIGH, the D_B serial input is selected.
9	CLR	I	Clear. The asynchronous clear to the register. When the clear is LOW, the outputs of the flip-flops are set LOW independent of all other inputs. When the clear is HIGH, the register will perform the selected function.
11	CP	I	Clock. The clock pulse for the register. Register operations occur on the LOW-to-HIGH transition of the clock pulse.
8	$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the eight DY_i outputs are in the high-impedance state. When $\overline{OE}$ is LOW, data in the eight flip-flops will be present at the register parallel outputs unless S/P is LOW.

FUNCTION TABLE

Mode	Inputs							Outputs								
	Clear	Register Enable	Serial/ Parallel	Sign Extend	Mux Select	$\overline{OE}$*	Clock	DY_7	DY_6	DY_5	DY_4	DY_3	DY_2	DY_1	DY_0	Q_0
Clear	L	H	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	L	H	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	L	L	X	X	L	X	Z	Z	Z	Z	Z	Z	Z	Z	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X	↑	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_0
Shift Right	H	L	H	H	L	L	↑	D_A	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
	H	L	H	H	H	L	↑	D_B	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
Sign Extend	H	L	H	L	X	L	↑	Y_{7n}	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
Hold	H	H	X	X	X	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC

L = LOW
↑ = Clock LOW-to-HIGH Transition
X = Don't Care
H = HIGH
NC = No Change
Z = High-Impedance Output State

*When the OE input is HIGH, all input/output terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.

D_7, D_6...D_0 = the level of the steady-state input at the respective DY_n terminal is loaded into the flip-flop while the flip-flop outputs (except Q_0) are isolated from the DY_n terminal.

D_A, D_B = the level of the steady-state inputs to the serial multiplexer input.

Y_{7n}, Y_{6n}...Y_{0n} = the level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

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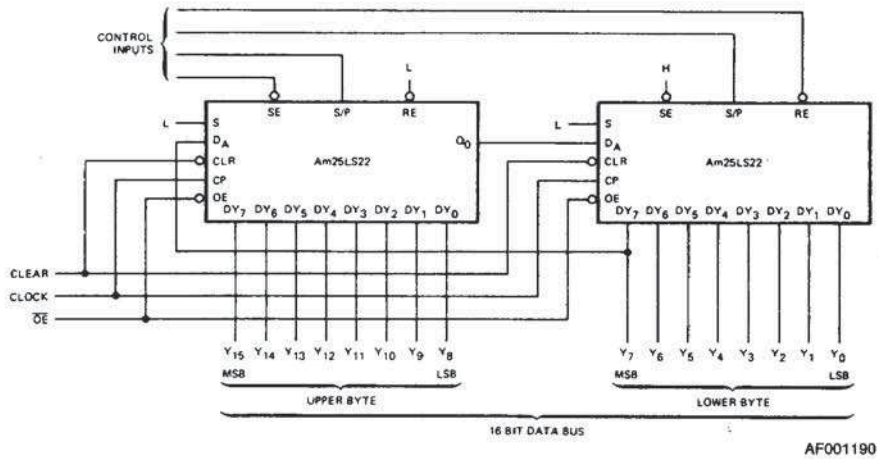
Refer to Page 13-1 for Essential Information on Military Devices

APPLICATION



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System Operation	Am25LS22 Upper Byte				Am25LS22 Lower Byte				Function
	$\overline{SE}$	S/P	$\overline{RE}$	$\overline{OE}$	$\overline{SE}$	S/P	$\overline{RE}$	$\overline{OE}$	Description
Load lower byte and extend lower byte sign to upper byte	H	H	L	X	X	L	L	X	Load from Bus
	L	H	L	H	X	X	H	H	7 clock cycles to extend sign
Load upper byte and extend upper byte sign while shifting value to lower byte position	X	L	L	X	X	X	X	X	Load from Bus
	H	H	L	H	H	H	L	H	8 clock cycles to extend upper byte sign and shift upper byte into lower byte position
Read 16-bit word to Bus	X	X	X	L	X	X	X	L	Unload

Two Am25LS22 8-bit registers can be used to perform the sign extend associated with two's complement 8-bit bytes for arithmetic operations in a 16-bit machine. If the upper byte value is to be used, it is shifted to the lower bit positions and its sign is extended. If the lower byte value is to be used, it is held in place while the sign is extended downward from the MSB position of the upper byte.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
HIGH Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ($\overline{OE}$, S/P, RE,
CP, CLR) ..... −0.5V to +7.0V
DC Input Voltage (Others) ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Q_O, I_{OH} = −440µA	MIL	2.5			Volts
				COM'L	2.7			
			DY_i, I_{OH} = −1.0mA	MIL	2.4			
			DY_i, I_{OH} = −2.6mA	COM'L	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		$\overline{SE}$			−1.08	mA
				S			− 0.72	
				Others			−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V (Except DY_i)		$\overline{SE}$			60	µA
				S			40	
				Others			20	
I_I	Input HIGH Current	V_{CC} = MAX, (Except DY_i)	V_{IN} = 7.0V	$\overline{OE}$,S/P,RE,CP,CLR			0.1	mA
			V_{IN} = 5.5V	$\overline{SE}$			0.3	
				S			0.2	
				Others			0.1	
I_{OZ}	Off state (High-Impedance) Output Current (DY_i)	V_{CC} = MAX		V_O = 2.4			40	mA
				V_O = 0.4V			−100	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX				40	65	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN, or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

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Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to DY_i		R_L = 2.0kΩ, C_L = 15pF		16.5	24	ns
t_{PHL}					18	26	
t_{PHL}	Clear to DY_i				23	30	ns
t_{PLH}	Clock to Q_0				16.5	24	ns
t_{PHL}					18	26	
t_{PHL}	Clear to Q_0				23	30	ns
t_{ZH}	$\overline{OE}$ to DY_i				13	21	ns
t_{ZL}					18	26	
t_{HZ}			R_L = 2.0kΩ, C_L = 5pF		13	21	
t_{LZ}					18	26	
t_{ZH}	SER/PAR to DY_i		R_L = 2.0kΩ, C_L = 15pF		18	26	ns
t_{ZL}					23	32	
t_{HZ}			R_L = 2.0kΩ, C_L = 5pF		18	26	
t_{LZ}					23	32	
t_s	RE to Clock		R_L = 2.0kΩ, C_L = 15pF	20			ns
t_s	SE to Clock			10			
t_s	S to Clock			15			
t_s	D_A and D_B to Clock			15			
t_s	DY_i (Load) to Clock			15			
t_s	Clear Recovery to Clock			8.0			
t_s	S/P to Clock			15			ns
t_h	Any Input			0			
t_h	Clear Hold			0			ns
t_{pw}	Clock	HIGH		8.0			ns
		LOW		8.0			
t_{pw}	Clear			20			ns
f_{max} (Note 1)	Maximum Clock Frequency			35	50		MHz

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

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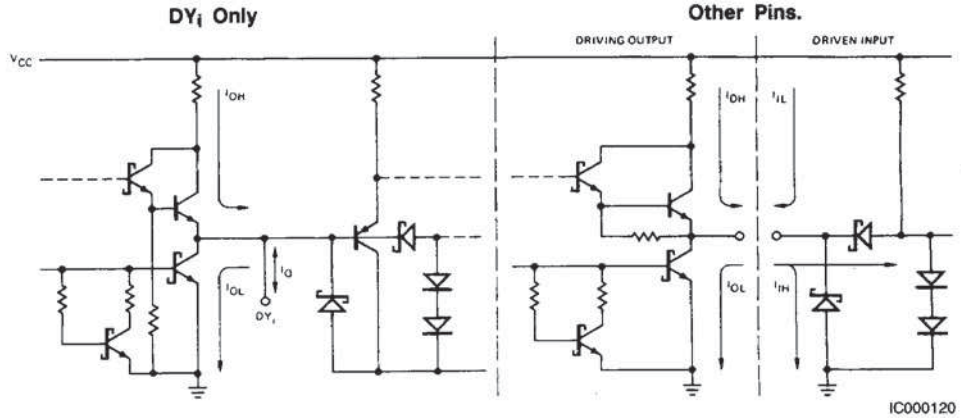
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description		Test Conditions	COMMERCIAL Am25LS Min	COMMERCIAL Am25LS Max	MILITARY Am25LS Min	MILITARY Am25LS Max	Units
t_{PLH}	Clock to DY_i		C_L = 50pF, R_L = 2.0kΩ		35		41	ns
t_{PHL}					38		44	
t_{PHL}	Clear to DY_i				43		50	ns
t_{PLH}	Clock to Q_0				35		41	ns
t_{PHL}					38		44	
t_{PHL}	Clear to Q_0				43		50	ns
t_{ZH}	OE to DY_i				32		36	ns
t_{ZL}					38		44	
t_{HZ}			C_L = 5.0pF, R_L = 2.0kΩ		28		31	
t_{LZ}					34		39	
t_{ZH}	SER/PAR to DY_i		C_L = 50pF, R_L = 2.0kΩ		38		44	ns
t_{ZL}					46		53	
t_{HZ}			C_L = 5.0pF, R_L = 2.0kΩ		34		39	
t_{LZ}					42		48	
t_s	RE to Clock		C_L = 50pF, R_L = 2.0KΩ	30		35		
t_s	SE to Clock			17		20		
t_s	S to Clock			24		27		ns
t_s	D_A and D_B to Clock			24		27		
t_s	DY_i (Load) to Clock			24		27		
t_s	Clear Recovery to Clock			15		17		
t_s	S/P to Clock			24		27		ns
t_h	Any Input			4		5		
t_h	Clear Hold			4		5		ns
t_{pw}	Clock	HIGH		15		17		ns
		LOW		15		17		
t_{pw}	Clear			30		35		ns
f_{max} (Note 1)	Maximum Clock Frequency			26		23		MHz

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.