AM25LS2518

Quad D Register with Standard and Three-State Outputs

The AM25LS2518 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

The same data as on the Q outputs is enabled at the three-state Y outputs when the “output control” ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer’s datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. ‘Typical’ values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am25LS2518

Quad D Register with Standard and Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Low-Power Schottky version of the popular Am2918 and Am25S18
- Four standard totem-pole outputs
- Four three-state outputs
- Four D-type flip-flops
- Second sourced by T. I. as the SN54/74LS388

GENERAL DESCRIPTION

The Am25LS2518 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

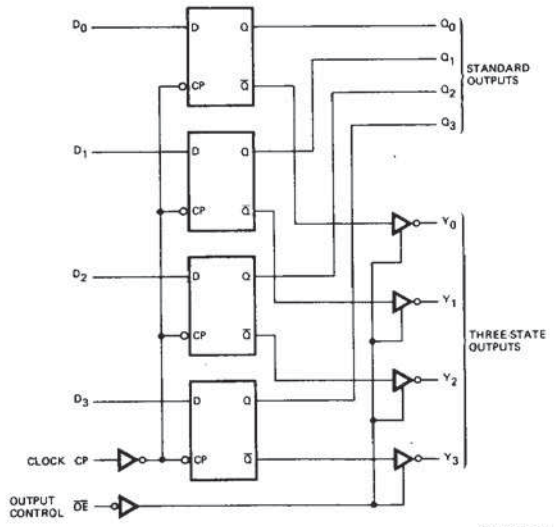
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am25LS2518 is a 4-bit, high-speed register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three-state outputs provide access to a data bus to dump the results after a number of iterations.

The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the Am25LS2518 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

BLOCK DIAGRAM



BD001510

RELATED PRODUCTS

Part No.	Description
Am25S18	Quad D Register
Am2918	Quad D Register
Am29LS18	Quad D Low Power Register
Am29LS2519	Quad D Low Power Register

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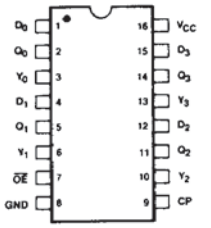
Refer to Page 13-1 for Essential Information on Military Devices

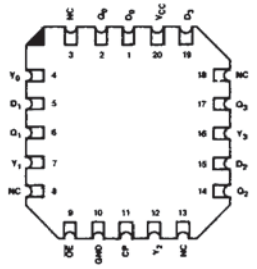
CONNECTION DIAGRAM
Top View

D-16, P-16



CD001670

L-20-1



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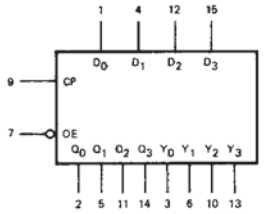
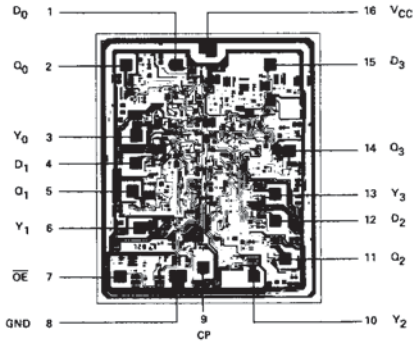
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000580

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.083" x 0.099"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2518 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 16-pin CERDIP
  - F – 16-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 16-pin plastic DIP
  - X – Dice
- **Am25LS2518** — Device type: Quad D Register

Valid Combinations	
Am25LS2518	PC DC, DM FM LC, LM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D_i	I	The four data inputs to the register.
	Q_i	O	The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.
	Y_i	O	The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.
9	CP	I	Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.
7	$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

TRUTH TABLE

INPUTS			OUTPUTS		
$\overline{OE}$	CLOCK CP	D	Q	Y	NOTES
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW NC = No change
H = HIGH ↑ = LOW-to-HIGH transition
X = Don't care Z = High-Impedance
Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

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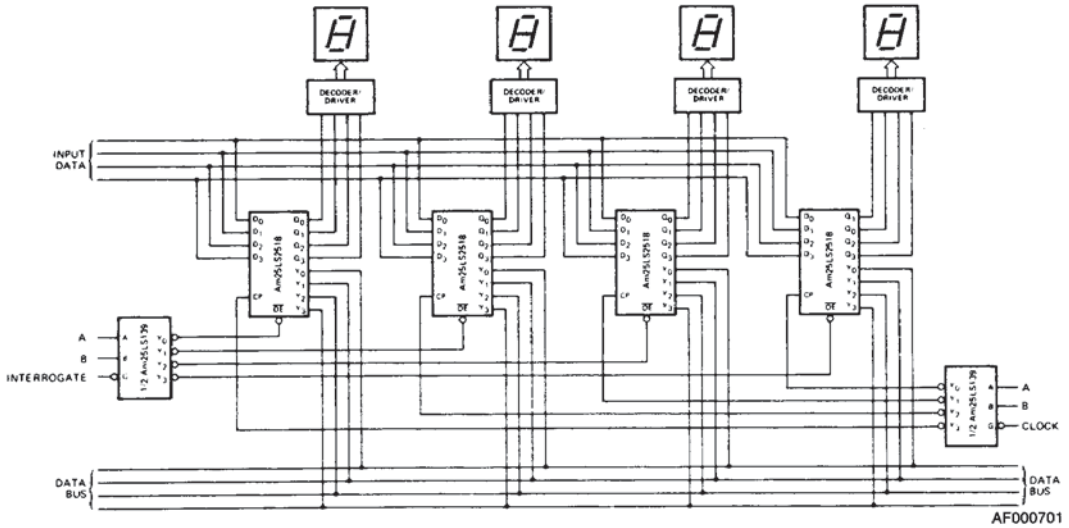
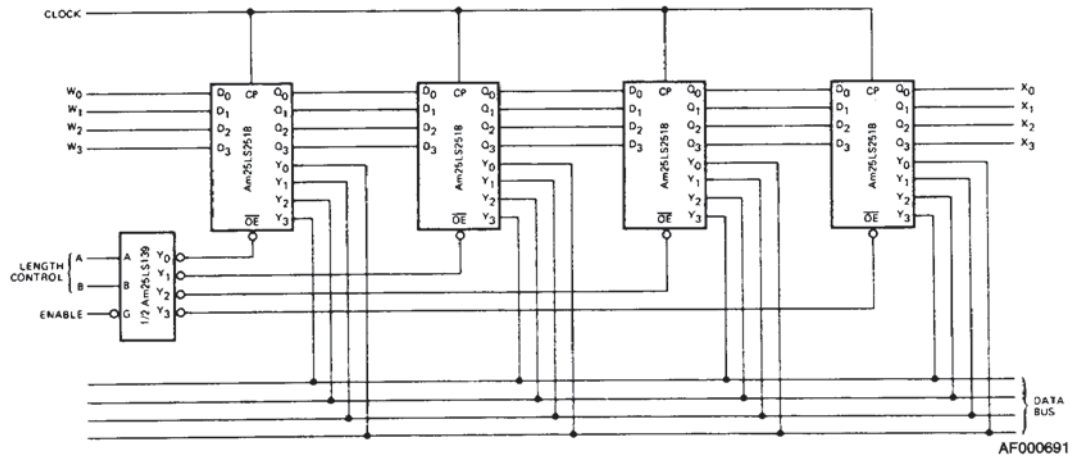
APPLICATIONS



The Am25LS2518 used as display register with bus interrogate capability.



The Am25LS2518 as a variable length (1, 2, 3 or 4 word) shift register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	O, I_{OH} = −660μA	MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
			Y	MIL, I_{OH} = −1.0mA	2.4	3.4		
				COM'L, I_{OH} = −2.6mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0 mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V					0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V				−20	μA
			V_O = 2.4V				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX				17	28	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all inputs at 4.5V and all outputs open.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Q_i		C_L = 15pF R_L = 2.0kΩ		18	27	ns
t_{PHL}					18	27	
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)				18	27	ns
t_{PHL}					18	27	
t_{pw}	Clock Pulse Width	LOW		18			ns
		HIGH		15			
t_s	Data			15			ns
t_h	Data			5.0			ns
t_{ZH}	$\overline{OE}$ to Y_i				7.0	11	ns
t_{ZL}					8	12	
t_{HZ}	$\overline{OE}$ to Y_i		C_L = 5.0pF R_L = 2.0kΩ		14	21	ns
t_{LZ}					12	18	
f_{max}	Maximum Clock Frequency (Note 1)			35	50		MHz

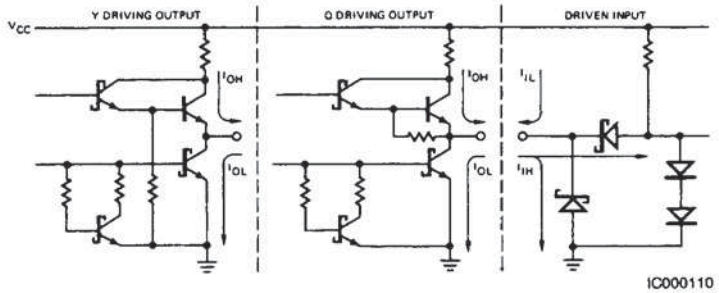
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description		Test Conditions	COMMERCIAL Am25LS2518 Min	COMMERCIAL Am25LS2518 Max	MILITARY Am25LS2518 Min	MILITARY Am25LS2518 Max	Units
t_{PLH}	Clock to Q_i		C_L = 50pF R_L = 2.0kΩ		38		45	ns
t_{PHL}					38		45	
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)				35		40	ns
t_{PHL}					35		40	
t_{pw}	Clock Pulse Width	LOW		20		20		ns
		HIGH		20		20		
t_s	Data			15		15		ns
t_h	Data			5.0		5.0		ns
t_{ZH}	$\overline{OE}$ to Y_i				15		17	ns
t_{ZL}					16		17	
t_{HZ}	$\overline{OE}$ to Y_i		C_L = 5.0pF R_L = 2.0kΩ		27		30	ns
t_{LZ}					24		30	
f_{max}	Maximum Clock Frequency (Note 1)			30		25		MHz

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS2518
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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Refer to Page 13-1 for Essential Information on Military Devices