AM25S18

Quad D Register with Standard and Three-State Outputs

The AM25S18 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

The same data as on the Q outputs is enabled at the three-state Y outputs when the “output control” ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer’s datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. ‘Typical’ values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am25S18

Quad D Register with Standard and Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75MHz clock frequency

GENERAL DESCRIPTION

The Am25S18 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

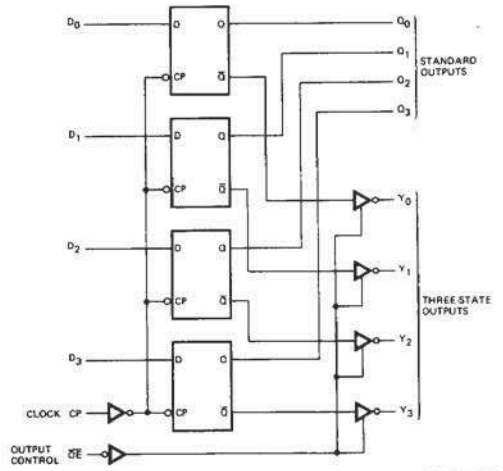
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am25S18 is a 4-bit, high speed Schottky register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three state outputs provide access to a data bus to dump the results after a number of iterations.

The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the Am25S18 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

BLOCK DIAGRAM



BD001510

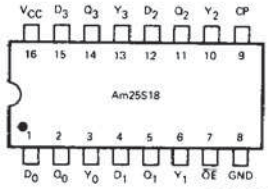
RELATED PRODUCTS

Part No.	Description
Am25S07	Register
Am25S08	Register
Am25S09	Register
Am25S374	Register
Am29821-26	Register

03613B

Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View



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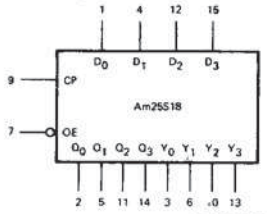
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



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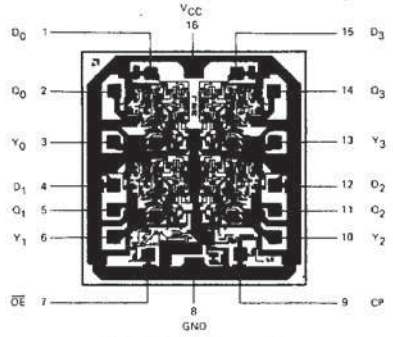
METALLIZATION AND PAD LAYOUT



DIE SIZE 0.077" x 0.079"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25S18 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am25S18** — Device type
  - Quad D Register with Standard and Three-State Outputs

Valid Combinations	
Am25S18	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D_i	I	The four data inputs to the register.
	Q_i	O	The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.
	Y_i	O	The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.
9	CP	I	Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.
7	$\overline{OE}$	O	Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

TRUTH TABLE

INPUTS			OUTPUTS		
$\overline{OE}$	CLOCK CP	D	Q	Y	NOTES
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW NC = No change
H = HIGH ↑ = LOW to HIGH transition
X = Don't care Z = High impedance
Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

LOADING RULES (In Unit Loads)

Input/Output	Pin Nos.	Input Unit Load	Fan-out	
			Output HIGH	Output LOW
D_0	1	1	–	–
Q_0	2	–	20	10*
Y_0	3	–	40/130	10*
D_1	4	1	–	–
Q_1	5	–	20	10*
Y_1	6	–	40/130	10*
$\overline{OE}$	7	1	–	–
GND	8	–	–	–
CP	9	1	–	–
Y_2	10	–	40/130	10*
Q_2	11	–	20	10*
D_2	12	1	–	–
Y_3	13	–	40/130	10*
Q_3	14	–	20	10*
D_3	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

*Fan-out on each Q_i and Y_i output pair should not exceed 15 unit loads (30mA) for i = 0, 1, 2, 3.

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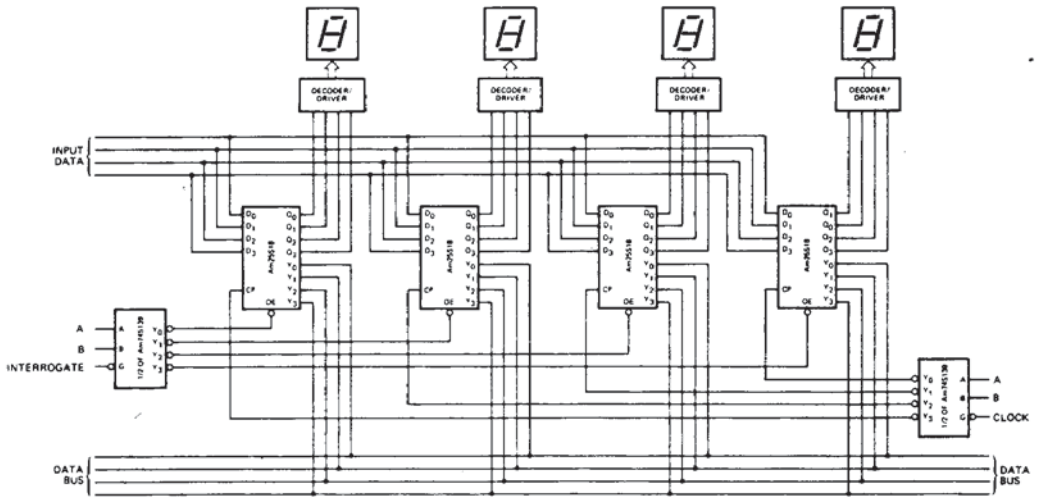
APPLICATIONS



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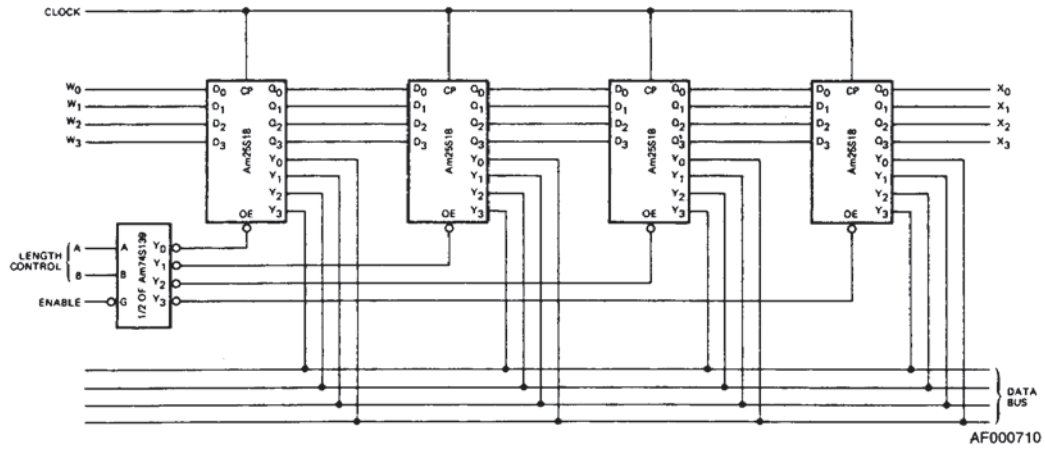
The Am25S18 Used As Display Register With Bus Interrogate Capability.



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The Am25S18 As A Variable Length (1, 2, 3 or 4 Word) Shift Register.

03613B

Refer to Page 13-1 for Essential Information on Military Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 18) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
HIGH Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

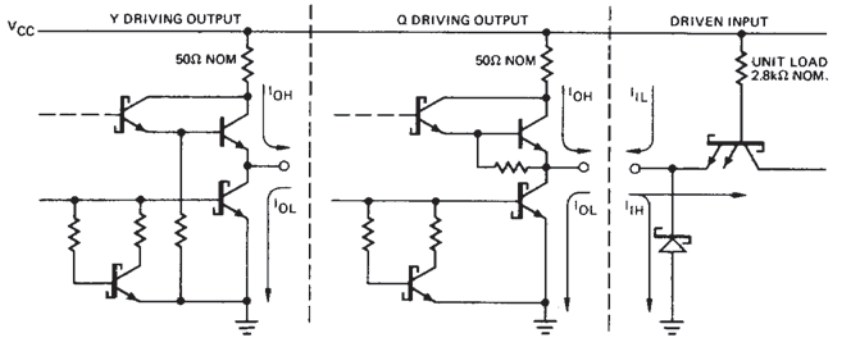
Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Q I_{OH} = −1mA	MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
			Y	XM, I_{OH} = −2mA	2.4	3.4		
				XC, I_{OH} = −6.5mA	2.4	3.2		
V_{OL}	Output LOW Voltage (Note 6)	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IH} or V_{IL}					0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V					−2.0	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					50	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_O	Y Output Off-State Leakage Current	V_{CC} = MAX.		V_O = 2.4V			50	µA
				V_O = 0.4V			−50	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				80	130	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under Operating Ranges for the applicable device type.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with all inputs at 4.5V and all outputs open.
6. Measured on Q outputs with Y outputs open. Measured on Y outputs with Q outputs open.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V, R_L=280Ω)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Q Output		C_L = 15pF		6.0	9.0	ns
t_{PHL}					8.5	13	
t_{pw}	Clock Pulse Width	HIGH		7.0			ns
		LOW		9.0			
t_s	Data			5.0			ns
t_h	Data			3.0			ns
t_{PLH}	Clock to Y Output				6.0	9.0	ns
t_{PHL}	($\overline{OE}$ LOW)				8.5	13	
t_{ZH}	Output Control to Output		C_L = 15pF		12.5	19	ns
t_{ZL}					12	18	
t_{HZ}			C_L = 5.0pF		4.0	6.0	
t_{LZ}					7.0	10.5	
f_{max}	Maximum Clock Frequency		C_L = 15pF	75	100		MHz

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



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Note: Actual current flow direction shown.