AM27S85, AM27S85A

16,384-Bit (4096x4) Registered PROM

This device contains a 4-bit parallel data register in the array-to-output path intended for normal registered data operations. In parallel with the output data registers is another 4-bit register with shifting capability, called a shadow register. As the name implies, the shadow register is intended to operate in the background of the normal output data register. This shadow register can be used in a systematic way to control and observe the output data register to exercise desired system functions during a diagnostic test mode.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am27S85/27S85A

16,384-Bit (4096x4) Registered PROM with SSR™ Diagnostics Capability

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

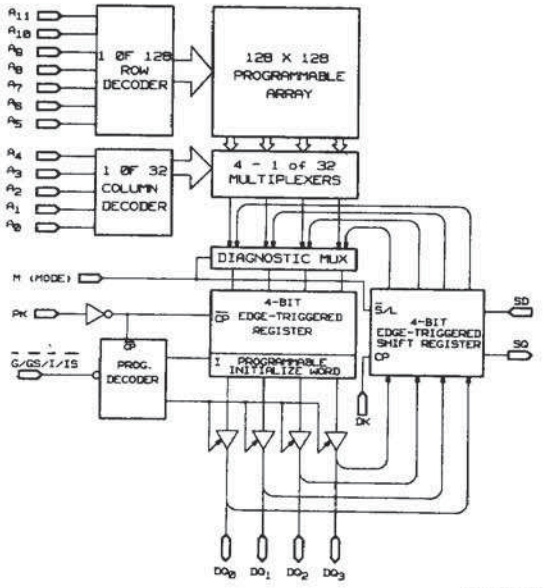
- On-chip diagnostic shift register for serial observability and controllability of the output register
- User-programmable for Asynchronous Enable, Synchronous Enable, Asynchronous Initialize, or Synchronous Initialize
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and registers.
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability.
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ. > 98%).
- Increased drive capability, 24 mA I_{OL}

GENERAL DESCRIPTION

This device contains a 4-bit parallel data register in the array-to-output path intended for normal registered data operations. In parallel with the output data registers is another 4-bit register with shifting capability, called a shadow register. As the name implies, the shadow register is intended to operate in the background of the normal output data register. This shadow register can be used in a systematic way to control and observe the output data register to exercise desired system functions during a diagnostic test mode.

To offer the system designer maximum flexibility, this device contains a single programmable multi-functional input ($\overline{G}/\overline{GS}/\overline{I}/\overline{IS}$). The unprogrammed state of this pin operates an Asynchronous Enable ($\overline{G}$) input. An architecture word permits the programming of the functionality of this pin to Synchronous Enable ($\overline{GS}$), Asynchronous Initialize ($\overline{I}$), or Synchronous Initialize ($\overline{IS}$).

BLOCK DIAGRAM



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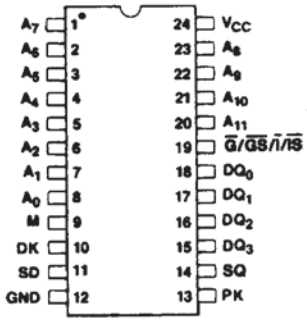
PRODUCT SELECTOR GUIDE

Part Number	Am27S85A		Am27S85	
Address Setup Time	27 ns	30 ns	35 ns	40 ns
Clock-to-Output Delay	12 ns	17 ns	15 ns	20 ns
Operatinge Range	C *	M	C	M

CONNECTION DIAGRAMS

Top View

DIPs*



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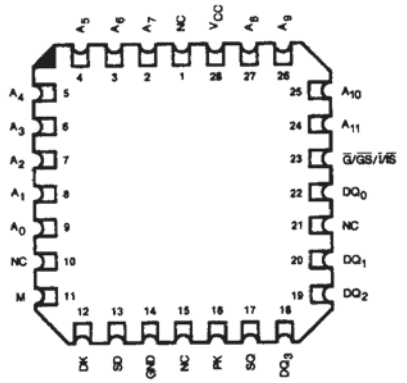
LCC**



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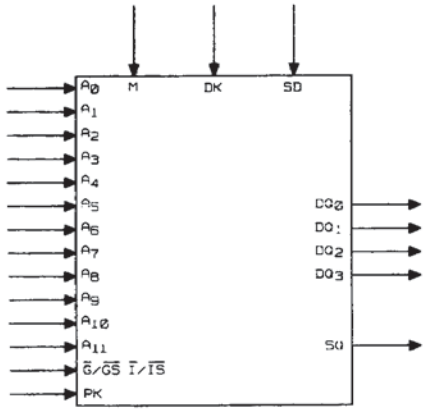
*Also available in a 24-pin Flatpack. Pinout identical to DIPs.
**Also available in a 28-pin Square PLCC. Pinout identical to LCC.
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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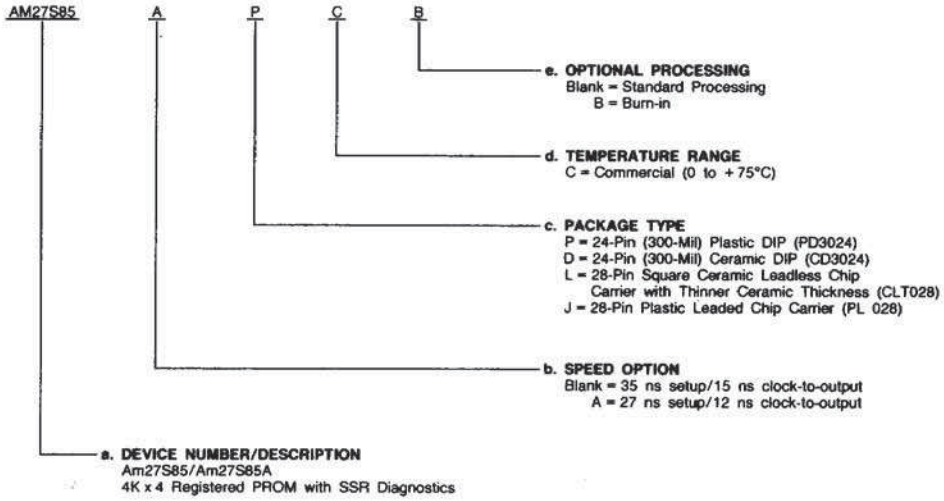
ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27S85	PC, PCB, DC, DCB, LC, LCB, JC, JCB
AM27S85A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

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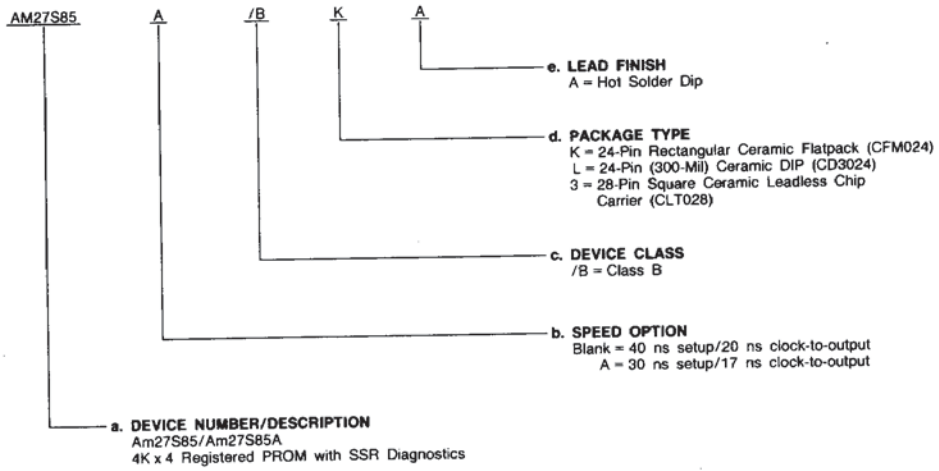
MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27S85	/BKA, /BLA, /B3A
AM27S85A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

PIN DESCRIPTION

$A_0 - A_{11}$ Address Inputs
The 12-bit field presented at the address inputs selects one of 4096 memory locatios to be read from.

PK Pipeline Clock (Input)
The pipeline clock is used to load data into the parallel registers. The data source may be the memory array, the shadow register, or the initialize word if programmed for synchronous initialize architecture. Transfer occurs on the LOW-to-HIGH transition of PK.

$DQ_0 - DQ_3$ Data I/O Port
Parallel data output from the pipeline register or parallel data input to the shadow register.

M Mode (Input)
Control input which controls the source data for both sets of registers. MODE inputs is LOW in the normal mode of operation. The PROM array is the input source for the output data registers. The shadow register is in the shift mode ($SD \rightarrow S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3/SQ$). MODE input HIGH allows transfer of data for diagnostic testing. Shadow register data may be loaded into the output register or output data bus information may be loaded into the shadow register.

DK Diagnostic Clock (Input)
The diagnostic clock is used to load or shift the data into the shadow register. Transfer occurs on the LOW-to-HIGH transition of DK.

SD Serial Data Input
This pin performs two functions depending on the state of the MODE input. If M is LOW, the SD pin is the data transfer pin for serial data ($SD \rightarrow S_0$). If the M input is HIGH, the SD pin operates as a control pin where SD asserted LOW permits output data to be loaded into the shadow register on the next LOW-toHIGH transition of DK. SD asserted HIGH represents a NO-OP function on this device.

SQ Serial Data Output
This pin operates as a transfer pin for serial data. When M input is LOW, $SQ = S_3$. When M is HIGH and SD operates as a control pin, the SQ pin operates as a pass through of SD control. SQ is an active totem-pole output.

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

This device contains a two bit architecture word which, according to programming, will provide the following functions:

$\overline{G}/\overline{GS}/\overline{I}/\overline{IS}$ Asynchronous/Synchronous Output Enable/ Asynchronous/Synchronous Initialize

With the architecture word unprogrammed this pin operates as an Asynchronous Output Enable ($\overline{G}$) and provides direct control of the DQ output three-state drivers independent of PK. With proper programming of the architecture word this pin will function as a Synchronous Output Enable ($\overline{GS}$) which will control the state of the DQ output three-state drivers in conjunction with PK. This is useful where more than one registered PROM is bussed together for word depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

The architecture word may also be programmed so that this pin will functions as an Asynchronous Initialize ($\overline{I}$) which is a control pin used to initialize the output data registers from a programmable word independent of PK. This can be used to generate any arbitrary microinstruction for system interrupt or reset. When the architecture word is properly programmed this pin will function as a Synchronous Initialize ($\overline{IS}$) which will initialize the output data registers from a programmable word in conjunction with PK. This can be used for a system interrupt or reset which must be synchronized with PK.

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MODE SELECT TABLE

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DK. M (MODE) and SD determine what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PK. M (MODE) selects whether the data source is the PROM Array or the shadow register output.

Because of the independence of the clock inputs, data can be shifted in the shadow register via DK and loaded into the pipeline register from the data input via PK as long as no set up or hold times are violated.

Inputs					Outputs			
SD	M	DK	PK	$\overline{IS}$*	SQ	Shadow Register	Pipeline Register	Operation
X	L	↑	–	X	S_3	$S_n \leftarrow S_{n-1}$ $S_0 \leftarrow SD$	NA	Serial Shift; $SD \rightarrow S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3/SQ$
X	L	–	↑	H	S_3	NA	$Q_n \leftarrow$ ARRAY DATA	Normal Load Pipeline Register from PROM
X	L	–	↑	L	S_3	NA	$Q_n \leftarrow$ INIT DATA	Synchronous Initialize Pipeline Register*
L	H	↑	–	X	SD	$S_n \leftarrow Q_n$	NA	Load Shadow Register from Outputs ($DQ_0 - DQ_3$)
X	H	–	↑	X	SD	NA	$Q_n \leftarrow S_n$	Load Pipeline Register from Shadow Register
H	H	↑	–	X	SD	Hold	NA	No-Op; Hold Shadow Register

MODE SELECT TABLE DEFINITIONS

INPUTS

H = HIGH
L = LOW
X = Don't Care
– = Steady State LOW or HIGH or HIGH-to-LOW transition
↑ = LOW-to-HIGH transition

OUTPUTS

SQ = Serial Data Output
$S_3 - S_0$ = Shadow Register Outputs (internal to devices)
$Q_3 - Q_0$ = Pipeline Register Outputs
NA = NOT applicable: Output is not a function of the specified input combinations

*Applies only if the architecture word has been programmed for Synchronous Initialize operation.

APPLICATIONS

Applying Serial Shadow Register (SSR) Diagnostics in Bipolar Microcomputers

Diagnostics

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware related failures in a system. This capability must be able to both *observe* intermediate test points and *control* intermediate signals – address, data, control, and status – to exercise all portions of the system under test. These two capabilities, observability and controllability, provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs and determine whether the system is functioning correctly.

Testing Combinational and Sequential Networks

The problem of testing a combinational logic network is well understood. Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set of test vectors will discover.

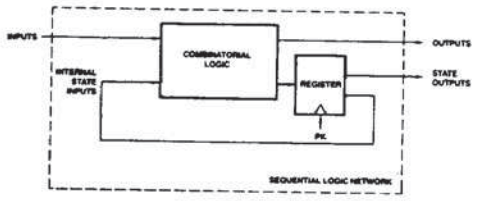

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Figure 1.

A sequential network (Figure 1) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

Serial Shadow Register Diagnostics

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinational network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 2 shows the method by which Serial Shadow Register diagnostics accomplishes these two functions.

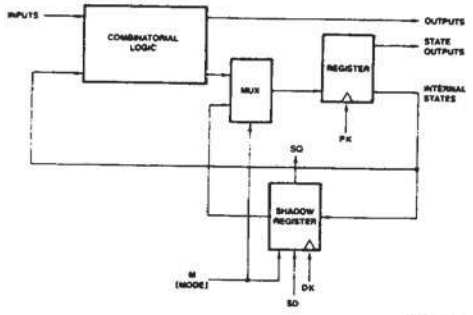

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Figure 2.

Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with PK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled. This means that those techniques which have been developed to test combinational networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temparature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 to V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec.) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +75°C
Supply Voltage (V_{CC}) ..... +4.75 V to +5.25 V

Military (M) Devices*
Case Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality and parameters of the device are guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Unit
V_{IH}	Input Voltage HIGH	Guarantee Input HIGH Voltage (Note 1)			2.0			V
V_{IL}	Input Voltage LOW	Guarantee Input LOW Voltage (Note 1)					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA					−1.2	V
V_{OH}	Output Voltage (HIGH)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} (DQ_0 − DQ_3) = −2 mA		2.4			V
			I_{OH} (SQ) = −0.5 mA					
V_{OL}	Output Voltage (LOW)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	COM'L I_{OL} (DQ_0 − DQ_3) = 24 mA				0.5	V
			MIL I_{OL} (DQ_0 − DQ_3) = 18 mA					
			I_{OL} (SQ) = 4 mA					
I_{IH}	Input Current (HIGH)	V_{CC} = Max.	V_{IN} = 2.7 V				25	μA
			V_{IN} = 5.5 V				40	
I_{IL}	Input Current (LOW)	V_{CC} = Max., V_{IN} = 0.40 V					−250	μA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max. V_{OUT} = 0 V (Note 2)	DQ_0 − DQ_3		−20		−90	mA
			SQ		−10		−85	
I_{CEX}	Output Leakage Current	V_{CC} = Max. $\overline{S0}/\overline{S1}$ = 2.4 V (Note 3)	V_{OUT} = V_{CC}				50	μA
			V_{OUT} = 0.4 V				−150	
I_{CC}	Power Supply Current	V_{CC} = Max., All inputs = 0.0 V (Note 4)	COM'L	T_A = 0°C			185	mA
				T_A = 25°C			175	
				T_A = 75°C			165	
			MIL	T_C = −55°C			195	
				T_C = 25°C			180	
				T_C = 125°C			155	
C_{IN}	Input Capacitance	V_{CC} = 5.0 V, T_A = 25°C V_{IN}/V_{OUT} = 2.0 V @ f = 1 MHz (Note 5)				5		pF
C_{OUT}	Output Capacitance					12		

Notes: 1. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
4. I_{CC} limits at temperature extremes are guaranteed by correlation to 25°C test limits.
5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted*) (Note 1)

No.	Parameter Symbol	Parameter Description	Am27S85A				Am27S85				Unit
			COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVPKH	Address to PK HIGH Setup Time	27		30		35		40		ns
2	TPKHAX	Address to PK HIGH Hold Time	0		0		0		0		ns
3	TPKHDQV1	Delay from PK HIGH to Output Valid, for initially active outputs (HIGH) or LOW) (Note 7)	4	12	4	17	4	15	4	20	ns
4	TPKHPKL TPKLPKH	PK Pulse Width (HIGH or LOW)	15		20		20		20		ns
5	TGLDQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW) (Note 3)		22		25		25		30	ns
6	TGHDQZ	Asynchronous Output Enable HIGH to Output High Z (Note 3)		17		22		20		25	ns
7	TGSVPKH	$\overline{GS}$ to PK HIGH Setup Time (Note 4)	12		12		15		15		ns
8	TPKHGSX	$\overline{GS}$ to PK HIGH Hold Time (Note 4)	0		0		0		0		ns
9	TPKHDQV2	Delay from PK HIGH to Output Valid, for initially High Z outputs (Note 4)		17		22		20		25	ns
10	TPKHDQZ	Delay from PK HIGH to Output High Z (Notes 2 & 4)		17		22		20		25	ns
11	TILDQV	Delay from $\overline{I}$ LOW to Output Valid (HIGH or LOW) (Note 5)		25		30		30		35	ns
12	TIHPKH	Asynchronous $\overline{I}$ Recovery to PK (HIGH) (Note 5)	20		25		25		30		ns
13	TILIH	Asynchronous $\overline{I}$ Pulse Width (LOW) (Note 5)	20		20		25		25		ns
14	TISVPKH	$\overline{IS}$ to PK HIGH Setup Time (Note 6)	20		25		20		25		ns
15	TPKHISX	$\overline{IS}$ to PK HIGH Setup Time (Note 6)	5		5		5		5		ns

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V, using test loads in A & B.
2. TGHDQZ and TPKHDQZ are measured to Steady State HIGH −0.5 V and Steady State LOW +0.5 V output levels, using the test load in C.
3. Applies only if the architecture is configured for Asynchronous $\overline{Enable}$.
4. Applies only if the architecture word has been programmed for a Synchronous $\overline{Enable}$ input.
5. Applies only if the architecture word has been programmed for a Asynchronous $\overline{Initialize}$ input.
6. Applies only if the architecture word has been programmed for a Synchronous $\overline{Initialize}$ input.
7. Minimum Delay times are guaranteed by design and supported by characterization data.

*Subgroups 7 and 8 apply to functional tests.

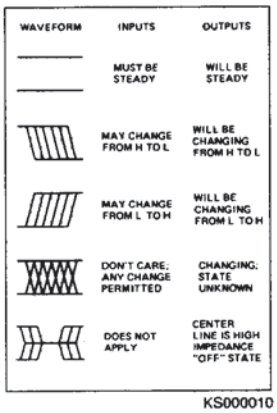
DIAGNOSTIC MODE SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted*)

No.	Parameter Symbol	Parameter Description	Am27S85/27S85A				Unit
			COM'L		MIL		
			Min.	Max.	Min.	Max.	
16	TSDVDKH	Serial Data In to DK HIGH Setup Time	25		30		ns
17	TDKHSDX	Serial Data In to DK HIGH Hold Time	0		0		ns
18	TMVPKH	Mode to PK HIGH Setup Time	35		40		ns
19	TPKHMX	Mode to PK HIGH Hold Time	0		0		ns
20	TMVDKH	Mode to DK HIGH Setup Time	35		40		ns
21	TDKHMX	Mode to DK HIGH Hold Time	0		0		ns
22	TDQVDKH	Output Data In to DK HIGH Setup Time	25		30		ns
23	TDKHDQX	Output Data In to DK HIGH Hold Time	0		0		ns
24	TDKHSQV	Delay from DK HIGH to Serial Data Output (Shifting)		30		35	ns
25	TSDVSQV	Delay from SD Valid to SQ Valid (Mode Input HIGH)		25		30	ns
26	TDKHDKL TDKLDKH	DK Pulse Width (HIGH or LOW)	25		25		ns
27	TMHSQV TMLSQV	Delay from Mode (HIGH or LOW) to SQ Valid		25		30	ns

See also Switching Test Circuits.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS



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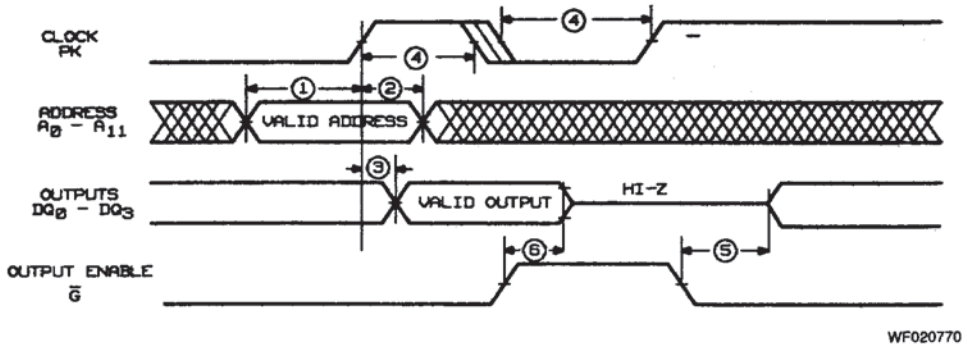

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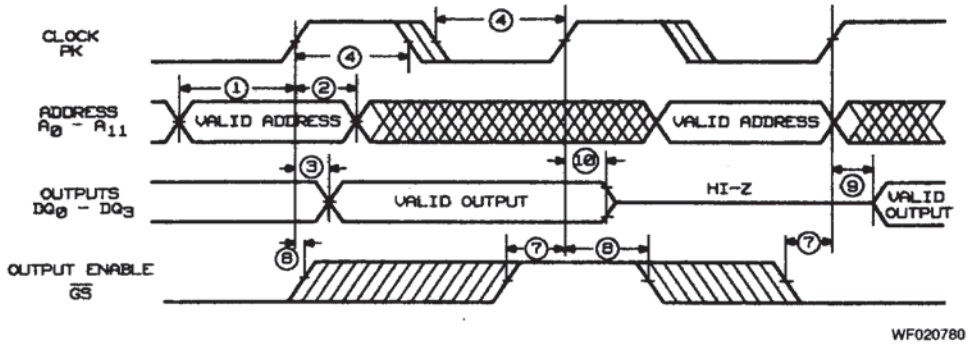
Timing Set 1. Using Asynchronous Enable



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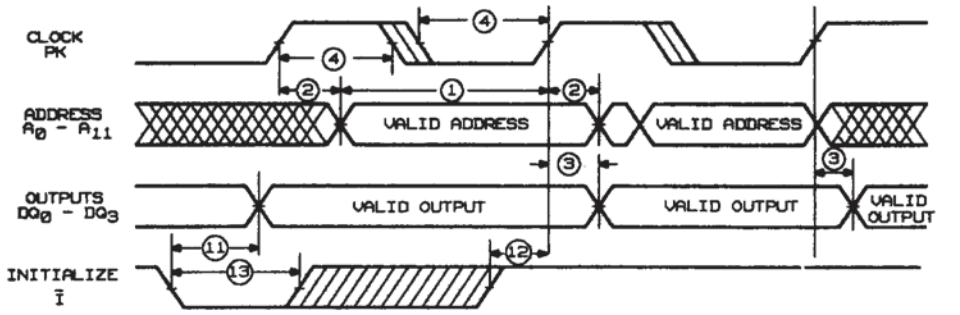
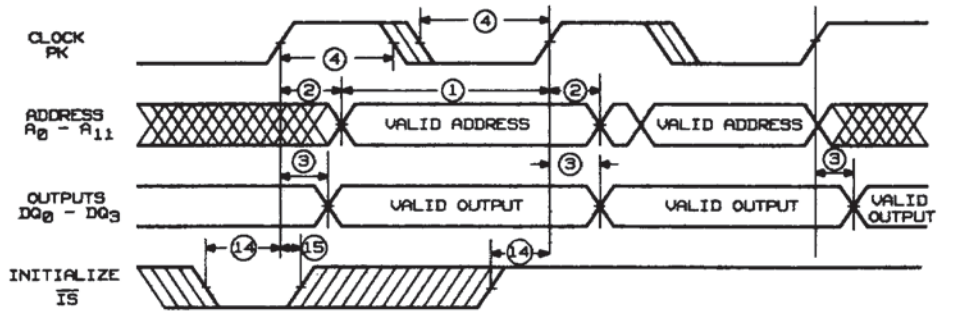
Timing Set 2. Using Synchronous Enable

SWITCHING WAVEFORMS (Cont'd.)



Timing Set 3. Using Asynchronous Initialize



Timing Set 4. Using Synchronous Initialize

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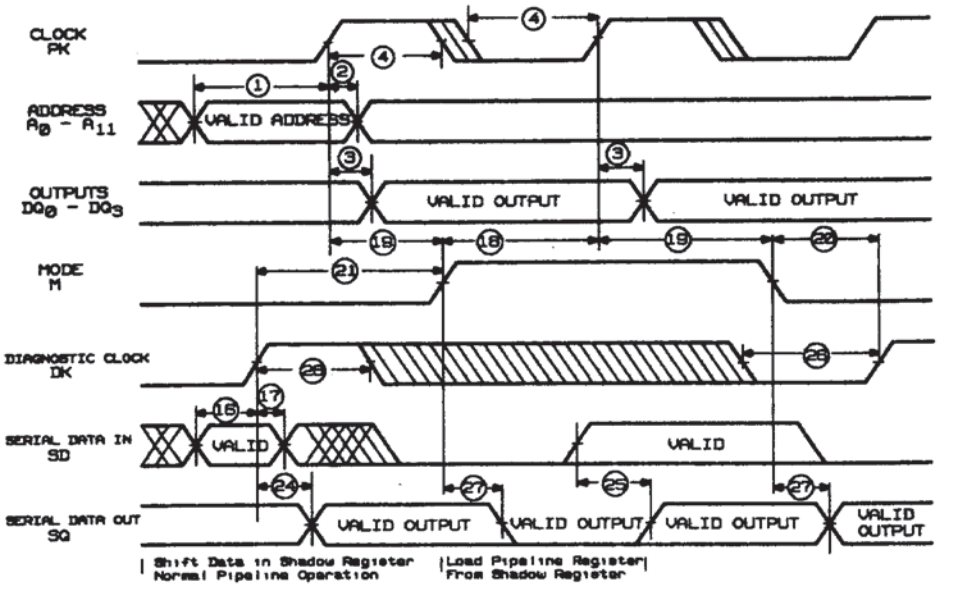
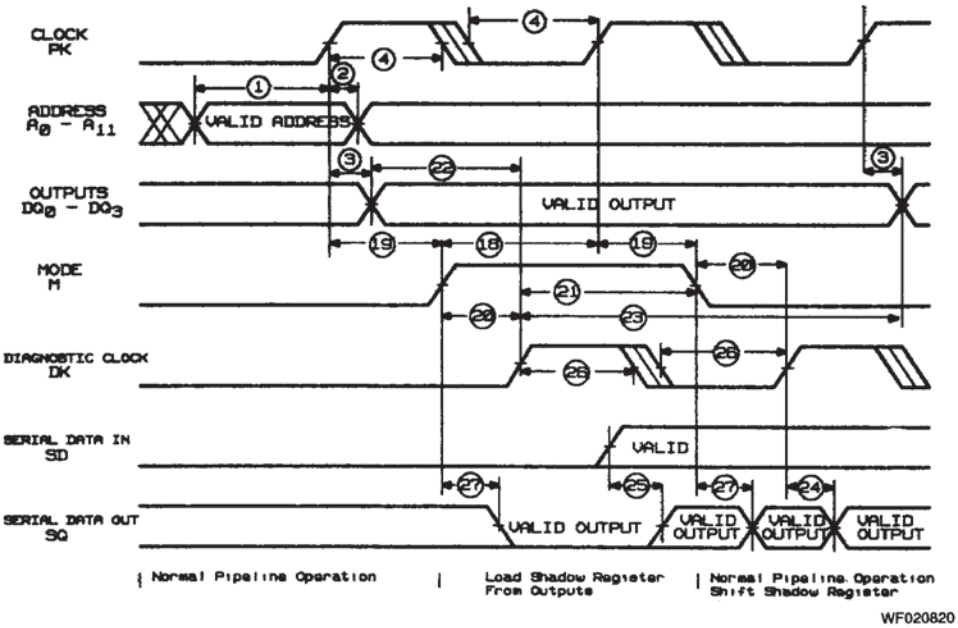
SWITCHING WAVEFORMS (Cont'd.)

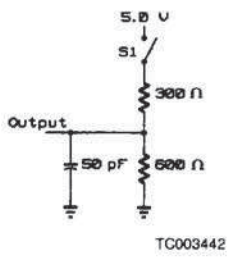


Timing Set 5. Diagnostic Test Mode (System Control)

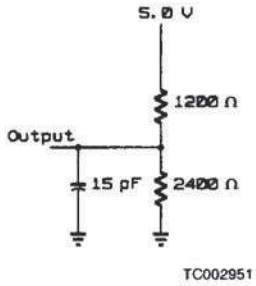


Timing Set 6. Diagnostic Test Mode (System Observation)

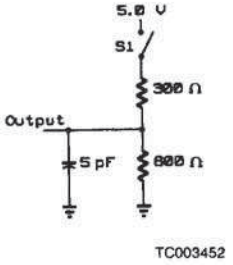
SWITCHING TEST CIRCUITS



A. Output Load for $DQ_0 - DQ_3$



B. Output Load for SQ



C. Output Load for TGHDQZ and TPKHDQZ on Outputs $DQ_0 - DQ_3$

Notes: 1. All devices test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

NOTES ON TESTING

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1μFarad or larger capacitor and a 0.01μFarad or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

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