AM2940

DMA Address Generator

The AM2940, a 28-pin member of AMD's AM2900 family of Low-Power Schottky bipolar LSI chips, is a high-speed, cascadable, eight-bit wide Direct Memory Access Address Generator slice. Any number of AM2940's can be cascaded to form larger addresses.

The primary function of the device is to generate sequential memory addresses for use in the sequential transfer of data to or from a memory. It also maintains a data word count and generates a DONE signal when a programmable terminal count has been reached. The device is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am2940

DMA Address Generator

DISTINCTIVE CHARACTERISTICS

- **DMA Address Generation**
  Generates memory address, word count and DONE signal for DMA transfer operation.
- **Expandable Eight-bit Slice**
  Any number of Am2940's can be cascaded to form larger memory addresses – three devices address 16 megawords.
- **Repeat Data Transfer Capability**
  Initial memory address and word count are saved so that the data transfer can be repeated.
- **Programmable Control Modes**
  Provides four types of DMA transfer control plus memory address increment/decrement.
- **High Speed, Bipolar LSI**
  Advanced Low-Power Schottky TTL technology provides typical CLOCK to DONE propagation delay of 50ns and 24mA output current sink capability.
- **Microprogrammable**
  Executes 8 different instructions.

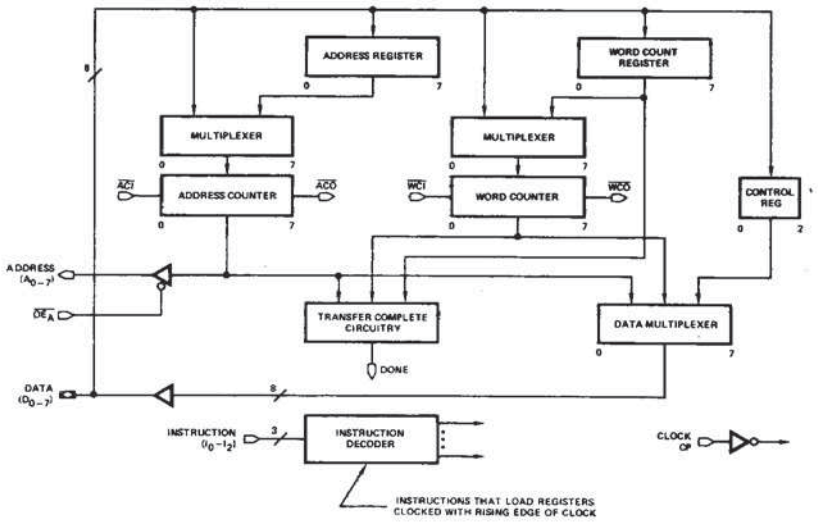
GENERAL DESCRIPTION

The Am2940, a 28-pin member of Advanced Micro Devices' Am2900 family of Low-Power Schottky bipolar LSI chips, is a high-speed, cascadable, eight-bit wide Direct Memory Access Address Generator slice. Any number of Am2940's can be cascaded to form larger addresses.

The primary function of the device is to generate sequential memory addresses for use in the sequential transfer of data to or from a memory. It also maintains a data word count and generates a DONE signal when a programmable terminal count has been reached. The device is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory.

The Am2940 can be programmed to increment or decrement the memory address in any of four control modes, and executes eight different instructions. The initial address and word count are saved internally by the Am2940 so that they can be restored later in order to repeat the data transfer operation.

BLOCK DIAGRAM



Am2940 DMA Address Generator BD002450

For applications information see the last part of this data sheet and Chapter VII of *Bit Slice Microprocessor Design*, by Mick and Brick, McGraw-Hill Publishers.

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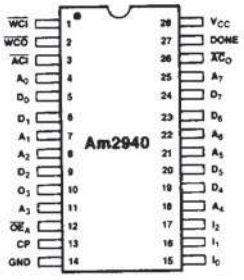
CONNECTION DIAGRAM
Top View

D-28

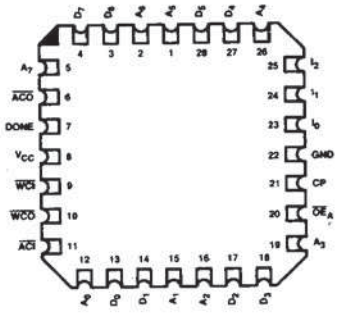
CD004620

F-28



CD004630

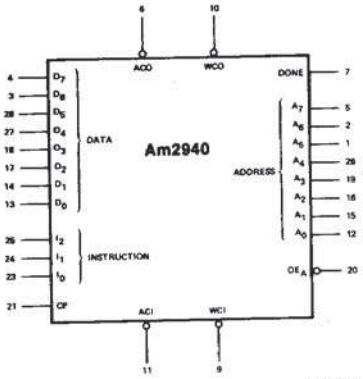
Chip-Pak™ L-28



CD004740

Note: Pin 1 is marked for orientation

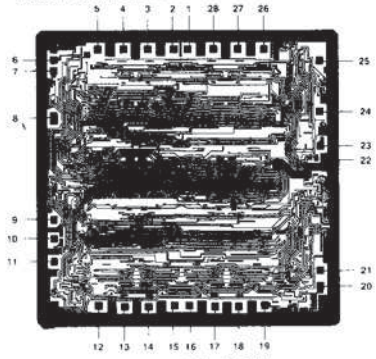
LOGIC SYMBOL



LS001021

METALLIZATION AND PAD LAYOUT

Note: Numbers refer to DIP pin connection.



DIE SIZE: 0.178" x 0.181"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2940 D C B

- B — Screening Option: Blank – Standard processing; B – Burn-in
- C — Temperature (See Operating Range): C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D – 28-pin CERDIP; F – 28-pin flatpak; L – 28-pin leadless chip carrier; X – Dice
- Am2940 — Device type: DMA Address Generator

Valid Combinations	
Am2940	DC, DCB, DMB FMB LC, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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PIN DESCRIPTION

Pin No.	Name	I/O	Description
23, 24, 25	I_{0-2}	I	Selects one of eight instructions.
11	$\overline{ACI}$	I	Carry-in to the address counter.
6	$\overline{ACO}$	O	Carry-out from the address counter.
9	$\overline{WCI}$	I	Carry-in to the word counter.
10	$\overline{WCO}$	O	Carry-out from the word counter.
	D_{0-7}	I/O	External data.
	A_{0-7}	O	Address outputs under control of Output Enable input, $\overline{OE}_A$.
20	$\overline{OE}_A$	I	Address output enable.
7	DONE	O	Transfer complete signal.
21	CP	I	Clock input. Registers and counters change on the LOW-to-HIGH transition.

Am2940 ARCHITECTURE

As shown in the Block Diagram, the Am2940 consists of the following:

- A three-bit Control Register
- An eight-bit Address Counter with input multiplexer
- An eight-bit Address Register
- An eight-bit Word Counter with input multiplexer
- An eight-bit Word Count Register
- Transfer complete circuitry
- An eight-bit wide data multiplexer with three-state output buffers
- Three-state address output buffers with external output enable control
- An instruction decoder

Control Register

Under instruction control, the Control Register can be loaded or read from the bidirectional DATA lines D_0-D_7. Control Register bits 0 and 1 determine the Am2940 Control Mode, and bit 2 determines whether the Address Counter increments or decrements. Figure 1 defines the Control Register format.

Address Counter

The Address Counter, which provides the current memory address, is an eight-bit, binary, up/down counter with full look-ahead carry generation. The Address Carry Input ($\overline{ACI}$) and Address Carry Output ($\overline{ACO}$) allow cascading to accommodate larger addresses. Under instruction control, the Address Counter can be enabled, disabled, and loaded from the DATA inputs, D_0-D_7, or the Address Register. When enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments/decrements on the LOW-to-HIGH transition of the CLOCK input, CP. The Address Counter output can be enabled onto the three-state ADDRESS outputs A_0-A_7 under control of the Output Enable input, $\overline{OE}_A$.

Address Register

The eight-bit Address Register saves the initial address so that it can be restored later in order to repeat a transfer operation. When the LOAD ADDRESS instruction is executed, the Address Register and Address Counter are simultaneously loaded from the DATA inputs, D_0-D_7.

Word Counter and Word Count Register

The Word Counter and Word Count Register, which maintain and save a word count, are similar in structure and operation to the Address Counter and Address Register, with the exception that the Word Counter increments in Control Modes 1 and 3, decrements in Control Mode 0, and is disabled in Control Mode 2. The LOAD WORD COUNT instruction simultaneously loads the Word Counter and Word Count Register.

Transfer Complete Circuitry

The Transfer Complete Circuitry is a combinational logic network which detects the completion of the data transfer operation in three Control Modes and generates the DONE output signal. The DONE signal is an open-collector output, which can be dot-anded between chips.

Data Multiplexer

The Data Multiplexer is an eight-bit wide, 3-input multiplexer which allows the Address Counter, Word Counter, and Control Register to be read at the DATA lines, D_0-D_7. The Data Multiplexer and three-state Data Output Buffers are instruction controlled.

Address Output Buffers

The three-state Address Output Buffers allow the Address Counter output to be enabled onto the ADDRESS lines, A_0-A_7, under external control. When the Output Enable input, $\overline{OE}_A$, is LOW, the Address output buffers are enabled; when $\overline{OE}_A$ is HIGH, the ADDRESS lines are in the high-impedance state. The Address and Data Output Buffers can sink 24mA output current over the commercial operating range.

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the INSTRUCTION inputs, I_0-I_2 and Control Register bits, CR_0-CR_1.

Clock

The CLOCK input, CP is used to clock the Address Register, Address Counter, Word Count Register, Word Counter, and Control Register, all on the LOW-to-HIGH transition of the CP signal.

Control Register

CR_2	CR_1	CR_0

CR_1	CR_0	Control Mode Number	Control Mode Type	Word Counter	DONE Output Signal	
					$\overline{WCI}$ = LOW	$\overline{WCI}$ = HIGH
L	L	0	Word Count Equals Zero	Decrement	HIGH when Word Counter = 1	HIGH when Word Counter = 0
L	H	1	Word Count Compare	Increment	HIGH when Word Counter + 1 = Word Count Reg.	HIGH when Word Counter = Word Count Reg.
H	L	2	Address Compare	Hold	HIGH when Word Counter = Address Counter	
H	H	3	Word Counter Carry Out	Increment	Always LOW	

CR_2	Address Counter
L	Increment
H	Decrement

L = LOW
H = HIGH

Figure 1. Control Register Format Definition.

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Am2940 CONTROL MODES

Control Mode 0 – Word Count Equals Zero Mode

In this mode, the LOAD WORD COUNT instruction loads the word count into the Word Count Register and Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter decrements on the LOW-to-HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

Control Mode 1 – Word Count Compare Mode

In this mode the LOAD WORD COUNT instruction loads the word count into the Word Count Register and clears the Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter increments on the LOW-to-HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

Control Mode 2 – Address Compare Mode

In this mode, only an initial and final memory address need be specified. The initial Memory Address is loaded into the Address Register and Address Counter and the final memory address is loaded into the Word Count Register and Word Counter. The Word Counter is always disabled in this mode and serves as a holding register for the final memory address. When the Address Counter is enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments or decrements (depending on Control Register bit 2) on the LOW-to-HIGH transition of the CLOCK input, CP. The Transfer Complete Circuitry compares the Address Counter with the Word Counter and generates the DONE signal during the last word transfer; i.e., when the Address Counter equals the Word Counter.

Control Mode 3 – Word Counter Carry Out Mode

For this mode of operation, the user can load the Word Count Register and Word Counter with the two's complement of the number of data words to be transferred. When the Word Counter is enabled and the $\overline{WCI}$ input is LOW, the Word Counter increments on the LOW-to-HIGH transition of the CLOCK input, CP. A Word Counter Carry Out signal, $\overline{WCO}$, indicates the last data word is being transferred. The DONE signal is not required in this mode and, therefore, is always LOW.

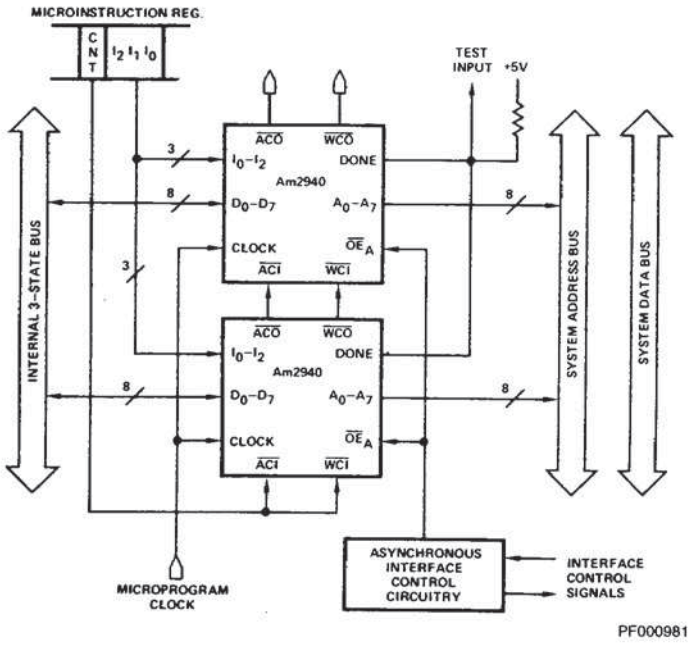

Figure 2. Am2940 Interconnections.

Am2940 INSTRUCTIONS

The Am2940 instruction set consists of eight instructions. Six instructions load and read the Address Counter, Word Counter and Control Register; one instruction enables the Address and Word counters; and one instruction reinitializes the Address and Word Counters. The function of the REINITIALIZE COUNTERS, LOAD WORD COUNT, and ENABLE COUNTERS instructions varies with the Control Mode being utilized. Table 1 defines the Am2940 Instructions as a function of Instruction inputs I_0-I_2 and the four Am2940 Control Modes.

The WRITE CONTROL REGISTER instruction writes DATA input D_0-D_2 into the Control Register; DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The READ CONTROL REGISTER instruction gates the Control Register outputs to DATA lines, D_0-D_2. DATA lines D_3-D_7 are in the HIGH state during this instruction.

The Word Counter can be read using the READ WORD COUNTER instruction, which gates the Word Counter outputs to DATA lines D_0-D_7. The LOAD WORD COUNT instruction is Control Mode dependent. In Control Modes 0, 2, and 3, DATA inputs D_0-D_7 are written into both the Word Count Register and Word Counter. In Control Mode 1, DATA inputs D_0-D_7 are written into the Word Count Register and the Word Counter is cleared.

The READ ADDRESS COUNTER instruction gates the Address Counter outputs to DATA lines D_0-D_7, and the LOAD ADDRESS instruction writes DATA inputs D_0-D_7 into both the Address Register and Address Counter.

In Control Modes 0, 1, and 3, the ENABLE COUNTERS instruction enables both the Address and Word Counters; in Control Mode 2, the Address Counter is enabled and the Word Counter holds its contents. When enabled and the carry input is active, the counters increment on the LOW-to-HIGH transition of the CLOCK input, CP. Thus, with this instruction applied, counting can be controlled by the carry inputs.

The REINITIALIZE COUNTERS instruction also is Control Mode dependent. In Control Modes 0, 2, and 3, the contents of the Address Register and Word Count Register are transferred to the respective Address Counter and Word Counter; in Control Mode 1, the content of the Address Register is transferred to the Address Counter and the Word Counter is cleared. The REINITIALIZE COUNTERS instruction allows a data transfer operation to be repeated without reloading the address and word count from the DATA lines.

TABLE I. Am2940 INSTRUCTIONS

I_2	I_1	I_0	Octal Code	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Address Reg.	Address Counter	Control Register	Data D_0–D_7
L	L	L	0	WRITE CONTROL REGISTER	WRCR	0,1,2,3	HOLD	HOLD	HOLD	HOLD	D_0–D_2 → CR	INPUT
L	L	H	1	READ CONTROL REGISTER	RDCR	0,1,2,3	HOLD	HOLD	HOLD	HOLD	HOLD	CR → D_0–D_2 (Note 1)
L	H	L	2	READ WORD COUNTER	RDWC	0,1,2,3	HOLD	HOLD	HOLD	HOLD	HOLD	WC → D
L	H	H	3	READ ADDRESS COUNTER	RDAC	0,1,2,3	HOLD	HOLD	HOLD	HOLD	HOLD	AC → D
H	L	L	4	REINITIALIZE COUNTERS	REIN	0,2,3	HOLD	WCR → WC	HOLD	AR → AC	HOLD	Z
						1	HOLD	ZERO → WC	HOLD	AR → AC	HOLD	Z
H	L	H	5	LOAD ADDRESS	LDAD	0,1,2,3	HOLD	HOLD	D → AR	D → AC	HOLD	INPUT
H	H	L	6	LDAD WORD COUNT	LDWC	0,2,3	D → WR	D → WC	HOLD	HOLD	HOLD	INPUT
						1	D → WR	ZERO → WC	HOLD	HOLD	HOLD	INPUT
H	H	H	7	ENABLE COUNTERS	ENCT	0,1,3	HOLD	ENABLE COUNT	HOLD	ENABLE COUNT	HOLD	Z
						2	HOLD	HOLD	HOLD	ENABLE COUNT	HOLD	Z

CR = Control Reg.
AR = Address Reg.
AC = Address Counter
WCR = Word Count Reg.
WC = Word Counter
D = Data
L = LOW
H = HIGH
Z = High Impedance

Note 1: Data Bits D_3-D_7 are high during this instruction.

APPLICATIONS

The Am2940 is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory. One or more Am2940's can be used in each peripheral controller of a distributed DMA system to provide the memory address and word count required for DMA operation.

Figure 3 shows a block diagram of an example microprogrammed DMA peripheral controller. The Am2910A Microprogram Sequencer, Microprogram Memory, and the Microinstruction Register form the microprogram control portion of this peripheral controller. The Am2940 generates the memory address and maintains the word count required for DMA operation. An internal three-state bus provides the communication path between the Microinstruction Register, the Am2917 Data Transceivers, the Am2940, the Am2901C Microprocessor, and the Device Interface Circuitry.

The Am2940 interconnections are shown in detail in Figure 2. Two Am2940's are cascaded to generate a sixteen-bit address. The Am2940 ADDRESS and DATA output current sink capability is 24mA over the commercial operating range. This allows the Am2940's to drive the System Address Bus and Internal Three-State Bus directly, thereby eliminating the need for separate bus drivers. Three-bits in the Microinstruction Register provide the Am2940 Instruction Inputs, I_0-I_2. The microprogram clock is used to clock the Am2940's and, when the ENABLE COUNTERS instruction is applied, address and word counting is controlled by the CNT bit of the Microinstruction Register.

Asynchronous interface control circuitry generates System Bus control signals and enables the Am2940 Address onto the System Address Bus at the appropriate time. The open-collector DONE outputs are dot-anded and used as a test input to the Am2910A Microprogram Sequencer.

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Refer to Page 13-1 for Essential Information on Military Devices

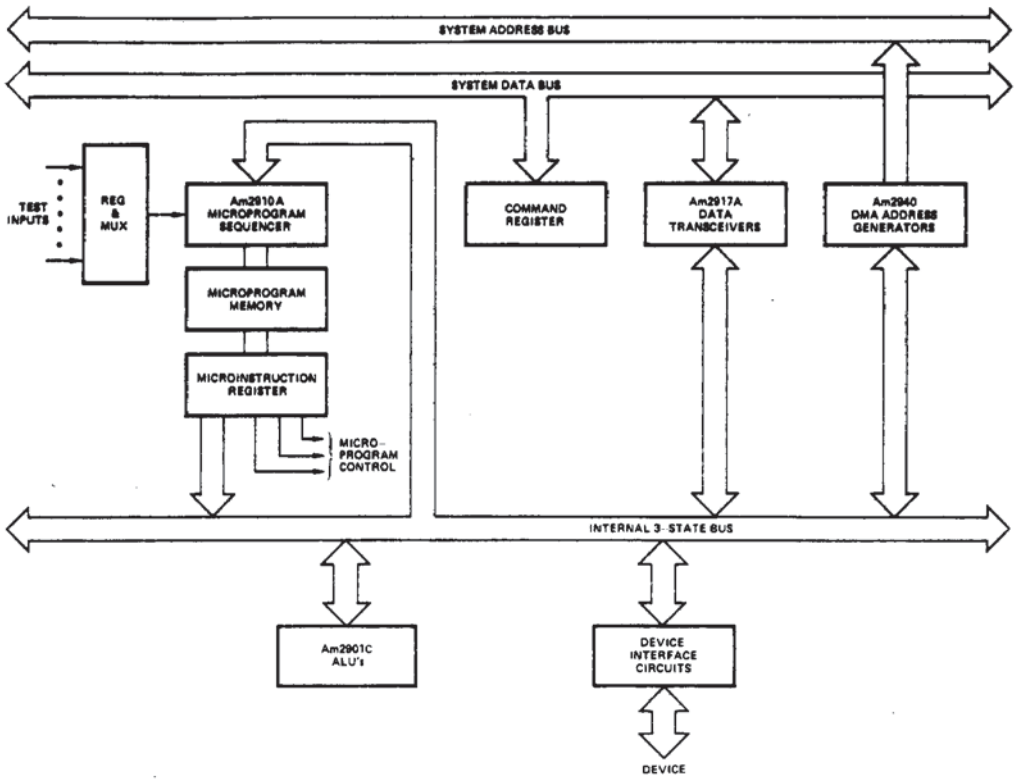

Figure 3. DMA Peripheral Controller Block Diagram.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL I_{OH} = −1.0mA		2.4			Volts
			COM'L I_{OH} = −2.6mA					
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL} (Note 5)	$\overline{WCO}$, $\overline{ACO}$	MIL I_{OL} = 8.0mA			0.5	Volts
				COM'L I_{OL} = 12mA				
			A_{0-7}, D_{0-7} DONE	MIL I_{OL} = 16mA				
				COM'L I_{OL} = 24mA				
V_{IH}	Input HIGH Level (Note 4)	Guaranteed input Logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed Input Logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		D_{0-7}			−0.15	mA
				All Others			−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		D_{0-7}			150	µA
				All Others			40	
I_{CEX}	Output Leakage on DONE	V_{CC} = MAX, V_O = 5.5V					250	µA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX + 0.5V, V_O = 0.5V			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX, $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V	A_{0-7}			−50	µA
				D_{0-7}			−150	
I_{OZH}			V_{OUT} = 2.4	A_{0-7}			50	
				D_{0-7}			150	
I_{CC}	Power Supply Current	V_{CC} = MAX	Am2940DC	T_A = 0°C to +70°C			290	mA
				T_A = +70°C			235	
			Am2940DM, FM	T_C = −55°C to +125°C			315	
				T_C = +125°C			225	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be static tested in a noise-free environment (not functionally tested).
5. I_{OL} limit on A_i and D_i (i = 0 to 7) applies to either output individually, but not both at the same time. The sum of the loading on A_i plus D_i is limited to 24mA MIL or 32mA COM'L.

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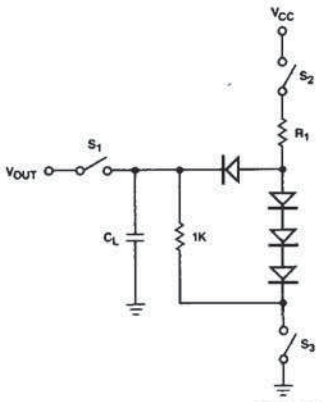
Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING TEST CIRCUIT

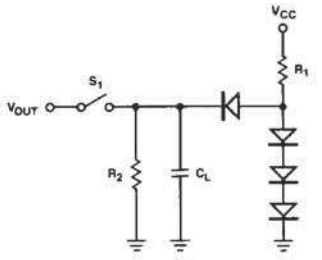
A. THREE-STATE OUTPUTS



TC001100

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{1K}}$$

B. NORMAL OUTPUTS

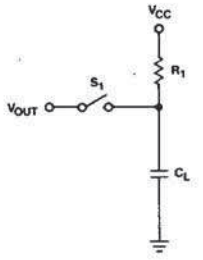


TC001081

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{R_2}}$$

C. OPEN-COLLECTOR OUTPUTS



TC001220

$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, stray wiring and capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2940 (DIP)

Pin# (DIP)	Pin Label	Test Circuit	R_1	R_2
–	A_{0-7}	A	220	1K
–	D_{0-7}	A	220	1K
6	$\overline{ACO}$	B	470	2.4K
7	DONE	C	270	–
10	$\overline{WCO}$	B	470	2.4K

For additonal information on testing, see section "Guidelines on Testing Am2900 Family Devices."

SWITCHING CHARACTERISTICS

The tables below define the Am2940 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with C_L = 50pF except output disable times ($\overline{OE}$ to A and I to D) which are specified or a 5pF load.

I. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

Am2940DC (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	24	4
I_{012}	46	5
$\overline{ACI}$	30	4
$\overline{WCI}$ (Note 1)	30	3

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	20	-	-	-	-
$\overline{WCI}$ (Note 2)	-	20	-	46	-
I_{0-2}	-	-	-	-	37
CP (Note 3)	58	58	54	85	-

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	34	ns
Maximum Clock Frequency	17	MHz

D. Enable/Disbable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	35	35	ns
$\overline{OE}$	A_{0-7}	25	25	ns

II. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

Am2940DM, FM (T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	27	6
I_{012}	49	5
$\overline{ACI}$	34	5
$\overline{WCI}$ (Note 1)	34	5

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	21	-	-	-	-
$\overline{WCI}$ (Note 2)	-	21	-	54	-
I_0-I_2	-	-	-	-	41
CP (Note 3)	64	64	62	88	-

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	35	ns
Maximum Clock Frequency	16	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	42	42	ns
$\overline{OE}$	A_{0-7}	30	30	ns

Notes:
1. Control modes 0, 1, and 3 only.
2. $\overline{WCI}$ to DONE occurs only in control modes 0 and 1.
3. CP to DONE occurs only in control modes 0, 1, and 2.

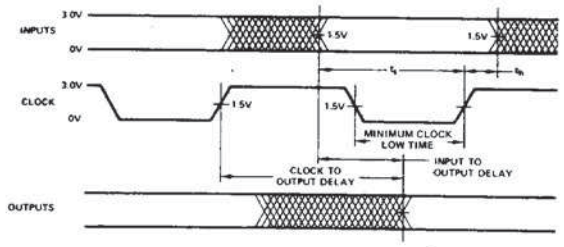


Figure 4. Switching Waveforms.

See Tables A for t_s and t_h for various inputs. See Tables B for combinational delays from clock and other inputs to outputs.

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current when the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.