AM3448A

IEEE-488 Quad Bidirectional Transceiver

The AM3448A is a quad bidirectional transceiver meeting the requirement of IEEE-488 standard digital interface for programmable instrumentation for the driver, receiver, and composite device load. One pull-up enable input is provided for each pair of transceivers which controls the operating mode of the driver outputs as either an open collector or active pull-up configuration.

The receivers feature input hysteresis for improved noise immunity in system applications. The device bus (receiver input) changes from standard bus loading to a high impedance load when power is removed. In addition no spurious noise is generated on the bus during power-up or power-down.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am3448A

IEEE-488 Quad Bidirectional Transceiver

DISTINCTIVE CHARACTERISTICS

- Four independent driver/receiver pairs
- Three-state outputs
- High impedance inputs
- Receiver hysteresis – 600mV (Typ.)
- Fast Propagation Times – 15-20ns (Typ.)
- TTL compatible receiver outputs
- Single +5 volt supply
- Open collector driver output option with internal passive pull up
- Power up/power down protection (No invalid information transmitted to bus)
- No bus loading when power is removed from device
- Required termination characteristics provided
- Advanced Schottky processing
- 100% product assurance screening to MIL-STD-883 requirements

GENERAL DESCRIPTION

The Am3448A is a quad bidirectional transceiver meeting the requirement of IEEE-488 standard digital interface for programmable instrumentation for the driver, receiver, and composite device load. One pull-up enable input is provided for each pair of transceivers which controls the operating mode of the driver outputs as either an open collector or active pull-up configuration.

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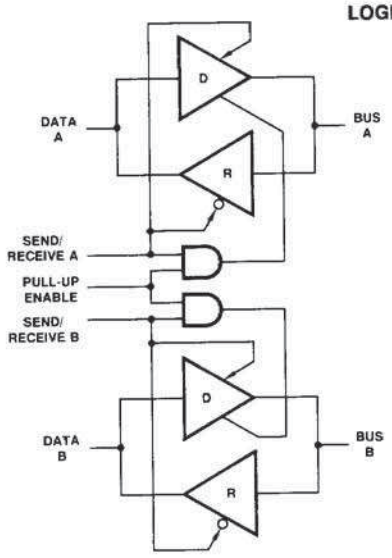
LOGIC DIAGRAM



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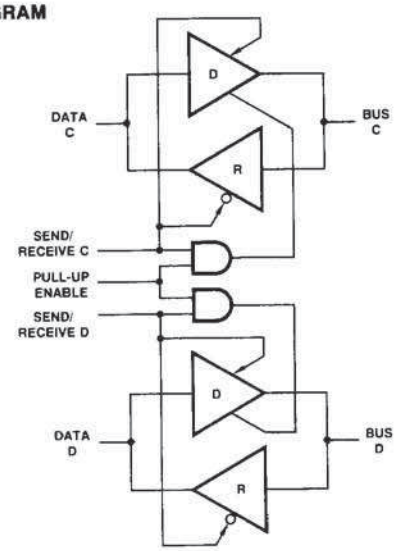

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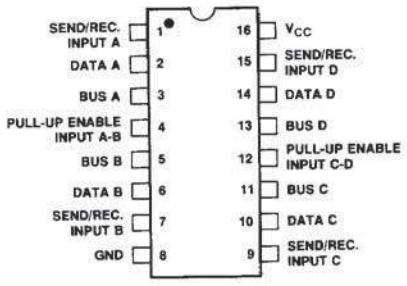
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +70°C	MC3448AL
Molded DIP	0°C to +70°C	MC3448AP
Dice	0°C to +70°C	AM3448AX

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

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ABSOLUTE MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Driver Output Current	150mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am3448A T_A = 0°C to 70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V

DC ELECTRICAL CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
Bus Characteristics							
$V_{(BUS)}$	Bus Voltage	Bus Pin Open, $V_{I(S/R)}$ = 0.8V		2.75		3.7	Volts
$V_{IC(BUS)}$		$I_{(BUS)}$ = −12mA				−1.5	
$I_{(BUS)}$	Bus Current	5.0V ≤ $V_{(BUS)}$ ≤ 5.5V		0.7		2.5	mA
		$V_{(BUS)}$ = 0.5V		−1.3		−3.2	
		V_{CC} = 0V, 0V ≤ $V_{(BUS)}$ ≤ 2.75V				0.04	
Driver Characteristics							
$V_{IC(D)}$	Driver Input Clamp Voltage	$V_{I(S/R)}$ = 2.0V, $I_{IC(D)}$ = −18mA				−1.5	Volts
$V_{OH(D)}$	Driver Output Voltage − High Logic State	$V_{I(S/R)}$ = 2.0V, $V_{IH(D)}$ = 2.0V, $V_{IH(E)}$ = 2.0V, I_{OH} = −5.2mA		2.5			Volts
$V_{OL(D)}$	Driver Output Voltage − Low Logic State	$V_{I(S/R)}$ = 2.0V, $I_{OL(D)}$ = 48mA				0.5	Volts
$I_{OS(D)}$	Output Short Circuit Current	$V_{I(S/R)}$ = 2.0V, $V_{IH(D)}$ = 2.0V $V_{IH(E)}$ = 2.0V		−30		−120	mA
$V_{IH(D)}$	Driver Input Voltage − High Logic State	$V_{I(S/R)}$ = 2.0V		2.0			Volts
$V_{IL(D)}$	Driver Input Voltage − Low Logic State	$V_{I(S/R)}$ = 2.0V				0.8	Volts
$I_{I(D)}$	Driver Input Current − Data Pins	$V_{I(S/R)}$ = $V_{I(E)}$ = 2.0V	0.5 ≤ $V_{I(D)}$ ≤ 2.7V	−200		40	μA
$I_{IB(D)}$			$V_{I(D)}$ = 5.5V			200	
Receiver Characteristics							
$V_{HYS(R)}$	Receiver Input Hysteresis	$V_{I(S/R)}$ = 0.8V		400	600		mV
$V_{ILH(R)}$	Receiver Input Threshold	$V_{I(S/R)}$ = 0.8V, Low to High			1.6	1.8	Volts
$V_{IHL(R)}$		$V_{I(S/R)}$ = 0.8V, High to Low		0.8	1.0		
$V_{OH(R)}$	Receiver Output Voltage − High Logic State	$V_{I(S/R)}$ = 0.8V, $I_{OH(R)}$ = −800μA, $V_{(BUS)}$ = 2.0V		2.7			Volts
$V_{OL(R)}$	Receiver Output Voltage − Low Logic State	$V_{I(S/R)}$ = 0.8V, $I_{OL(R)}$ = 16mA, $V_{(BUS)}$ = 0.8V				0.5	Volts
$I_{OS(R)}$	Receiver Output Short Circuit Current	$V_{I(S/R)}$ = 0.8V, $V_{(BUS)}$ = 2.0V		−15		−75	mA
Enable, Send/Receive Characteristics							
$I_{I(S/R)}$	Input Current − Send/Receive	0.5 ≤ $V_{I(S/R)}$ ≤ 2.7V		−100		20	μA
$I_{IB(S/R)}$		$V_{I(S/R)}$ = 5.5V				100	
$I_{I(E)}$	Input Current − Enable	0.5 ≤ $V_{I(E)}$ ≤ 2.7V		−200		20	μA
$I_{IB(E)}$		$V_{I(E)}$ = 5.5V				100	
Power Supply Current							
I_{CCL}	Power Supply Current	Listening Mode − All Receivers On			63	85	mA
I_{CCH}		Talking Mode − All Drivers On			106	125	

Note 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C unless otherwise noted)

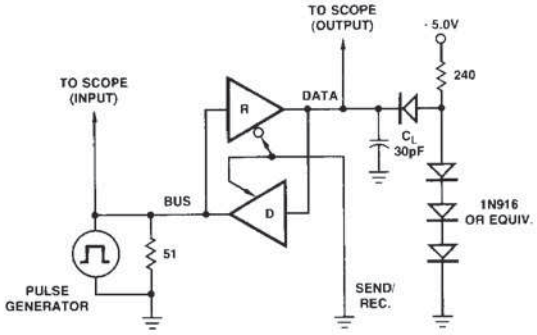
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
$t_{PLH(D)}$	Propagation Delay of Driver (Fig. 2)	Output Low to High	–		15	ns
$t_{PHL(D)}$		Output High to Low			17	
$t_{PLH(R)}$	Propagation Delay of Receiver (Fig. 1)	Output Low to High	–		25	ns
$t_{PHL(R)}$		Output High to Low	–		23	
$t_{PHZ(R)}$	Propagation Delay Time – Send/Receiver to Data (Fig. 4)	Logic High to Third State	–		30	ns
$t_{PZH(R)}$		Third State to Logic High	–		30	
$t_{PLZ(R)}$		Logic Low to Third State	–		30	
$t_{PZL(R)}$		Third State to Logic Low			30	
$t_{PHZ(D)}$	Propagation Delay Time – Send/Receiver to Bus (Fig. 3)	Logic High to Third State	–		30	ns
$t_{PZH(D)}$		Third State to Logic High	–		30	
$t_{PLZ(D)}$		Logic Low to Third State	–		30	
$t_{PZL(D)}$		Third State to Logic Low			30	
$t_{POFF(E)}$	Turn-On Time – Enable to Bus (Fig. 5)	Pull-Up Enable to Open Collector	–		30	ns
$t_{PON(E)}$		Open Collector to Pull-Up Enable	–		20	

TRUTH TABLE

Send/Rec.	Enable	Into Flow	Comments
0	X	Bus → Data	
1	1	Data → Bus	Active Pull-Up
1	0	Data → Bus	Open Collector

X = Don't Care

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS



*Includes Jig and Probe Capacitance.

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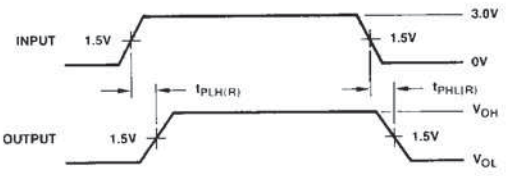
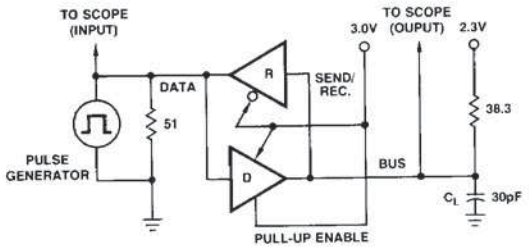


f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0$ns (10-90%)
Duty Cycle = 50%

LIC-450

Figure 1. Bus Input to Data Output (Receiver).



*Includes Jig and Probe Capacitance.

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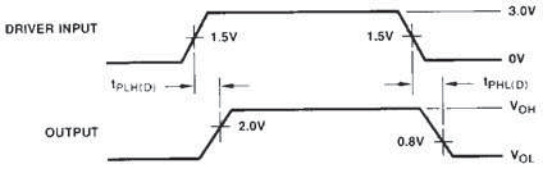

f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0$ns (10-90%)
Duty Cycle = 50%

LIC-452

Figure 2. Data Input to Bus Output (Driver).

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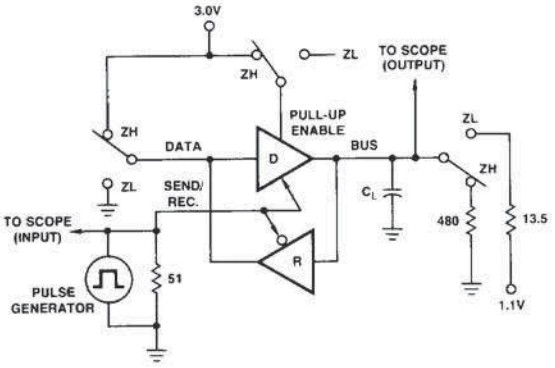
PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS (Cont.)



C_L = 15pF (Includes Jig and Probe Capacitance)

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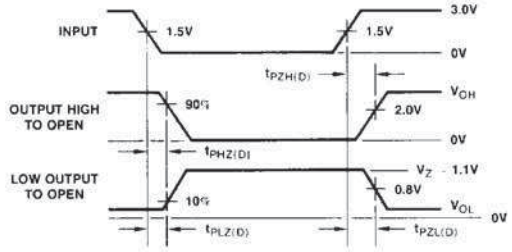
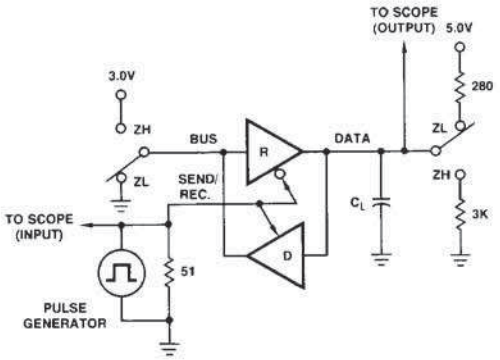


f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0$ns (10-90%)
Duty Cycle = 50%

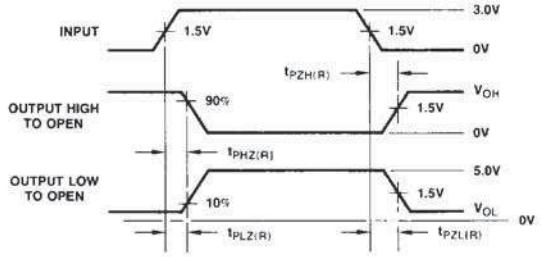
LIC-454

Figure 3. Send/Receive Input to Bus Output (Driver).



C_L = 15pF (Includes Jig and Probe Capacitance)

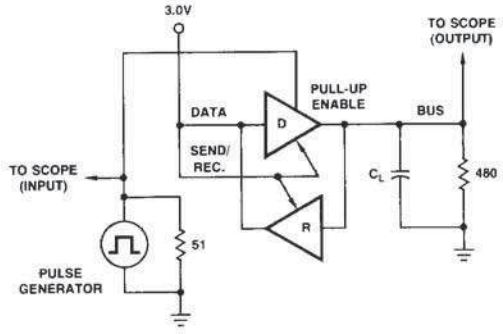
LIC-455



f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0$ns (10-90%)
Duty Cycle = 50%

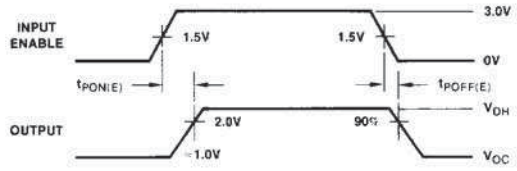
LIC-456

Figure 4. Send/Receive Input to Data Output (Receiver).



C_L = 15pF (Includes Jig and Probe Capacitance)

LIC-457



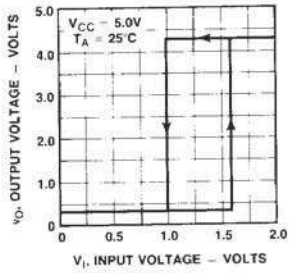
f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0$ns (10-90%)
Duty Cycle = 50%

LIC-458

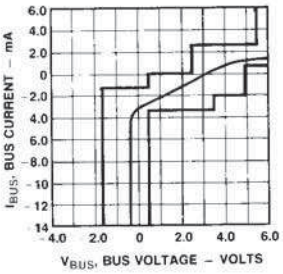
Figure 5. Enable Input to Bus Output (Driver).

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS (Cont.)

TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS



TYPICAL BUS LOAD LINE



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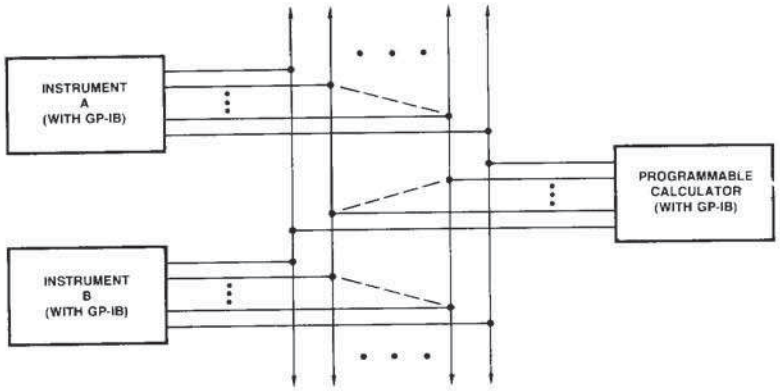
TYPICAL APPLICATION



16 LINES TOTAL
(FOUR Am3448A'S FOR EACH BUS INTERFACE)

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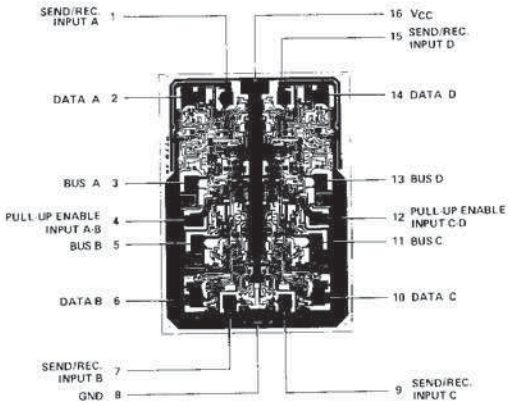
TYPICAL MEASUREMENT SYSTEM APPLICATION

Metallization and Pad Layout



DIE SIZE .063" X .087"

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