AM79C940B

Media Access Controller for Ethernet (MACE)

The Media Access Controller for Ethernet (MACE) chip is a CMOS VLSI device designed to provide flexibility in customized LAN design. The MACE device is specifically designed to address applications where multiple I/O peripherals are present, and a centralized or system specific DMA is required. The high speed, 16-bit synchronous system interface is optimized for an external DMA or I/O processor system, and is similar to many existing peripheral devices such as SCSI and serial link controllers.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FINAL

Am79C940

Media Access Controller for Ethernet (MACE™)

DISTINCTIVE CHARACTERISTICS

- **Integrated Controller with Manchester encoder/decoder and 10BASE-T transceiver and AUI port**
- **Supports IEEE 802.3/ANSI 8802-3 and Ethernet standards**
- **84-pin PLCC and 100-pin PQFP Packages**
- **80-pin Thin Quad Flat Pack (TQFP) package available for space critical applications such as PCMCIA**
- **Modular architecture allows easy tuning to specific applications**
- **High speed, 16-bit synchronous host system interface with 2 or 3 cycles/transfer**
- **Individual transmit (136 byte) and receive (128 byte) FIFOs provide increase of system latency and support the following features:**
  - — Automatic retransmission with no FIFO reload
  - — Automatic receive stripping and transmit padding (individually programmable)
  - — Automatic runt packet rejection
  - — Automatic deletion of collision frames
  - — Automatic retransmission with no FIFO reload
- **Direct slave access to all on board configuration/status registers and transmit/ receive FIFOs**
- **Direct FIFO read/write access for simple interface to DMA controllers or I/O processors**
- **Arbitrary byte alignment and little/big endian memory interface supported**
- **Internal/external loopback capabilities**
- **External Address Detection Interface (EADI™) for external hardware address filtering in bridge/router applications**
- **JTAG Boundary Scan (IEEE 1149.1) test access port interface for board level production test**
- **Integrated Manchester Encoder/Decoder**
- **Digital Attachment Interface (DAI™) allows by-passing of differential Attachment Unit Interface (AUI)**
- **Supports the following types of network interface:**
  - — AUI to external 10BASE2, 10BASE5 or 10BASE-F MAU
  - — DAI port to external 10BASE2, 10BASE5, 10BASE-T, 10BASE-F MAU
  - — General Purpose Serial Interface (GPSI) to external encoding/decoding scheme
  - — Internal 10BASE-T transceiver with automatic selection of 10BASE-T or AUI port
- **Sleep mode allows reduced power consumption for critical battery powered applications**
- **5 MHz-25 MHz system clock speed**
- **Support for operation in industrial temperature range (–40°C to +85°C) available in all three packages**

GENERAL DESCRIPTION

The Media Access Controller for Ethernet (MACE) chip is a CMOS VLSI device designed to provide flexibility in customized LAN design. The MACE device is specifically designed to address applications where multiple I/O peripherals are present, and a centralized or system specific DMA is required. The high speed, 16-bit synchronous system interface is optimized for an external DMA or I/O processor system, and is similar to many existing peripheral devices, such as SCSI and serial link controllers.

The MACE device is a slave register based peripheral. All transfers to and from the system are performed using simple memory or I/O read and write commands. In conjunction with a user defined DMA engine, the MACE chip provides an IEEE 802.3 interface tailored to a specific application. Its superior modular architecture and versatile system interface allow the MACE device to be configured as a stand-alone device or as a connectivity cell incorporated into a larger, integrated system.

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Issue Date: **May 2000**

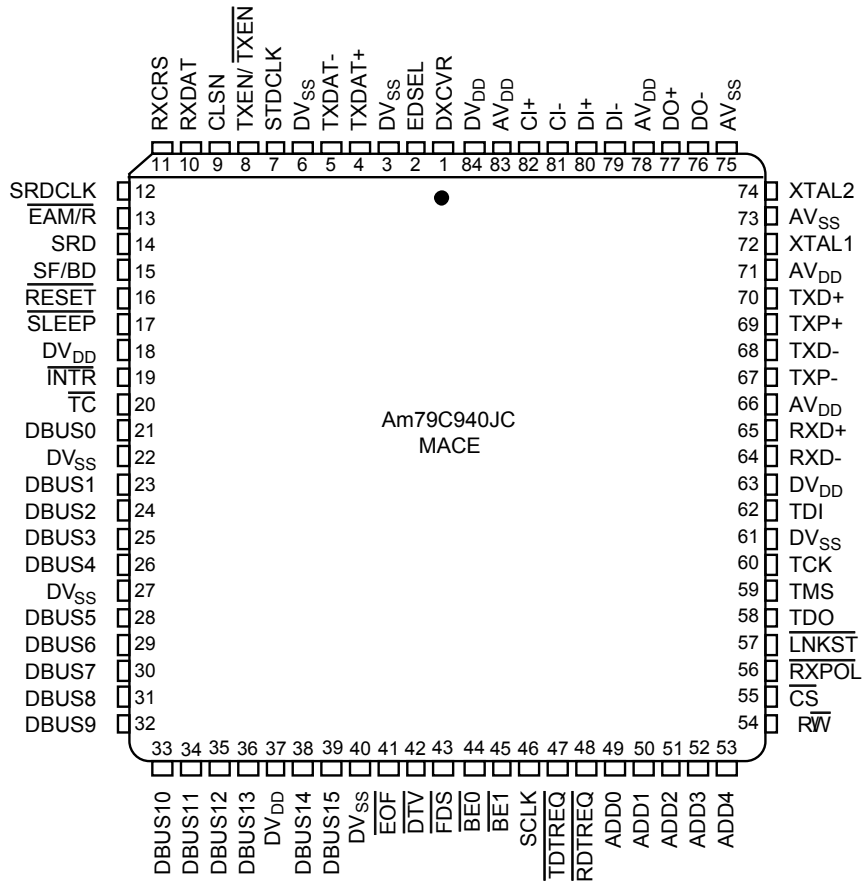
The MACE device provides a complete Ethernet node solution with an integrated 10BASE-T transceiver, and supports up to 25-MHz system clocks. The MACE device embodies the Media Access Control (MAC) and Physical Signaling (PLS) sub-layers of the IEEE 802.3 standard, and provides an IEEE defined Attachment Unit Interface (AUI) for coupling to an external Medium Attachment Unit (MAU). The MACE device is compliant with 10BASE2, 10BASE5, 10BASE-T, and 10BASE-F transceivers.

Additional features also enhance over-all system design. The individual transmit and receive FIFOs optimize system overhead, providing substantial latency during packet transmission and reception, and minimizing intervention during normal network error recovery. The integrated Manchester encoder/decoder eliminates the need for an external Serial Interface Adapter (SIA) in the node system. If support for an external encoding/decoding scheme is desired, the General Purpose Serial Interface (GPSI) allows direct access to/from the MAC. In addition, the Digital Attachment Interface (DAI), which is a simplified electrical attachment specification, allows implementation of MAUs that do not require DC isolation between the MAU and DTE. The DAI port can also be used to indicate transmit, receive, or collision status by connecting LEDs to the port. The MACE device also provides an External Address Detection Interface (EADI) to allow external hardware address filtering in internet working applications.

The Am79C940 MACE chip is offered in a Plastic Leadless Chip Carrier (84-pin PLCC), a Plastic Quad Flat Package (100-pin PQFP), and a Thin Quad Flat Package (TQFP 80-pin). There are several small functional and physical differences between the 80-pin TQFP and the 84-pin PLCC and 100-pin PQFP configurations. Because of the smaller number of pins in the TQFP configuration versus the PLCC configuration, four pins are not bonded out. Though the die is identical in all three package configurations, the removal of these four pins does cause some functionality differences between the TQFP and the PLCC and PQFP configurations. Depending on the application, the removal of these pins will or will not have an effect. (See section: “Pins Removed for TQFP Package and Their Effects.)

With the rise of embedded networking applications operating in harsh environments where temperatures may exceed the normal commercial temperature (0°C to +70°C) window, an industrial temperature (-40°C to +85°C) version is available in all three packages; 84-pin PLCC, 100-pin PQFP and 80-pin TQFP. The industrial temperature version of the MACE Ethernet controller is characterized across the industrial temperature range (-40°C to +85°C) within the published power supply specification (4.75 V to 5.25 V; i.e., ±5% V_{CC}). Thus, conformance of MACE performance over this temperature range is guaranteed by the design and characterization monitor.

CONNECTION DIAGRAMS
PL 084
PLCC PACKAGE



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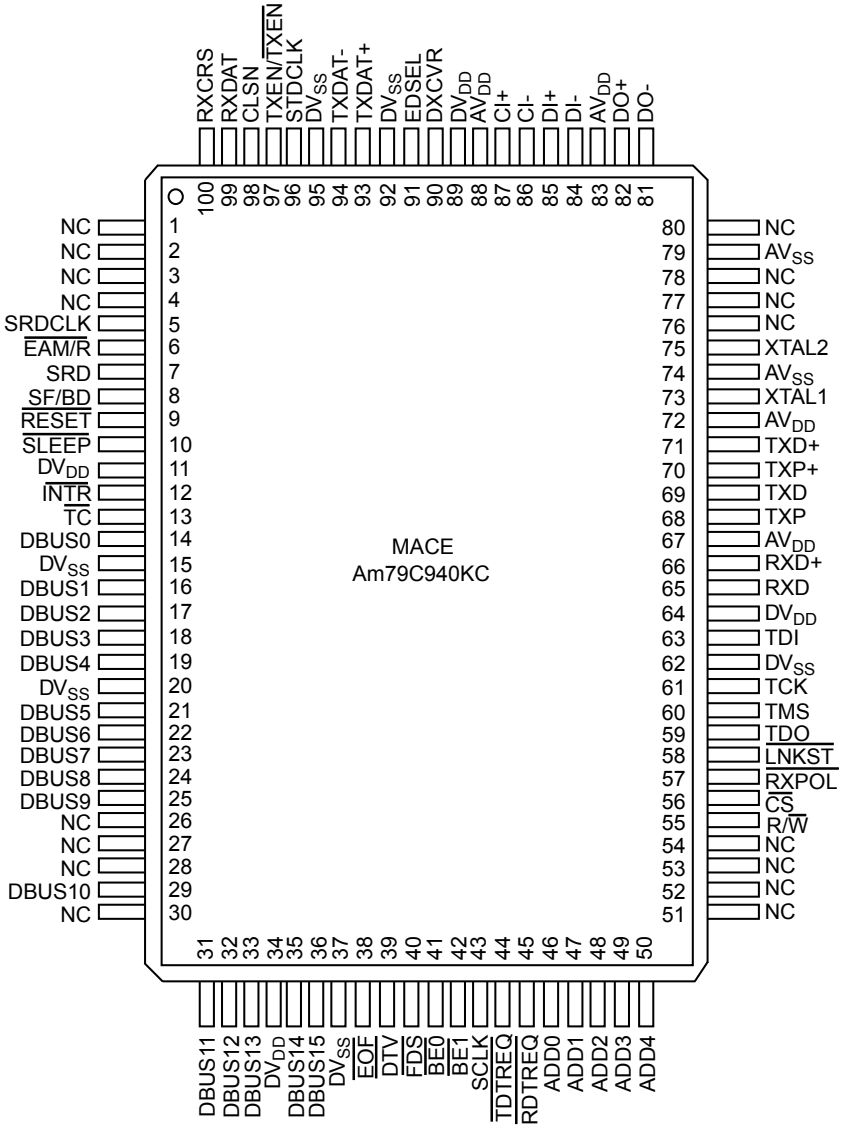
CONNECTION DIAGRAMS
PQR100
PQFP PACKAGE



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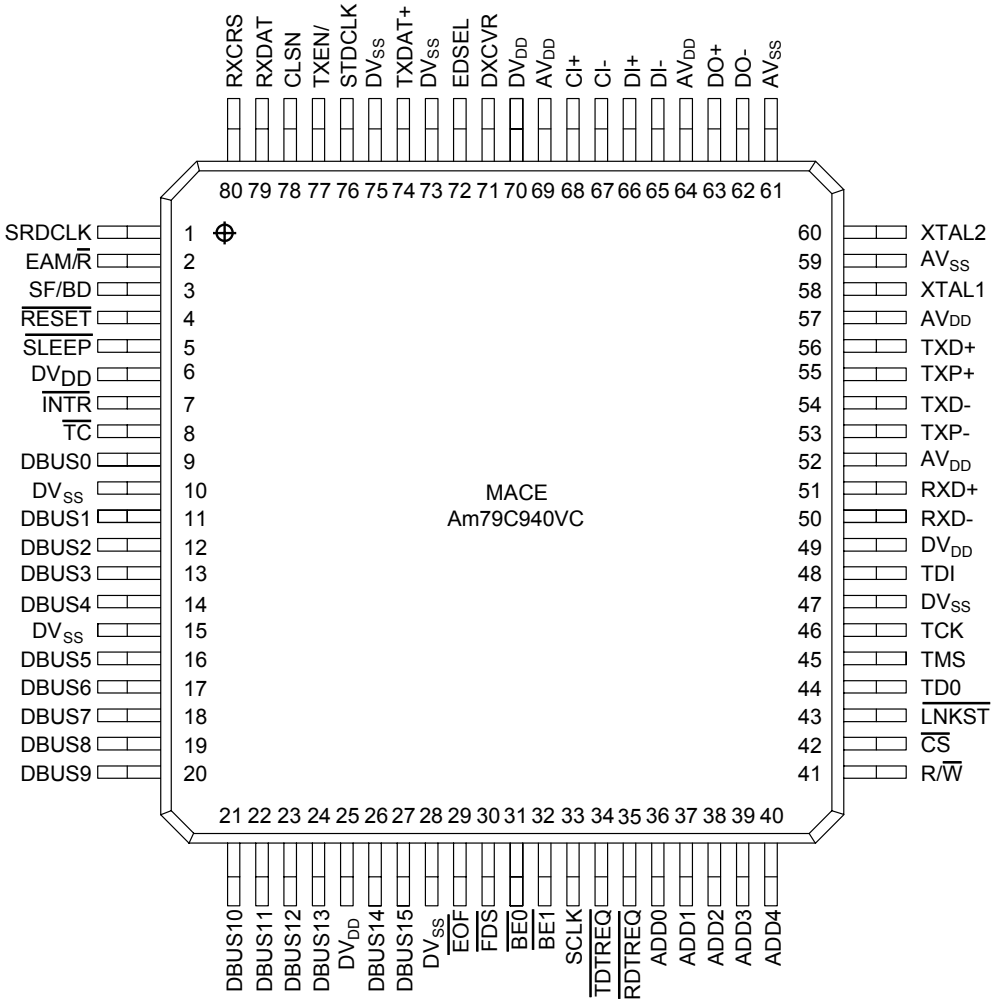
CONNECTION DIAGRAMS
PQT080
TQFP PACKAGE



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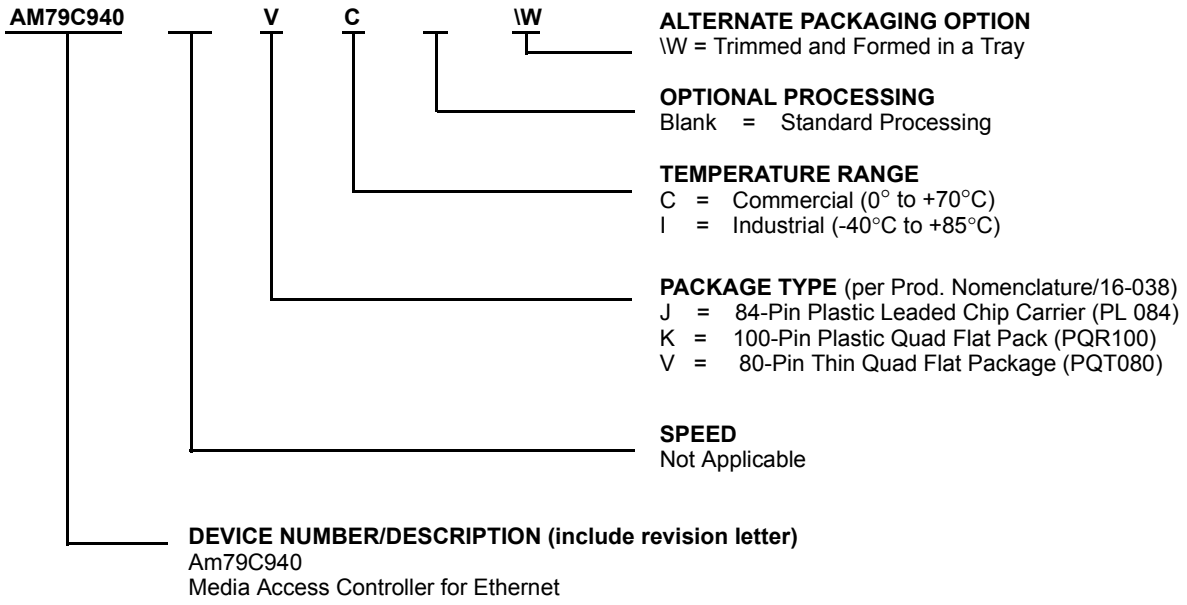
Notes: *Four pin functions available on the PLCC and PQFP packages are not available with the TQFP package. (See full data sheet for description of pins not included with the 80-pin TQFP package. In particular, see section "Pin Functions not available with the 80-pin TQFP package.")*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM79C940	JC, KC, KC\W, VC, VC\W
AM79C940	JI, KI, KI\W, VI, VI\W

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note:

Currently the silicon revision level of the MACE Ethernet controller is revision C0. This is designated by the marking on the package as Am79C940Bxx, where "xx" indicate package type and temperature range.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature . . . . . Under Bias . . . . . 0°C to +70°C

Supply Voltage to AVSS or DVss (AVDD, DVDD) . . . . . -0.3 V to +6.0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . .0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . .–40°C to +85°C

V_{CC} Supply Voltages

. . . . . (AVDD, DVDD) 5 V ±5%

All inputs within the range: . . AVDD – 0.5 V ≤ Vin ≤ . . . . . AVSS + 0.5 V, or . . . . . DV_{DD} – 0.5 V ≤ Vin ≤ . . . . . .DV_{SS} + 0.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS (Unless otherwise noted, parametric values are the same between Commercial devices and Industrial devices.)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{ILX}	XTAL1 Input LOW Voltage (External Clock Signal)	V_{SS} = 0.0 V	–0.5	0.8	V
V_{IHX}	XTAL1 Input HIGH Voltage (External Clock Signal)	V_{SS} = 0.0 V	V_{DD}– 0.8	V_{DD}+ 0.5	V
V_{OL}	Output LOW Voltage	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = -0.4 mA (Note 1)	2.4		V
I_{IL1}	Input Leakage Current	V_{DD} = 5 V, V_{IN} = 0 V (Note 2)	–10	10	µA
I_{IL2}	Input Leakage Current	V_{DD} = 5 V, V_{IN} = 0 V (Note 2)	–200	200	µA
I_{IH}	Input Leakage Current	V_{DD} = 5 V, V_{IN} = 2.7 V (Note 3)		–100	µA
I_{IAXD}	Input Current at DI+ and DI–	–1 V < V_{IN} < AV_{DD} + 0.5 V	–500	+500	µA
I_{IAXC}	Input Current at CI+ and CI–	–1 V < V_{IN} < AV_{DD} + 0.5 V	–500	+500	µA
I_{ILXN}	XTAL1 Input LOW Current during normal operation	V_{IN} = 0 V $\overline{SLEEP}$ = HIGH		–92 **(Note 9)**	µA
I_{IHXN}	XTAL1 Input HIGH Current during normal operation	V_{IN} = 5.5 V $\overline{SLEEP}$ = HIGH		92 **(Note 10)**	µA
I_{ILXS}	XTAL1 Input LOW Current during Sleep	V_{IN} = 0 V $\overline{SLEEP}$ = LOW		<10	µA
I_{IHXS}	XTAL1 Input HIGH Current during Sleep	V_{IN} = 5.5 V $\overline{SLEEP}$ = LOW		410	µA
I_{OZ}	Output Leakage Current	0.4 V < V_{OUT} < V_{DD} (Note 4)	–10	10	µA
V_{AOD}	Differential Output Voltage |(DO+)–(DO–)|	R_L = 78 Ω	630	1200	mV
V_{AODOFF}	Transmit Differential Output Idle Voltage	R_L = 78 Ω (Note 5)	–40	+40	mV

DC CHARACTERISTICS (Continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{AODOFF}	Transmit Differential Output Idle Current	R_L = 78 Ω	–1	+1	mA
V_{AOCM}	DO± Common Mode Output Voltage	R_L = 78 Ω	2.5	AVDD	V
$V_{OD}I$	DO± Differential Output Voltage Imbalance	R_L = 78 Ω (Note 6)	–25	25	mV
V_{ATH}	Receive Data Differential Input Threshold	R_L = 78 Ω (Note 6)	–35	35	mV
V_{ASQ}	DI± and CI± Differential Input Threshold Squelch	R_L = 78 Ω (Note 6)	–160	–275	mV
V_{IRDVD}	DI± and CI± Differential Mode Input Voltage Range			1.5	V
V_{ICM}	DI± and CI± Input Bias Voltage	I_{IN}= 0 mA	AV_{DD} –3.0	AV_{DD} –0.8	V
V_{OPD}	DI± Undershoot Voltage at Zero Differential on Transmit Return to Zero (ETD)	(Note 5)		–100	mV
I_{DD}	Power Supply Current	SCLK = 25 MHz XTAL1 = 20 MHz		75	mA
$I_{DDSLEEP}$	Power Supply Current	SLEEP Asserted, AWAKE = 0 RWAKE = 1 (Note 7)		100	µA
$I_{DDSLEEP}$	Power Supply Current	SLEEP Asserted, AWAKE = 1 RWAKE = 0 (Note 7)		10	mA
$I_{DDSLEEP}$	Power Supply Current	SLEEP Asserted, AWAKE = 0 RWAKE = 1 (Note 7)		20	mA
Twisted Pair Interface					
I_{IRXD}	Input Current at RXD±	$AV_{SS} < V_{IN} < AV_{DD}$	–500	500	µA
R_{RXD}	RXD± Differential Input Resistance	(Note 8)	10		KΩ
V_{TIVB}	RXD±, RXD– Open Circuit Input Voltage (Bias)	I_{IN}= 0 mA	AV_{DD} –3.0	AV_{DD} –1.5	V
V_{TIDV}	Differential Mode Input Voltage Range (RXD±)	AV_{DD}= +5V	–3.1	+3.1	V
V_{TSQ+}	RXD Positive Squelch Threshold (Peak)	Sinusoid 5 MHz ≤ f ≤10 MHz	300	520	mV
$V_{TSQ–}$	RXD Negative Squelch Threshold (Peak)	Sinusoid 5 MHz ≤ f ≤10 MHz	–520	–300	mV
V_{THS+}	RXD Post-Squelch Positive Threshold (Peak)	Sinusoid 5 MHz ≤ f ≤10 MHz	150	293	mV
$V_{THS–}$	RXD Post-Squelch Negative Threshold) (Peak)	Sinusoid 5 MHz ≤ f ≤10 MHz	–293	–150	mV
V_{LTSQ+}	RXD Positive Squelch Threshold (Peak)	$\overline{LRT}$ = LOW	180	312	mV
$V_{LTSQ–}$	RXD Negative Squelch Threshold (Peak)	$\overline{LRT}$ = LOW	–312	–180	mV
V_{LTHS+}	RXD Post-Squelch Positive Threshold (Peak)	$\overline{LRT}$ = LOW	90	156	mV

DC CHARACTERISTICS (Continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{LTHS-}	RXD Post-Squelch Negative Threshold (Peak)	$\overline{LRT}$ = LOW	–156	–90	mV
V_{RXDTH}	RXD Switching Threshold	(Note 4)	–35	35	mV
V_{TXH}	TXD± and TXD± Output HIGH Voltage	DV_{SS} = 0V	DV_{DD} –0.6	DV_{DD}	V
V_{TXL}	TXD± and TXD± Output LOW Voltage	DV_{DD} = +5V	DV_{SS}	DV_{SS} + 0.6	V
V_{TXI}	TXD± and TXD± Differential Output Voltage Imbalance		–40	+40	mV
V_{TXOFF}	TXD± and TXD± Idle Output Voltage	DV_{DD} = +5V		40	mV
R_{TX}	TXD± Differential Driver Output Impedance	(Note 8)		40	Ω
	TXD± Differential Driver Output Impedance	(Note 8)		80	Ω

Notes:

1. *V_{OH} does not apply to open-drain output pins.*
2. *I_{IL1} and I_{IL2} applies to all input only pins except DI±, CI±, and XTAL1.*
   I_{IL1} = ADD4–0, $\overline{BE}$1–0, $\overline{CS}$, $\overline{EAM/R}$, $\overline{FDS}$, $\overline{RESET}$, RXDAT, R/$\overline{W}$, SCLK.
   I_{IL2} = $\overline{TC}$, TDI, TCK, TMS.
3. *Specified for input only pins with internal pull-ups: TC, TDI, TCK, TMS.*
4. *I_{OZ} applies to all three-state output pins and bi-directional pins.*
5. *Test not implemented to data sheet specification.*
6. *Tested, but to values in excess of limits. Test accuracy not sufficient to allow screening guard bands.*
7. *During the activation of $\overline{SLEEP}$:*
   –The following pins are placed in a high impedance state: SRD, SF/BD, TXDAT, DXCVR, $\overline{DTV}$, $\overline{TDTREQ}$, $\overline{RDTREQ}$, $\overline{NTR}$ and TDO.
   –The following I/O pins are placed in a high impedance mode and have their internal TTL level translators disabled: DBUS15–0, $\overline{EOF}$, SRDCLK, RXCRS, RXDAT, CLSN, $\overline{TXEN}$, STDCLK and TXDAT+.
   –The following input pin has its internal pull-up and TTL level translator disabled: $\overline{TC}$.
   –The following input pins have their internal TTL level translators disabled and do not have internal pull-ups: $\overline{CS}$, $\overline{FDS}$, R/$\overline{W}$, ADD4-0, SCLK, $\overline{BE0}$, $\overline{BE1}$ and $\overline{EAM/R}$.
   –The following pins are pulled low: XTAL1 (XTAL2 feedback is cut off from XTAL1), TXD+, TXD–, TXP+, TXP–, DO+ and DO.
   –The following pins have their input voltage bias disabled: DI+, DI, CI+ and CI.
   –AWAKE and RWAKE are reset to zero. $I_{DDSLEEP}$, with either AWAKE set or RWAKE set, will be much higher and its value remains to be determined.
8. *Parameter not tested.*
9. *For industrial temperature version, Max value is –150 μA.*
10. *For industrial temperature version, Max value is +150 μA.*

AC CHARACTERISTICS (Unless otherwise noted, parametric values are the same between Commercial devices and Industrial devices.)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min (ns)	Max (ns)
Clock and Reset Timing					
1	t_{SCLK}	SCLK period		40	1000
2	t_{SCLKL}	SCLK LOW pulse width		0.4*t_{SCLK}	0.6*t_{SCLK}
3	t_{SCLKH}	SCLK HIGH pulse width		0.4*t_{SCLK}	0.6*t_{SCLK}
4	t_{SCLKR}	SCLK rise time			5
5	t_{SCLKF}	SCLK fall time			5
6	t_{RST}	$\overline{\text{RESET}}$ pulse width		15*t_{SCLK}	
7	t_{BT}	Network Bit Time (BT)=2*tX1 or tSTDC		99	101
Internal MENDEC Clock Timing					
9	t_{X1}	XTAL1 period		49.995	50.005
11	t_{X1H}	XTAL1 HIGH pulse width		20	
12	t_{X1L}	XTAL1 LOW pulse width		20	
13	t_{X1R}	XTAL1 rise time			5
14	t_{X1F}	XTAL1 fall time			5
BIU TIMING (Note 1)					
31	t_{ADDS}	Address valid setup to SCLK↓		9	
32	t_{ADDH}	Address valid hold after SCLK↓		2	
1. 33	t_{SLVS}	$\overline{\text{CS}}$ or $\overline{\text{FDS}}$ and $\overline{\text{TC}}$, $\overline{\text{BE}}$1–0, R/$\overline{\text{W}}$ setup to SCLK↓		9	
34	t_{SLVH}	$\overline{\text{CS}}$ or $\overline{\text{FDS}}$ and $\overline{\text{TC}}$, $\overline{\text{BE}}$1–0, R/$\overline{\text{W}}$ hold after SCLK↓		2	
35	t_{DATD}	Data out valid delay from SCLK↓	C_L = 100 pF (Note 2)		32
36	t_{DATH}	Data out valid hold from SCLK↓		6	
37	t_{DTVD}	$\overline{\text{DTV}}$ valid delay from SCLK↓	C_L = 100 pF (Note 2)		32
38	t_{DTVH}	$\overline{\text{DTV}}$ valid hold after SCLK↓		6	
39	t_{EOFD}	$\overline{\text{EOF}}$ valid delay from SCLK↓	C_L = 100 pF (Note 2)		32
40	t_{EOFH}	$\overline{\text{EOF}}$ output valid hold after SCLK↓		6	
41	t_{CSIS}	$\overline{\text{CS}}$ inactive prior to SCLK↓		9	
42	t_{EOFS}	$\overline{\text{EOF}}$ input valid setup to SCLK↓		9	
43	t_{EOFH}	$\overline{\text{EOF}}$ input valid hold after SCLK↓		2	
44	t_{RDTD}	$\overline{\text{RDTREQ}}$ valid delay from SCLK↓	C_L = 100 pF (Note 2)		32
45	t_{RDTH}	$\overline{\text{RDTREQ}}$ input valid hold after SCLK↓		6	
46	t_{TDTD}	$\overline{\text{TDTREQ}}$ valid delay from SCLK↓	C_L = 100 pF (Note 2)		32
47	t_{TDTH}	$\overline{\text{TDTREQ}}$ input valid hold after SCLK↓		6	
48	t_{DATS}	Data in valid setup to SCLK↓		9	
49	t_{DATIH}	Data in valid setup after SCLK↓		2	
50	t_{DATE}	Data output enable delay from SCLK↓ (Note 3)		0	
51	t_{DATD}	Data output disable delay from SCLK↓ (Note 3, 4)			25

Notes:

1. *The following BIU timing assumes that EDSEL = 1. Therefore, these parameters are specified with respect to the falling edge of SCLK (SCLK↓). If EDSEL = 0, the same parameters apply but should be referenced to the rising edge of SCLK ↑).*
2. *Tested with C_L set at 100 pF and derated to support the Indicated distributed capacitive Load. See the BIU output valid delay vs. Load Chart.*
3. *Guaranteed by design–not tested.*
4. *t_{DATD} is defined as the time required for outputs to turn high impedence and is not referred to as output voltage lead.*

AC CHARACTERISTICS (continued)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min (ns)	Max (ns)
AUI Timing					
53	t_{DOTD}	XTAL1 (externally driven) to DO± ουτπυτ			100
54	t_{DOTR}	DO± rise time (10% to 90%)		2.5	5.0
55	t_{DOTF}	DO± fall time (10% to 90%)		2.5	5.0
56	t_{DOETM}	DO± rise and fall mismatch			1
57	t_{DOETD}	DO± End of Transmit Delimiter		200	375
58	t_{PWRDI}	DI± pulse width to reject	|input| > $\|_{VASQ}$|		15
59	t_{PWODI}	DI± pulse width to turn on internal DI carrier sense	|input| > $\|_{VASQ}$|	45	
60	t_{PWMDI}	DI± pulse width to maintain internal DI carrier sense on	|input| > $\|_{VASQ}$|	45	136
61	t_{PWKDI}	DI± pulse width to turn internal DI carrier sense off	|input| > $\|_{VASQ}$|	200	
62	t_{PWRCI}	CI± pulse width to reject	|input| > $\|_{VASQ}$|		10
63	t_{PWOCI}	CI± pulse width to turn on internal SQE sense	|input| > $\|_{VASQ}$|	26	
64	t_{PWMCI}	CI± pulse width to maintain internal SQE sense on	|input| > $\|_{VASQ}$|	26	90
65	t_{PWKCI}	CI± pulse width to turn internal SQE sense off	|input| > $\|_{VASQ}$|	160	
66	t_{SQED}	CI± SQE Test delay from O± inactive	|input| > $\|_{VASQ}$|		
67	t_{SQEL}	CI± SQE Test length	|input| > $\|_{VASQ}$|		
79	t_{CLSHI}	CLSN high time		t_{STDC} + 30	
80	t_{TXH}	$\overline{\text{TXEN}}$ or DO± hold time from CLSN↑	|input| > $\|_{VASQ}$|	32*t_{STDC}	96*t_{STDC}
DAI Port Timing					
70	t_{TXEND}	STDCLK↑ delay to $\overline{\text{TXEN}}$↓	C_L = 50 pF		70
72	t_{TXDD}	STDCLK↑ delay to TXDAT± change	C_L = 50 pF		70
80	t_{TXH}	$\overline{\text{TXEN}}$ or TXDAT± hold time from CLSN↑		32*t_{STDC}	96*t_{STDC}
95	t_{DOTF}	Mismatch in STDCLK ≠ to $\overline{\text{TXEN}}$↓ and $\overline{\text{TXDAT}}$± change			15
96	t_{TXDTR}	$\overline{\text{TXDAT}}$± rise time	See Note 1		5
97	t_{TXDTF}	$\overline{\text{TXDAT}}$± fall time	See Note 1		5
98	t_{TXDTM}	$\overline{\text{TXDAT}}$± rise and fall mismatch	See Note 1		1
99	$t_{TXENETD}$	$\overline{\text{TXEN}}$ End of Transmit Delimiter		250	350
100	t_{FRXDD}	First RXDAT↓ delay to RXCRS↑			100
101	t_{LRXDD}	Last RXDAT ≠ delay to RXCRS↓			120
102	$t_{CRSCLSD}$	RXCRS↑ delay to CLSN↑ ($\overline{\text{TXEN}}$ = 0)			100

AC CHARACTERISTICS (continued)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min (ns)	Max (ns)
GPSI Clock Timing					
17	t_{STDC}	STDCLK period		99	101
18	t_{STDCL}	STDCLK low pulse width	See Note 1	45	
19	t_{STDCH}	STDCLK high pulse width		45	
20	t_{STDCR}	STDCLK rise time	See Note 1		5
21	t_{STDCF}	STDCLK fall time	See Note 1		5
22	t_{SRDC}	SRDCLK period		85	115
23	t_{SRDCH}	SRDCLK HIGH pulse width		38	
24	t_{SRDCL}	SRDCLK LOW pulse width		38	
25	t_{SRDCR}	SRDCLK rise time	See Note 1		5
26	t_{SRDCF}	SRDCLK fall time	See Note 1		5
GPSI Timing					
70	t_{TXEND}	STDCLK↑ delay to $\overline{\text{TXEN}}$↑	(C_L = 50 pF)		70
71	t_{TXENH}	$\overline{\text{TXEN}}$ hold time from STDCLK↑	(C_L = 50 pF)	5	
72	t_{TXDD}	STDCLK↑ delay to TXDAT+ change	(C_L = 50 pF)		70
73	t_{TXDH}	TXDAT+ hold time from STDCLK↑	(C_L = 50 pF)	5	
74	t_{RXDR}	RXDAT rise time	See Note 1		8
75	t_{RXDF}	RXDAT fall time	See Note 1		8
76	t_{RXDH}	RXDAT hold time (SRDCLK↑ to RXDAT change)		25	
77	t_{RXDS}	RXDAT setup time (RXDAT stable to SRDCLK↑)		0	
78	t_{CRSL}	RXCRS low time		t_{STDC} + 20	
79	t_{CLSHI}	CLSN high time		t_{STDC} + 30	
80	t_{TXH}	$\overline{\text{TXEN}}$ or TXDAT± hold time from CLSN↑		$32*t_{STDC}$	$96*t_{STDC}$
81	t_{CRSH}	RXCRS hold time from SRDCLK↑		0	
EADI Feature Timing					
85	t_{DSFBDR}	SRDCLK↓ delay to SF/BD↑			20
86	t_{DSFBDF}	SRDCLK↓ delay to SF/BD↑			20
87	t_{EAMRIS}	$\overline{\text{EAM/R}}$ invalid setup prior to SRDCLK↓ after SFD		–150	
88	t_{EAMS}	$\overline{\text{EAM}}$ setup to SRDCLK↓ at bit 6 of Source Address byte 1 (match packet)		0	
89	t_{EAMRL}	$\overline{\text{EAM/R}}$ low time		200	
90	$t_{SFBDHIH}$	SF/BD high hold from last SRDCLK↓		100	
91	t_{EARS}	EAR setup SRDCLK↓ at bit 6 of message byte 64 (reject normal packet)		0	

Note:

1. Not tested but data available upon request.

AC CHARACTERISTICS (continued)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max
IEEE 1149.1 Timing					
109	t_{TCLK}	TCK Period, 50% duty cycle (+5%)		100	
110	t_{su1}	TMS setup to TCK↑		8	
111	t_{su2}	TDI setup to TCK↑		5	
112	t_{hd1}	TMS hold time from TCK↑		5	
113	t_{hd2}	TDI hold time from TCK↑		10	
114	t_{d1}	TCK↓ delay to TDO			30
115	t_{d2}	TCK↓ delay to SYSTEM OUTPUT			35
10BASE–T Transmit Timing				**Min**	**Max**
125	t_{TETD}	Transmit Start of Idle		250	350
126	t_{TR}	Transmitter Rise Time	(10% to 90%)		5.5
127	t_{TF}	Transmitter Fall Time	(90% to 10%)		5.5
128	t_{TM}	Transmitter Rise and Fall Time Mismatch			1
129	t_{XMTON}	XMT# Asserted Delay			100
130	t_{XMTOFF}	XMT# De-asserted Delay		TBD	TBD
131	t_{PERLP}	Idle Signal Period		8	24
132	t_{PWLP}	Idle Link Pulse Width	(Note 1)	75	120
133	t_{PWPLP}	Predistortion Idle Link Pulse Width	(Note 1)	45	55
134	t_{JA}	Transmit Jabber Activation Time		20	150
135	t_{JR}	Transmit Jabber Reset Time		250	750
136	t_{JREC}	Transmit Jabber Recovery Time (Minimum Time Gap Between Transmitted Packets to Prevent Jabber Activation)		1.0	
10BASE–T Receive Timing					
140	t_{PWNRD}	RXD Pulse Width Not to Turn Off Internal Carrier Sense	VIN > VTHS (min)	136	–
141	t_{PWROFF}	RXD Pulse Width to Turn Off VIN> VTHS (min)		200	
142	t_{RETD}	Receive Start of Idle		200	
143	t_{RCVON}	RCV# Asserted Delay		t_{RON} – 50	t_{RON} – 100
144	t_{RCVOFF}	RCV# De-asserted Delay		TBD	TBD

Note:

1. Not tested but data available upon request.