AM82S62

Nine-Input Parity Checker/Generator

The AM82S62 is a 9-bit parity generator/parity checker with both an ODD parity output and an EVEN parity output. The device can be used to detect errors in data transmission or data retrieval systems as well as to generate this parity check bit.

The AM82S62 features one special high-speed input (P_9) to facilitate expansion. The propagation delay to the outputs through this path is considerably reduced when compared to the P_1 through P_8 paths. This short delay path allows parity checkers/generators of larger size than 9-bits to be built with a minimum of additional delay.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am82S62

Nine-Input Parity Checker/Generator

Distinctive Characteristics

- ODD/EVEN parity outputs
- Inhibit input to disable both outputs
- High-speed expansion input – P_9
- PNP inputs
- Advanced Schottky technology
- 100% reliability assurance testing in compliance wi MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am82S62 is a 9-bit parity generator/parity checker with both an ODD parity output and an EVEN parity output. The device can be used to detect errors in data transmission or data retrieval systems as well as to generate this parity check bit.

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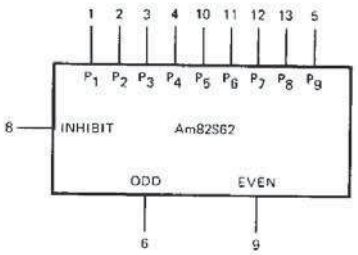
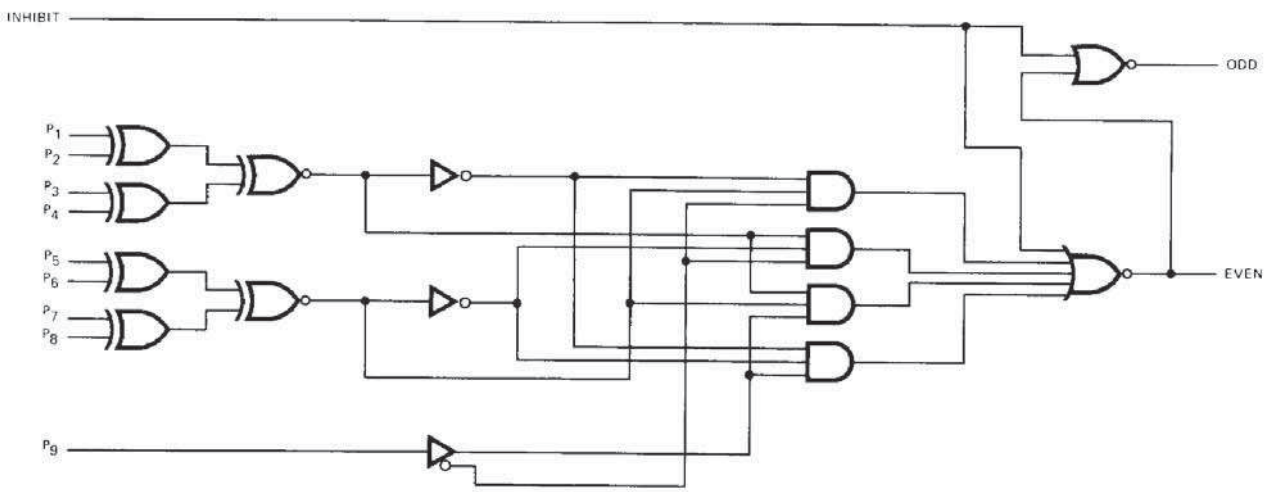
The device is built using advanced Schottky technology and incorporates PNP input transistors to reduce input loading to 0.4 STTL unit loads. The EVEN output is one gate propagation delay time shorter than the ODD output.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

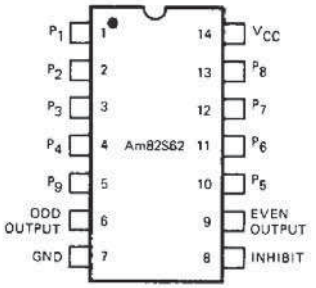
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	N82S62A
Hermetic DIP	0°C to +75°C	N82S62F
Dice	0°C to +75°C	N82S62X
Hermetic DIP	–55°C to +125°C	S82S62F
Dice	–55°C to +125°C	S82S62X

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

N82S62 T_A = 0°C to +75°C
S82S62 T_A = −55°C to +125°C
V_{CC} = 5.0V ±5% MIN. = 4.75V MAX. = 5.25V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA, V_{IN} = V_{IH} or V_{IL}	S82	2.5			Volts
			N82	2.7			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	P9			−0.4	mA
			Others			−0.8	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 4.5V				10	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				67	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. P_1 through P_9 grounded; inhibit at 4.5V; outputs open.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	P_1 through P_8 to Even Output	V_{CC} = 5.0V, R_L = 280Ω, C_L = 15 pF			23	ns
t_{PHL}						
t_{PLH}	P_1 through P_8 to Odd Output				28	ns
t_{PHL}						
t_{PLH}	P_9 to Even Output				12	ns
t_{PHL}						
t_{PLH}	P_9 to Odd Output				18	ns
t_{PHL}						
t_{PLH}	Inhibit to Even Output				9	ns
t_{PHL}						
t_{PLH}	Inhibit to Odd Output				9	ns
t_{PHL}						

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TRUTH TABLE

INHIBIT	NUMBER OF P INPUTS		OUTPUT	
	LOW	HIGH	ODD	EVEN
L	0	9	H	L
L	1	8	L	H
L	2	7	H	L
L	3	6	L	H
L	4	5	H	L
L	5	4	L	H
L	6	3	H	L
L	7	2	L	H
L	8	1	H	L
L	9	0	L	H
H	X	X	L	L

H = HIGH
L = LOW
X = Don't Care

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
P_1	1	0.4	–	–
P_2	2	0.4	–	–
P_3	3	0.4	–	–
P_4	4	0.4	–	–
P_9	5	0.2	–	–
ODD	6	–	20	10
GND	7	–	–	–
INHIBIT	8	0.4	–	–
EVEN	9	–	20	10
P_5	10	0.4	–	–
P_6	11	0.4	–	–
P_7	12	0.4	–	–
P_8	13	0.4	–	–
V_{CC}	14	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

DEFINITION OF FUNCTIONAL TERMS

P_1 through P_9 The nine inputs to the parity tree.

INHIBIT A HIGH on the inhibit input forces both the odd output and even output LOW regardless of the P inputs. When the inhibit is LOW, the odd and even outputs will always be of opposite phase.

ODD The odd parity output of the device. When an odd number of P inputs are at a HIGH level, the odd output will be HIGH.

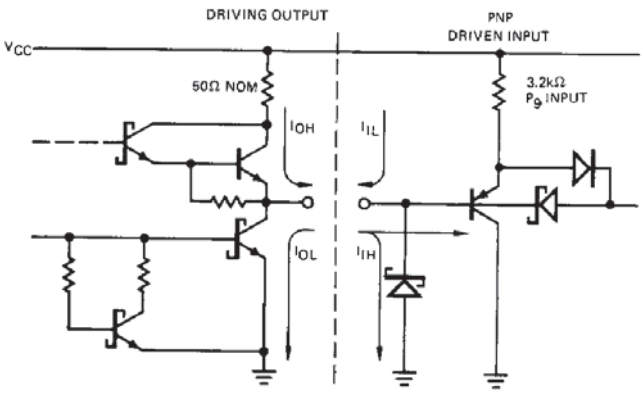
EVEN The even parity output of the device. When an even number of P inputs are at a HIGH level, the even output will be HIGH.

LOGIC EQUATIONS

ODD Output = $P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$

EVEN Output = $\overline{P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9}$

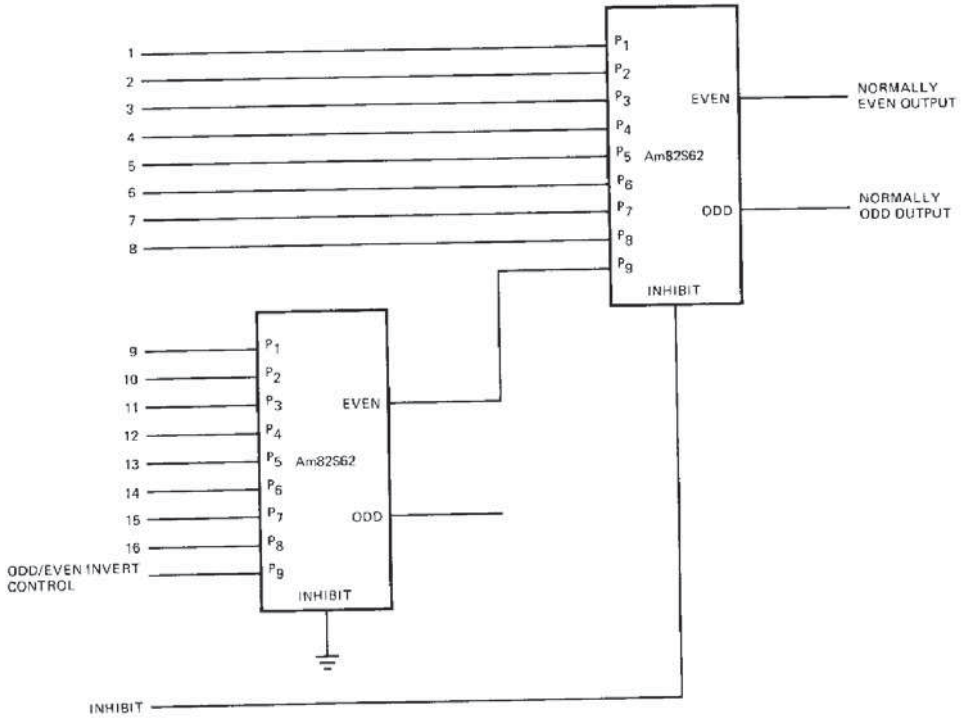
SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



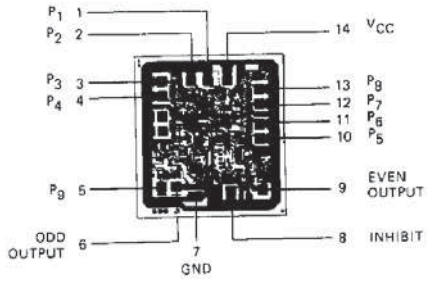
Note: Actual current flow direction shown.

APPLICATION

16-BIT PARITY GENERATOR WITH INVERT CONTROL



Metallization and Pad Layout



DIE SIZE 0.067" X 0.072"

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