CA3089

FM IF System

Intersil CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. The block diagram shows the CA3089 features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as delayed AGC for the RF tuner, and AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5V to +16V.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

CA3089

November 1996

FM IF System

Features

- **For FM IF Amplifier Applications in High-Fidelity, Automotive, and Communications Receivers**
- **Includes: IF Amplifier, Quadrature Detector, AF Preamplifier, and Specific Circuits for AGC, AFC, Muting (Squelch), and Tuning Meter**
- **Exceptional Limiting Sensitivity at -3dB Point. . . . . 12μV (Typ)**
- **Low Distortion: (with Double-Tuned Coil). . . . . 0.1% (Typ)**
- **Single-Coil Tuning Capability**
- **High Recovered Audio. . . . . 400mV (Typ)**
- **Provides Specific Signal for Control of Interchannel Muting (Squelch)**
- **Provides Specific Signal for Direct Drive of a Tuning Meter**
- **Provides Delayed AGC Voltage for RF Amplifier**
- **Provides a Specific Circuit for Flexible AFC**
- **Internal Supply-Voltage Regulators**

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA3089E	-40 to 85	16 Ld PDIP	E16.3
CA3089M1 (3089M)	-40 to 85	20 Ld SOIC	M20.3

Description

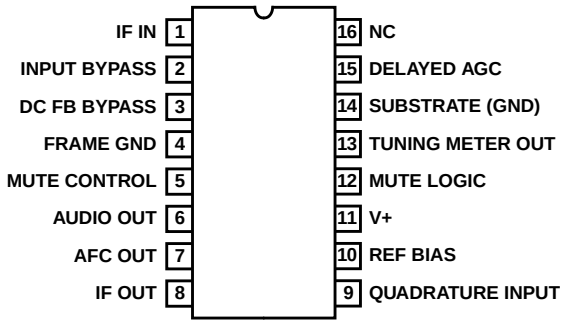
Intersil CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. The block diagram shows the CA3089 features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as delayed AGC for the RF tuner, and AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5V to +16V.

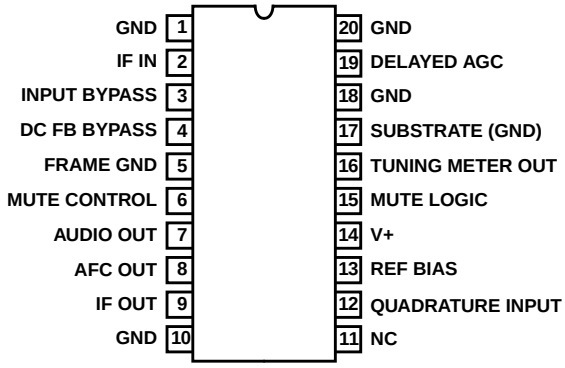
The CA3089 is ideal for high-fidelity operation. Distortion in a CA3089 FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.

Pinout

CA3089
(PDIP)
TOP VIEW



CA3089
(SOIC)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage
- Between V+ and Frame GND 16V
- Between V+ and Substrate GND 16V

DC Current (Out of Delayed AGC) 2mA

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PDIP Package	90
SOIC Package	80

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC

Maximum Storage Temperature Range . . . . . -65^oC to 150^oC

Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V+ = 12V (See Figures 3 and 4)

(NOTE 3) PARAMETER		TEST CONDITIONS		TEMP. (^oC)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS								
Quiescent Circuit Current		No signal input, Non muted		25	16	23	30	mA
DC Voltages	Terminal 1 (IF Input)			25	1.2	1.9	2.4	V
	Terminal 2 (AC Return to Input)			25	1.2	1.9	2.4	V
	Terminal 3 (DC Bias to Input)			25	1.2	1.9	2.4	V
	Terminal 6 (Audio Output)			25	5.0	5.6	6.0	V
	Terminal 10 (DC Reference)			25	5.0	5.6	6.0	V
DYNAMIC CHARACTERISTICS								
Input Limiting Voltage (-3dB point), V_1 (lim)		-	f_O = 10.7MHz, f_{MOD} = 400Hz, Deviation = ±75kHz	25	-	12	25	µV
AM Rejection (Terminal 6), AMR		V_{IN} = 0.1V, AM Mod. = 30%		25	45	55	-	dB
Recovered AF Voltage (Terminal 6) V_O (AF)		V_{IN} = 0.1V		25	300	400	500	mV
Total Harmonic Distortion, THD (Note 2)	Single Tuned (Terminal 6)			25	-	0.5	1.0	%
	Double Tuned (Terminal 6)			25	-	0.1	-	%
Signal Plus Noise to Noise Ratio (Terminal 6)				25	60	67	-	dB

NOTES:

2. THD characteristics are essentially a function of the phase characteristics of the network connected between Terminals 8, 9, and 10.
3. Terminal numbers refer to 16 Lead PDIP.

Application Information

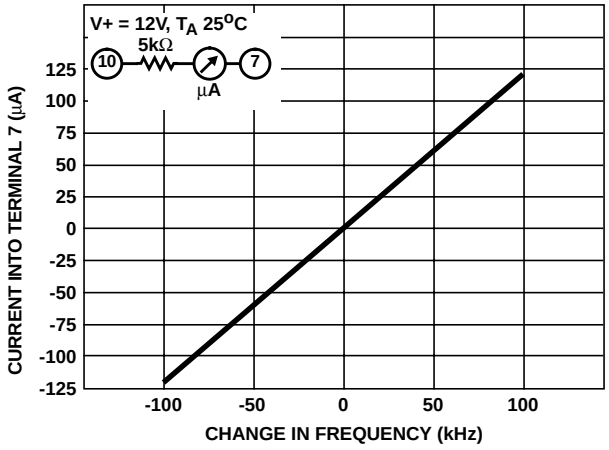


FIGURE 1. AFC CHARACTERISTICS (CURRENT AT TERMINAL 7) vs CHANGE IN FREQUENCY. (SEE TEST CIRCUIT FIGURE 3.)

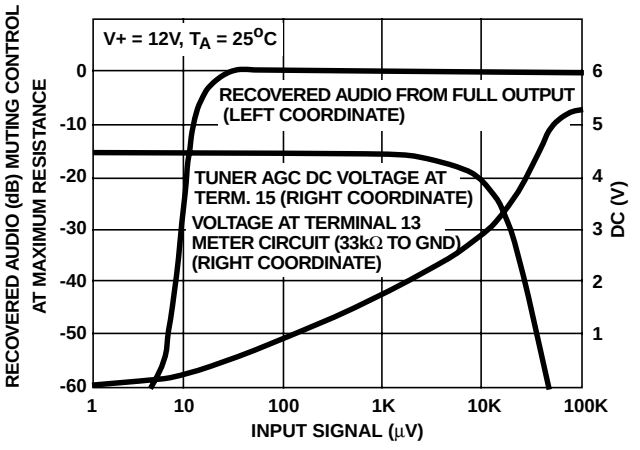
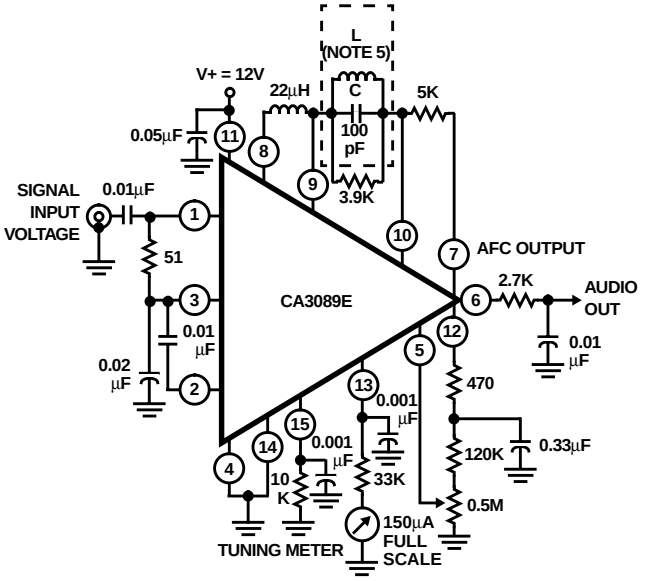


FIGURE 2. MUTING ACTION, TUNER AGC, AND TUNING METER OUTPUT vs INPUT SIGNAL VOLTAGE. (SEE TEST CIRCUIT FIGURE 3.)

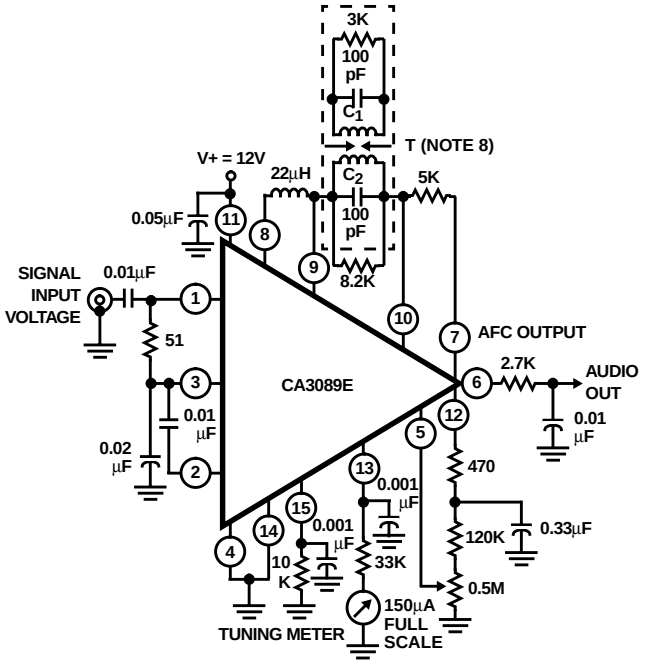
Test Circuits



NOTES:

4. All resistance values are in ohms.
5. L tunes with 100pF (C) at 10.7MHz.
6. Q_0 (unloaded) ≅ 75 (G.I. Automatic Mfg. Div. EX22741 or equivalent).

FIGURE 3. TEST CIRCUIT FOR CA3089E USING A SINGLE-TUNED DETECTOR COIL



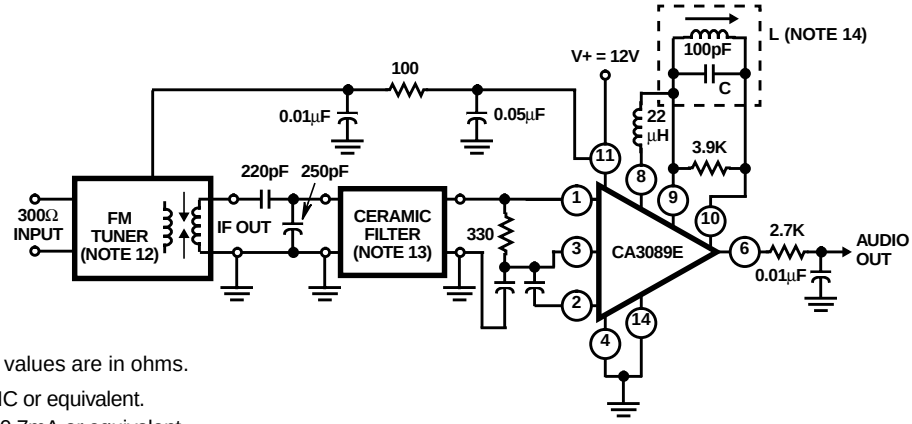
NOTES:

7. All resistance values are in ohms.
8. T PRI. - Q_0 (unloaded) ≅ 75 (tunes with 100pF (C_1) 20↑ of 34e on $^7/_{32}$" dia. form).
9. SEC. - Q_0 (unloaded) ≅ 75 (tunes with 100pF (C_2) 20↑ of 34e on $^7/_{32}$" dia. form).
10. kQ (percent of critical coupling) ≅ 70%.
    (Adjusted for coil voltage V_C) = 150mV.

Above values permit proper operation of mute (squelch) circuit "E" type slugs, spacing 4mm.

FIGURE 4. TEST CIRCUIT FOR CA3089E USING A DOUBLE-TUNED DETECTOR COIL

Typical Applications



NOTES:

11. All resistance values are in ohms.
12. Waller 4SN3FIC or equivalent.
13. Murata SFG 10.7mA or equivalent.
14. L tunes with 100pF (C) at 10.7MHz Q_0 unloaded ≅ 75 (G.I. EX22741 or equivalent).

Performance Data at f_O = 98MHz, f_{MOD} = 400Hz, Deviation = ±75kHz:

-3dB Limiting Sensitivity . . . . . 2µV (Antenna Level)
20dB Quieting Sensitivity . . . . . 1µV (Antenna Level)
30dB Quieting Sensitivity . . . . . 1.5µV (Antenna Level)

FIGURE 5. TYPICAL FM TUNER USING THE CA3089E WITH A SINGLE TUNED DETECTOR COIL

Typical Applications (Continued)

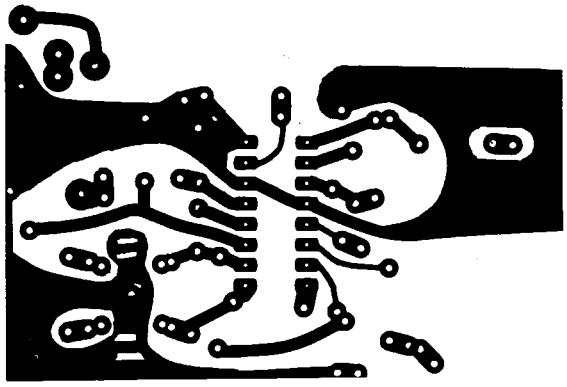


FIGURE 6A. BOTTOM VIEW OF PRINTED CIRCUIT BOARD

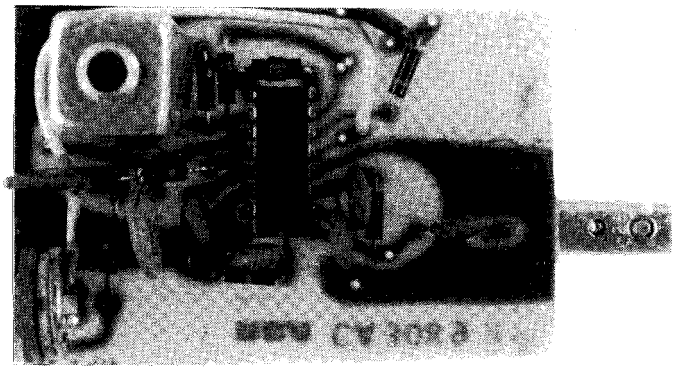
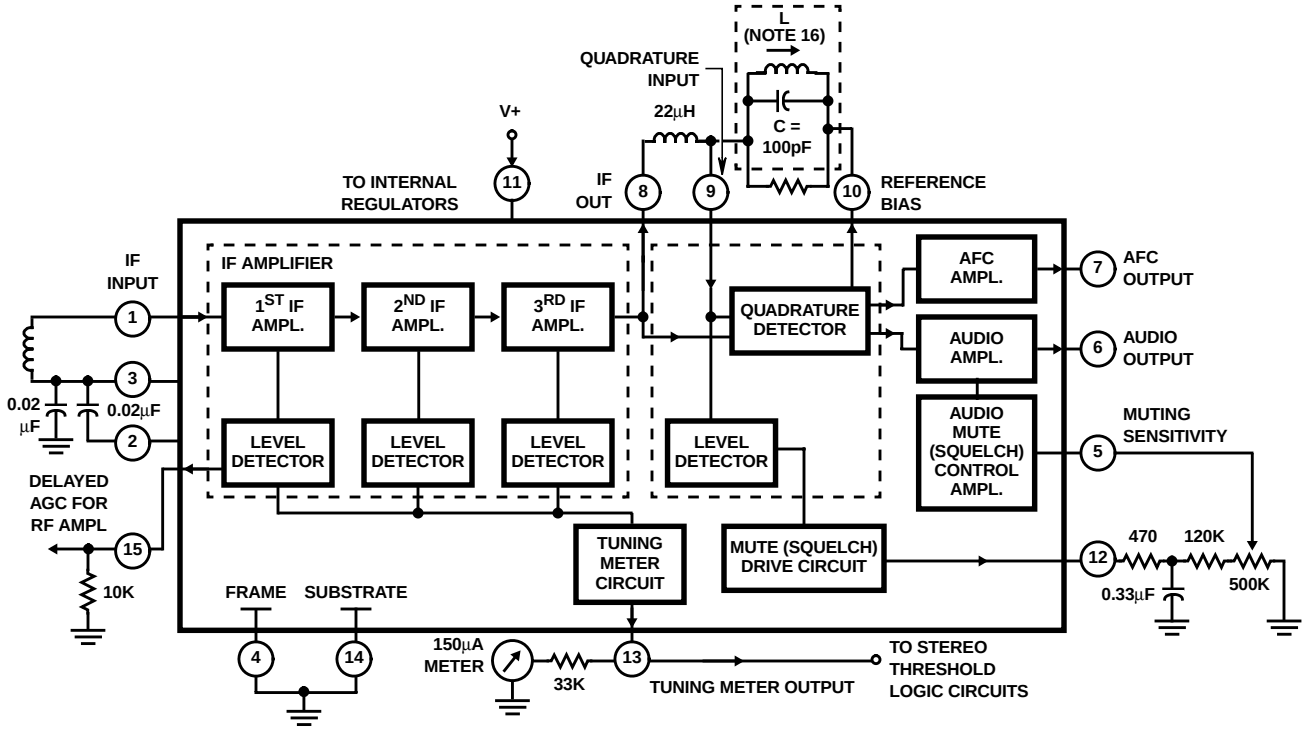


FIGURE 6B. COMPONENT SIDE - TOP VIEW

FIGURE 6. ACTUAL SIZE PHOTOGRAPHS OF THE CA3089E AND OUTBOARD COMPONENTS MOUNTED ON A PRINTED-CIRCUIT BOARD

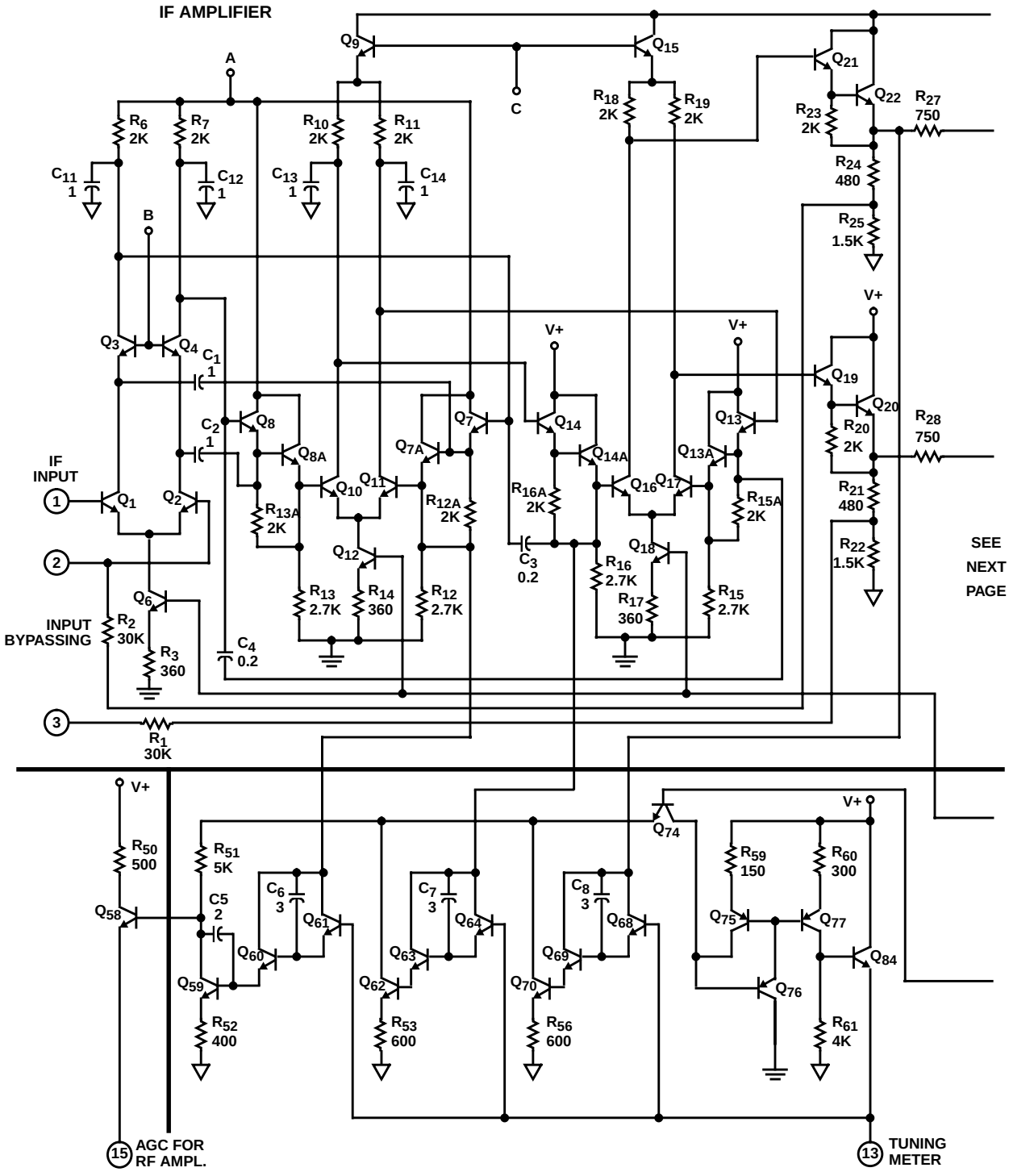
Block Diagram



NOTES:

15. All resistance values are in ohms.
16. L Tunes with 100pF (C) at 10.7MHz.
17. $Q_O \cong 75$ (G.I. EX22741 or equivalent).
18. Pin numbers refer to 16 lead DIP.

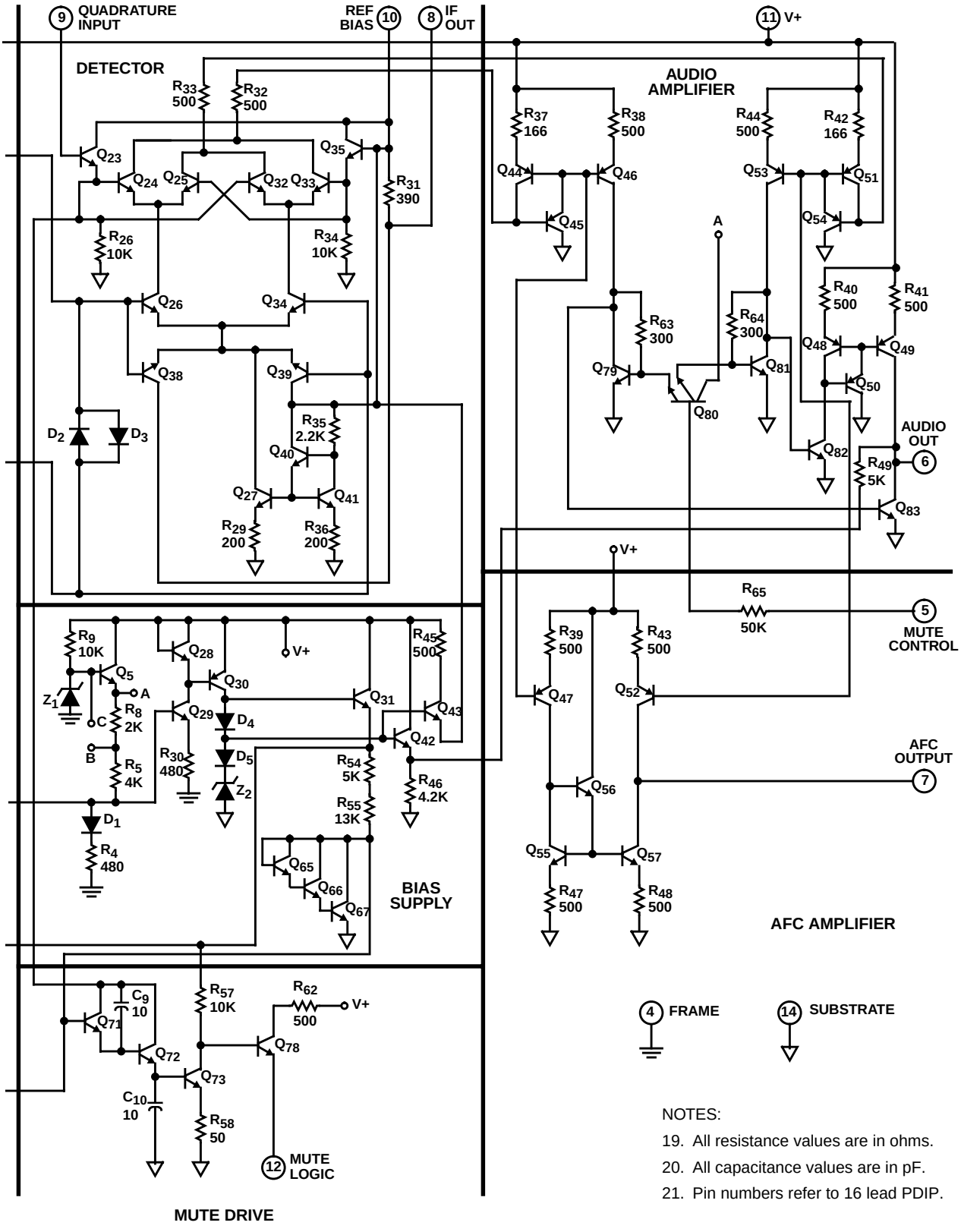
Schematic Diagram



NOTE: Pin numbers refer to 16 lead PDIP.

LEVEL DETECTOR AND METER CIRCUIT

Schematic Diagram (Continued)



NOTES:

19. All resistance values are in ohms.
20. All capacitance values are in pF.
21. Pin numbers refer to 16 lead PDIP.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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