CLC411

High Speed Video Op Amp with Disable

The CLC411 combines a state-of-the-art complementary bipolar process with National's patented current feedback architecture to provide a very high speed op amp operating from ±15V supplies. Drawing only 11mA quiescent current, the CLC411 provides a 200MHz small signal bandwidth and a 2300V/μs slew rate while delivering a continuous 70mA current output with ±4.5V output swing. The CLC411's high speed performance includes a 15ns settling time to 0.1% (2V step) and a 2.3ns rise and fall time (6V step).

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

May 2001

National Semiconductor

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General Description

The CLC411 combines a state-of-the-art complementary bipolar process with National's patented current feedback architecture to provide a very high speed op amp operating from ±15V supplies. Drawing only 11mA quiescent current, the CLC411 provides a 200MHz small signal bandwidth and a 2300V/µs slew rate while delivering a continuous 70mA current output with ±4.5V output swing. The CLC411's high speed performance includes a 15ns settling time to 0.1% (2V step) and a 2.3ns rise and fall time (6V step).

The CLC411 is designed to meet the requirements of professional broadcast video systems including composite video and high definition television. The CLC411 exceeds the HDTV standard for gain flatness to 30MHz with it's ±0.05dB flat frequency response and exceeds composite video standards with its very low differential gain and phase errors of 0.02%, 0.03˚. The CLC411 is the op amp of choice for all video systems requiring upward compatibility from NTSC and PAL to HDTV.

The CLC411 features a very fast disable/enable (10ns/55ns) allowing the multiplexing of high speed signals onto an analog bus through the common output connections of multiple CLC411's. Using the same signal source to drive disable/enable pins is easy since ″break-before-make″ is guaranteed.

Enhanced Solutions (Military/Aerospace)

SMD Number: 5962-94566

Space level versions also available.

For more information, visit http://www.national.com/mil

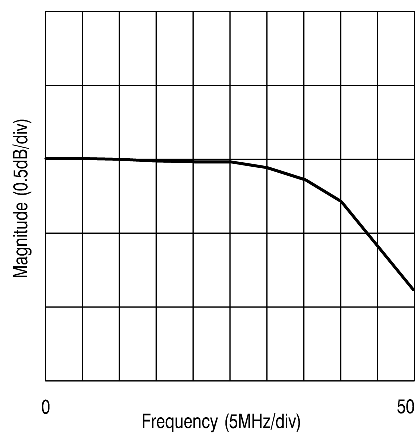
Features

- 200MHz small signal bandwidth ($1V_{PP}$)
- ±0.05dB gain flatness to 30MHz
- 0.02%, 0.03˚ differential gain, phase
- 2300V/µs slew rate
- 10ns disable to high impedance output
- 70mA continuous output current
- ±4.5V output swing into 100Ω load
- ±4.0V input voltage range

Applications

- HDTV amplifier
- Video line driver
- High speed analog bus driver
- Video signal multiplexer
- DAC output buffer

Gain Flatness (A_V=+2)



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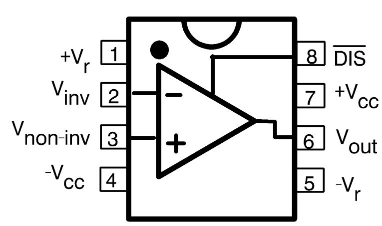
Connection Diagram



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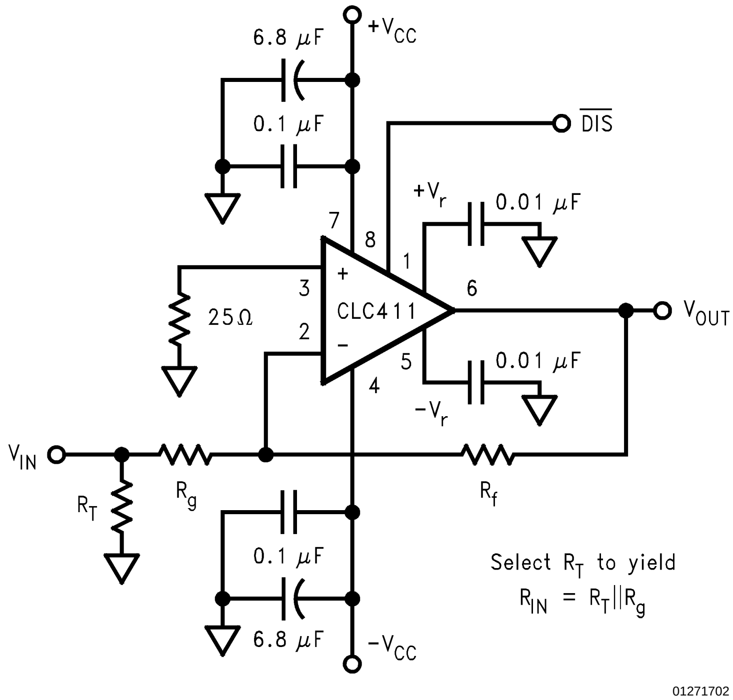
Pinout
DIP & SOIC

Typical Application



Recommended Inverting Gain Configuration

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
8-pin plastic DIP	−40˚C to +85˚C	CLC411AJP	CLC411AJP	N08E
8-pin plastic SOIC	−40˚C to +85˚C	CLC411AJE	CLC411AJE	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC}	±18V
I_{OUT}	125mA
Common-Mode Input Voltage	$\pm V_{CC}$
Differential Input Voltage	±15V
Maximum Junction temperature	+150˚C
Operating Temperature Range	−40˚C to +85˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering 10 sec)	+300˚C
ESD (Human Body Model)	1000V

Operating Ratings

Thermal Resistance

Package	(θ_{JC})	(θ_{JA})
SOIC	65˚C/W	120˚C/W
MDIP	55˚C/W	135˚C/W

Electrical Characteristics

(A_V = +2, V_{CC} = ±15V, R_L = 100Ω, R_f = 301Ω; unless specified).

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)			Units
Ambient Temperature		CLC411AJ	+25˚C	−40˚C	+25˚C	+85˚C	
Frequency Domain Response							
SSBW	-3dB Bandwidth	V_{OUT} <1V_{PP}	200	150	150	110	MHz
LSBW		V_{OUT}<6V_{PP}	75	50	50	40	MHz
	Gain Flatness	V_{OUT}< 1V_{PP}					
GFPL	Peaking	DC to 30MHz	0.05	0.2	0.2	0.3	dB
GFRL	Rolloff	DC to 30MHz	0.05	0.2	0.2	0.4	dB
GFPH	Peaking	DC to 200MHz	0.1	0.6	0.5	0.6	dB
GFRH	Rolloff	DC to 60MHz	0.2	0.7	0.4	0.7	dB
LPD	Linear Phase Deviation	DC to 60MHz	0.3	1.0	1.0	1.0	deg
DG	Differential Gain	R_L = 150Ω, 4.43MHz	0.02	–	–	–	%
DP	Differential Phase	R_L = 150Ω, 4.43MHz	0.03	–	–	–	deg
Time Domain Response							
TR	Rise and Fall Time	6V Step	2.3	–	–	–	ns
TS	Settling Time to 0.1%	2V Step	15	23	18	23	ns
OS	Overshoot	2V Step	5	15	10	15	%
SR	Slew Rate	6V Step	2300	–	–	–	V/µs
Distortion And Noise Response (Note 4)							
HD2	2nd Harmonic Distortion	2V_{PP}, 20MHz	−48	−35	−35	−35	dBc
HD3	3rd Harmonic Distortion	2V_{PP}, 20MHz	−52	−42	−42	−35	dBc
	Equivalent Input Noise						
VN	Voltage	>1MHz	2.5	–	–	–	nV/ $\sqrt{Hz}$
ICI	Inverting Current	>1MHz	12.9	–	–	–	pA/ $\sqrt{Hz}$
ICN	Non-Inverting Current	>1MHz	6.3	–	–	–	pA/ $\sqrt{Hz}$
SNF	Noise Floor	>1MHz	−157	–	–	–	dBm_{1Hz}
INV	Integrated Noise	1MHz to 200MHz	45	–	–	–	µV
Static, DC Performance							
VIO	Input Offset Voltage (Note 3)		±2	±13	±9.0	±14	mV
DVIO	Average Temperature Coefficient		±30	±50	–	±50	µV/˚C
IBN	Input Bias Current (Note 3)	Non-Inverting	12	65	30	±20	µA
DIBN	Average Temperature Coefficient		±200	±400	–	±250	nA/˚C
IBI	Input Bias Current (Note 3)	Inverting	±12	±40	±30	±30	µA
DIBI	Average Temperature Coefficient		±50	±200	–	±150	nA/˚C

Electrical Characteristics (Continued)

(A_V = +2, V_{CC} = ±15V, R_L = 100Ω, R_f = 301Ω; unless specified).

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)			Units
PSRR	Power Supply Rejection Ratio		56	48	50	48	dB
CMRR	Common-Mode Rejection Ratio		52	44	46	44	dB
ICC	Supply Current (Note 3)	No Load	11	14	12	12	mA
ICCD	Supply Current	Disabled	2.5	4.5	3.5	4.5	mA
DISABLE/ENABLE PERFORMANCE (Note 5)							
TOFF	Disabled Time	To >50dB Attenuation @10MHz	10	30	30	60	ns
TON	Enable Time		55	–	–	–	ns
	DIS Voltage	Pin 8					
VDIS	To Disable		4.5	<3.0	<3.0	<3.0	V
VEN	To Enable		5.5	>7.0	>6.5	>6.5	V
OSD	Off Isolation	At 10MHz	59	55	55	55	dB
Miscellaneous Performance							
RIN	Non-Inverting Input Resistance		1000	250	750	1000	kΩ
CIN	Non-Inverting Input Capacitance		2.0	3.0	3.0	3.0	pF
VO	Output Voltage Range	No Load	±6.0	–	±4.5	–	V
VOL	Output Voltage Range	R_L = 100Ω	±4.5	–	±4.0	–	V
CMIR	Common Mode Input Range		±4.0	–	±3.5	–	V
IO	Output Current		70	30	50	40	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

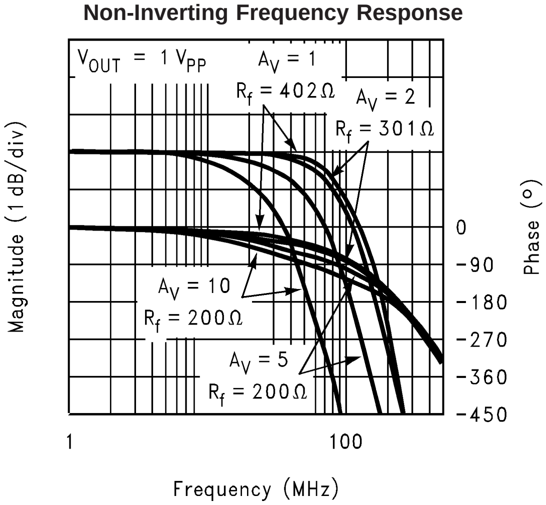
Note 3: AJ-level: spec. is 100% tested at +25˚C.

Note 4: Specifications guaranteed using 0.01mF bypass capacitors on pins 1 and 5.

Note 5: Break-before-make is guaranteed.

Typical Performance Characteristics

Non-Inverting Frequency Response



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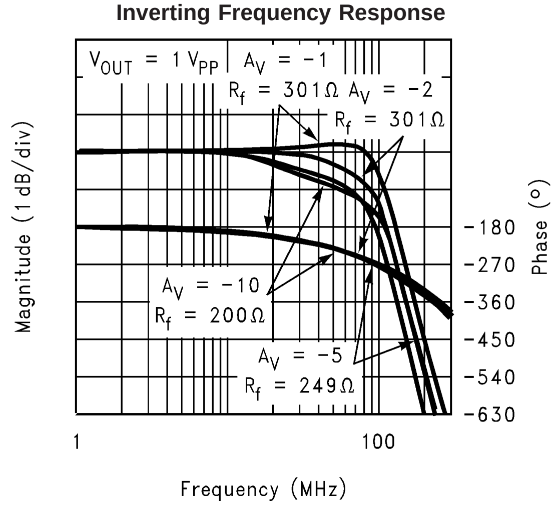
Inverting Frequency Response



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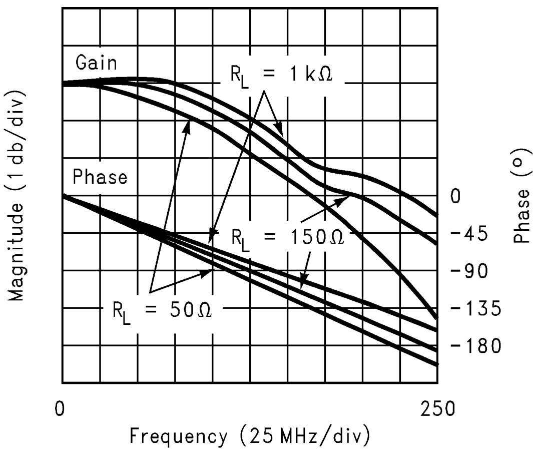
Typical Performance Characteristics (Continued)

Non-Inverting Frequency Response vs. Load



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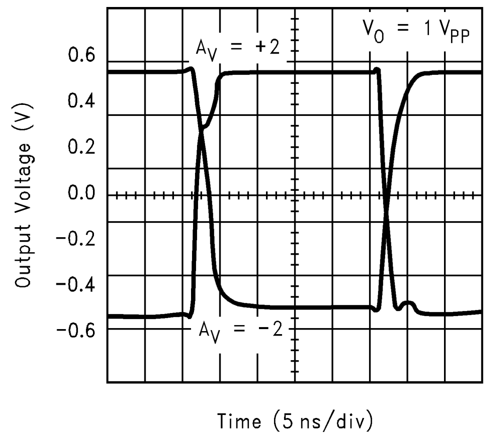
Pulse Response



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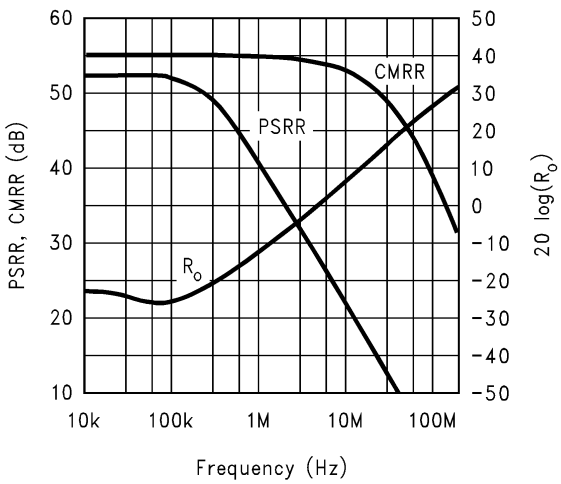
PSRR, CMRR, and Closed Loop R_O



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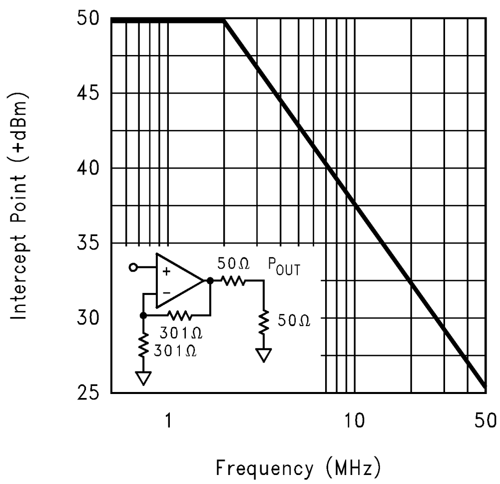
2-Tone, 3rd Order Intermodulation Intercept



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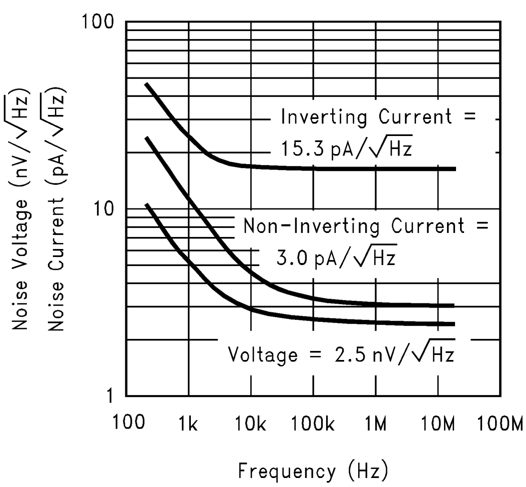
Equivalent Input Noise



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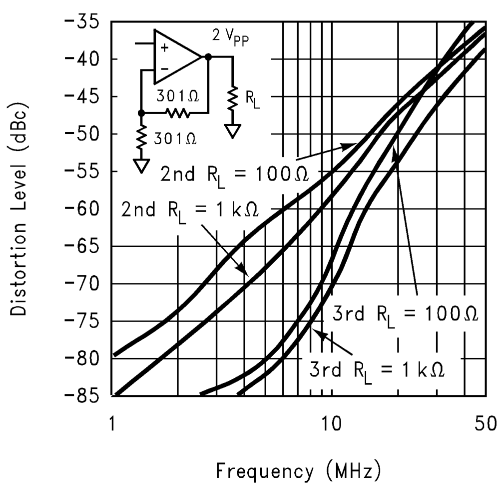
2nd and 3rd Harmonic Distortion



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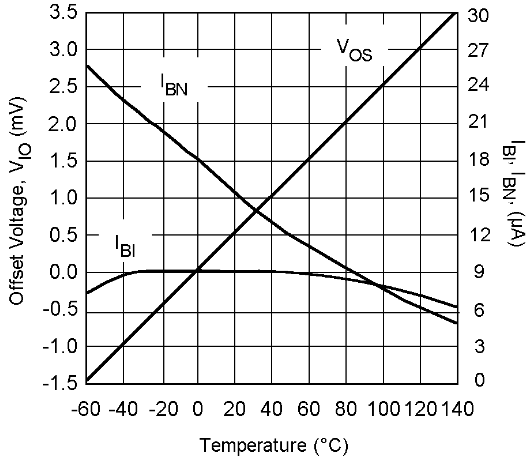
Typical Performance Characteristics (Continued)

I_{BI}, I_{BN}, V_{OS} vs. Temperature



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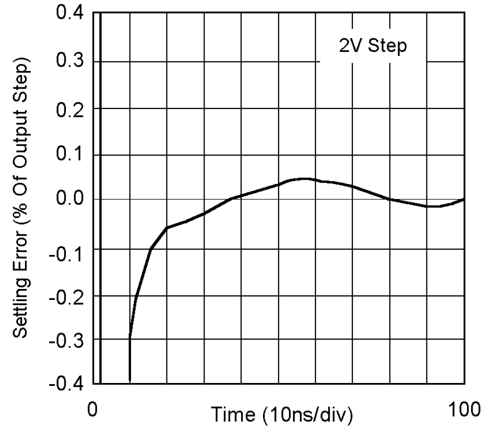
Short Term Settling Time



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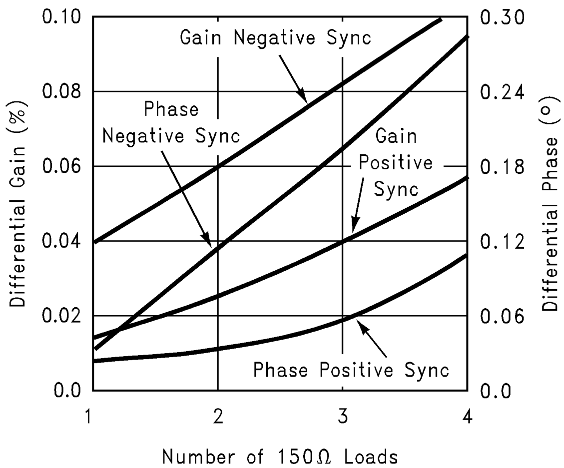
Differential Gain and Phase (4.43 MHz)



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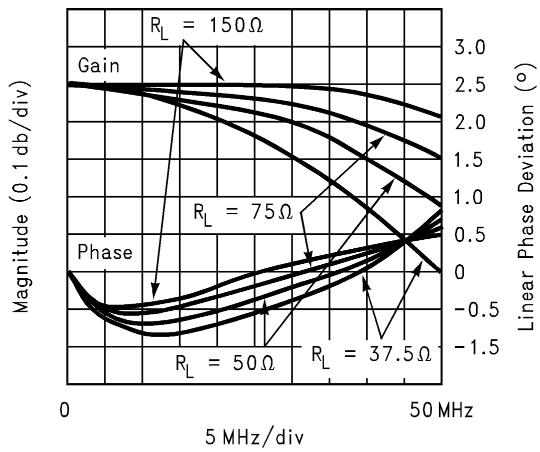
Gain Flatness and Linear Phase Deviation



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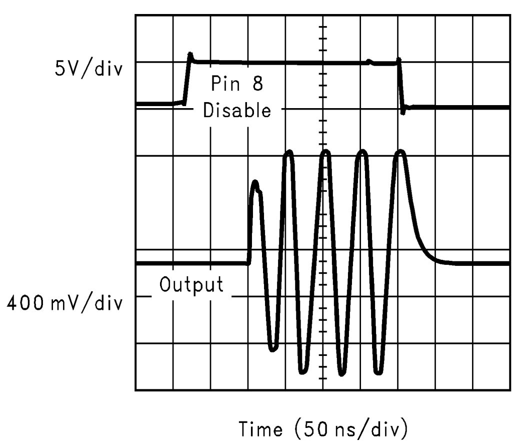
Enable/Disable Response



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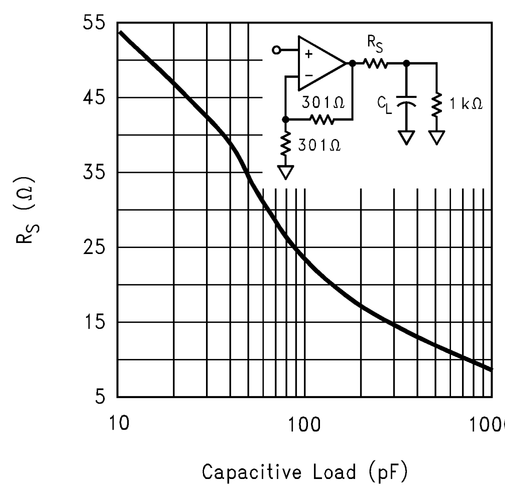
Recommended R vs. Capacitive Loads



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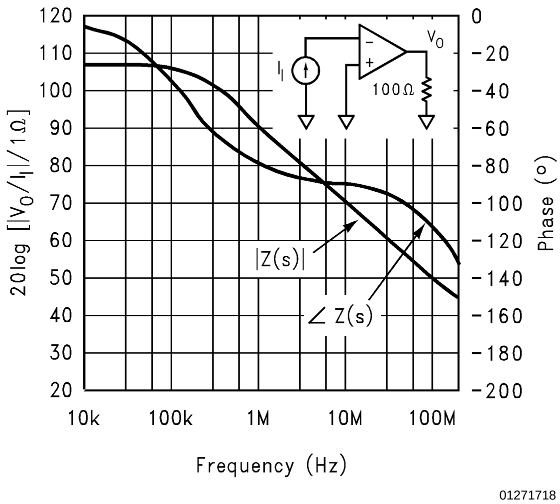
Typical Performance Characteristics (Continued)

Open-Loop Transimpedance Gain Z(s)



Application Division

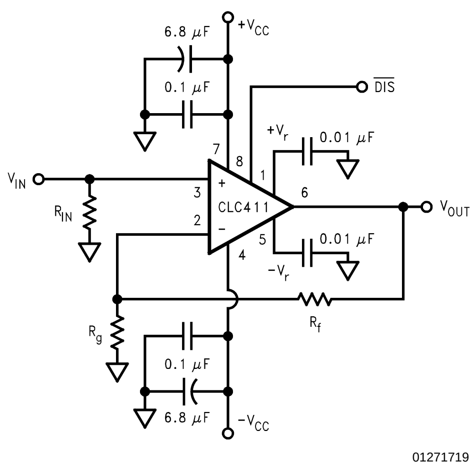


FIGURE 1. Recommended Non-Inverting Gain Circuit

Description

The CLC411 is a high speed current feedback operational amplifier which operates from ±15V power supplies. The external supplies (±V_{CC}) are regulated to lower voltages internally. The amplifier itself sees approximately ±6.5V rails. Thus the device yields performance comparable to National's ±5V devices, but with higher supply voltages. There is no degradation in rated specifications when the CLC411 is operated from ±12V. A slight reduction in bandwidth will be observed with ±10V supplies. Operation at less than ±10V is not recommended.

A block diagram of the amplifier and regulator topology is shown in *Figure 2*, ″CLC411 Equivalent Circuit.″ The regulators derive their reference voltage from an internal floating zener voltage source. External control of the zener reference pins can be used to level shift amplifier operation which is discussed in detail in the section entitled ″Extending Input/Output Range with V_r.″

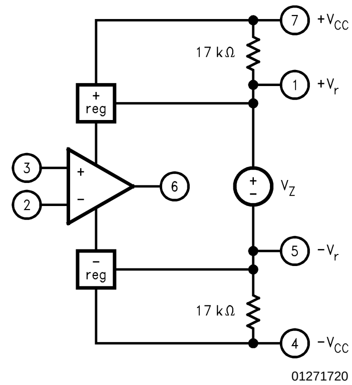


FIGURE 2. CLC411 Equivalent Circuit

Power Supply Decoupling

There are four pins associated with the power supplies. The V_{CC} pins (4,7) are the external supply voltages. The V_{CC} pins (5,1) are connected to internal reference nodes. *Figure 1*, *Figure 3* ″Recommended Non-inverting Gain Circuit″ and ″Recommended Inverting Gain Circuit″ show the recommended supply decoupling scheme with four ceramic and two electrolytic capacitors. The ceramic capacitors must be placed immediately adjacent to the device pins and connected directly to a good low inductance ground plane. Bypassing the V_r pins will reduce high frequency noise (>10MHz) in the amplifier. If this noise is not a concern these capacitors may be eliminated.

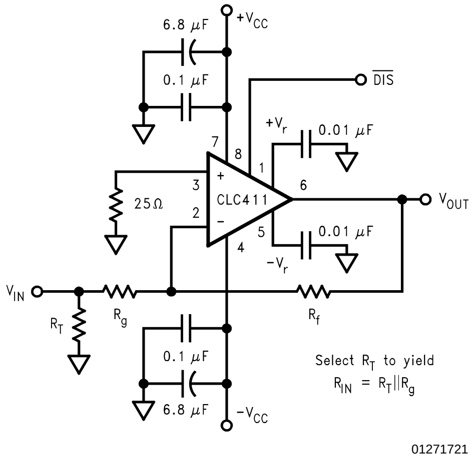


FIGURE 3. Recommended Inverting Gain Circuit

Differential Gain and Phase

The differential gain and phase errors of the CLC411 driving one doubly-terminated video load (R_L=150Ω) are specified and guaranteed in the ″Electrical Characteristics″ table. The ″Typical Performance″ plot, ″Differential Gain and Phase (4.43MHz) shows the differential gain and phase performance of the CLC411 when driving from one to four video loads. Application note OA-08, ″Differential Gain and Phase for Composite Video Systems,″ describes in detail the techniques used to measure differential gain and phase.

Feedback Resistor

The loop gain and frequency response for a current feedback operational amplifier is determined largely by the feedback resistor, R_f. The electrical characteristics and typical performance plots contained within the datasheet, unless otherwise stated, specify an R_f, of 301Ω, a gain of +2V/V and operation with a ±15V power supplies. The frequency response at different gain settings and supply voltages can be optimized by selecting a different value of R_f. Generally, lowering R_f will peak the frequency response and extend the bandwidth while increasing its value will roll off the response.

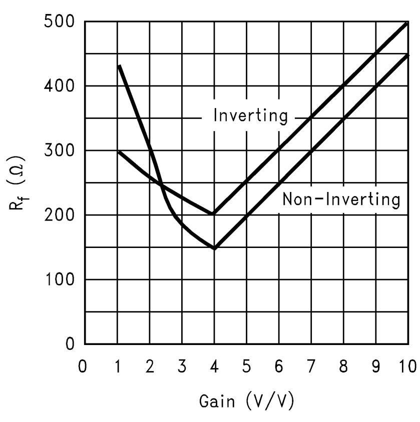


FIGURE 4. Recommended R_f vs. Gain

For unity gain voltage follower circuits, a non-zero R_f must be used with current feedback operational amplifiers such as the CLC411. Application note OA-13, ″Current-Feedback Loop-Gain Analysis and Performance Enhancements,″ explains the ramifications of R_f and how to use it to tailor the desired frequency response with respect to gain. The equations found in the application note should be considered as a starting point for the selection of R_f. The equations do not factor in the effects of parasitic capacitance found on the inverting input, the output nor across the feedback resistor. Equations in OA-13 require values for R (301Ω), Av(+2) and R_i (inverting input resistance, 50Ω). Combining these values yields a Z_t (optimum feedback transimpedance) of 400Ω. *Figure 4* entitled ″Recommended R_f vs. Gain″ will enable the selection of the feedback resistor that provides a maximally flat frequency response for the CLC411 over its gain range.

The linear portion of the two curves (i.e. A_V>4) results from the limitation on R_g (i.e. R_g≥50Ω).

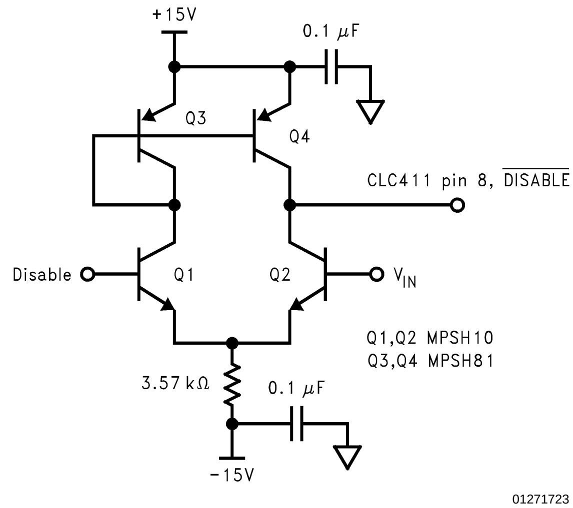


FIGURE 5. Disable Interface

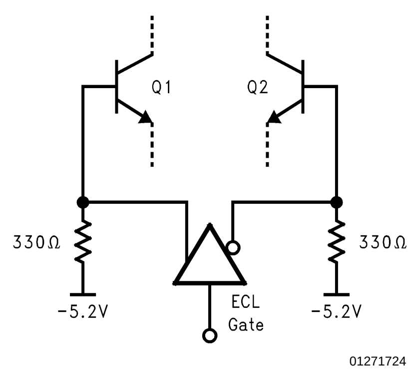


FIGURE 6. Differential ECL Interface

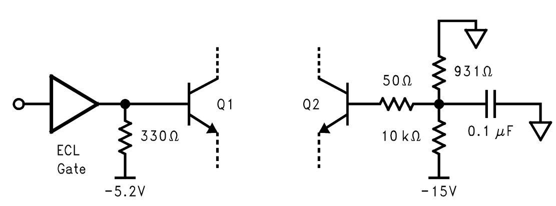


FIGURE 7. ECL Interface

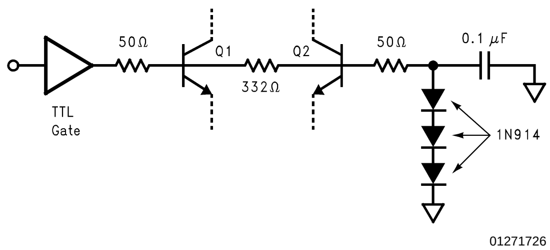


FIGURE 8. TTL Interface

Enable/Disable Operation

The disable feature allows the outputs of several CLC411 devices to be connected onto a common analog bus forming a high speed analog multiplexer. When disabled, the output and inverting inputs of the CLC411 become high impedances. The disable pin has an internal pull up resistor which is pulled up to an internal voltage, not to an external supply. Thee CLC411 is enabled when pin 8 is left open or pulled up to ≥ +7V and disabled when grounded or pulled below +3V. CMOS logic devices are necessary to drive the disable pin. For example, CMOS logic with V_{DD} ≥ +7V will guarantee proper operation over temperature. TTL voltage levels are inadequate for controlling the disable feature.

For faster enable/disable operation than 15V CMOS logic devices will allow, the circuit of *Figure 5* is recommended. A fast four transistor comparator, *Figure 5*, interfaces between the CLC411 DISABLE pin and several standard logic families. This circuit has a differential input between the bases of Q1 and Q2. As such it may be drive directly from differential ECL logic, as in shown in *Figure 6*. Single-ended logic families may also be used by establishing an appropriate threshold voltage on the V_{th} input, the base of Q2.

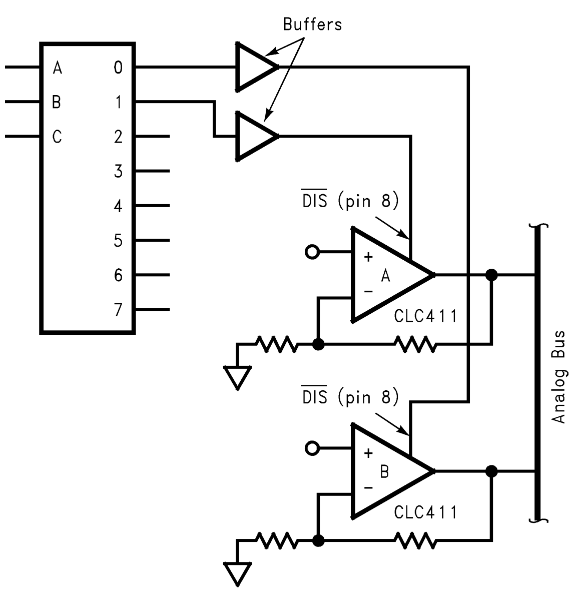


FIGURE 9. General Multiplexing Circuit

Figure 7 and *Figure 8* illustrate a single-enabled ECL and TTL interface respectively. The Disable input, the base of Q1, is driven above and below the threshold, V_{th}.

Fastest switching speeds result when the differential voltage between the bases of Q1 and Q2 is kept to less than one volt. Single-ended ECL, *Figure 7*, maintains this desired maximum differential input voltage. TTL and CMOS have higher V_{high} to V_{low} excursions. The circuit of *Figure 8* will ensure the voltage applied between the bases of Q1 and Q2 does not cause excessive switching delays in the CLC411. Under the above proscribed four transistor interface, all variations were evaluated with approximately 1ns rise and fall times which produced switching speeds equivalent to the rated disable/enable switching times found in the ″CLC411 Electrical Characteristics″ table.

A general multiplexer configuration using several CLC411s is illustrated in *Figure 9*, where a typical 8-to-1 digital mux is used to control the switching operation of the paralleled CLC411s. Since ″break-before-make″ is a guaranteed specification of the CLC411 this configuration works nicely. Notice the buffers used in driving the disable pins of the CLC411s. These buffers may be 15V CMOS logic devises mentioned previously or any variation of the four-transistor comparator illustrated above.

Extending Input/Output Range with V_r

As can be seen in *Figure 3*, the magnitude of the internal regulated supply voltages is fixed by V_z. In normal operation, with ±15V external supplies, $+V_r$ is nominally +9V when left floating. CMIR (common mode input range) and VO (output voltage range, no load) are specified under these conditions. These parameters implicitly have OV as their midpoint, i.e. the VO range is ±6V, centered at OV.

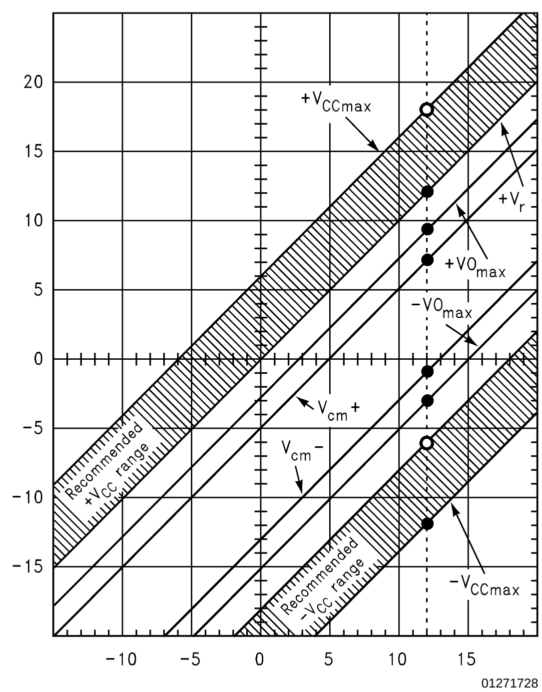


FIGURE 10. DC Parameters as a Function of $+V_r$

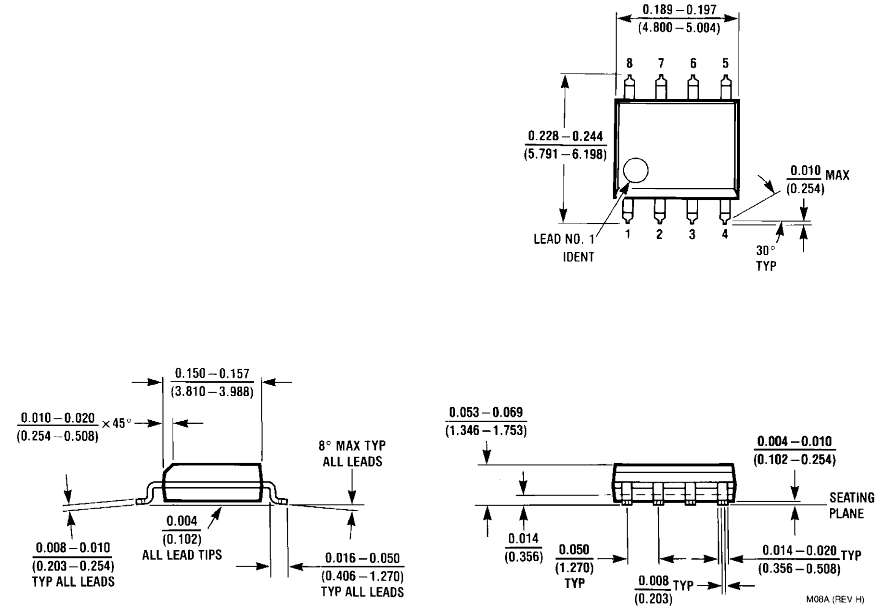
An external voltage source can be applied to $+V_r$ to shift the range of the input/output voltages. For example, if it were desired to move the positive VO range from +6V to a +9V maximum in unipolar operation, *Figure 10*, ″DC Parameters as a Function of $+V_r$″ is used to determine the required supply and $+V_r$ voltages. Referring to *Figure 10*, locate the point on the $+VO_{max}$ line where the ordinate is +9V. Draw a vertical line from this point intersecting the other lines in the graph. The circuit voltages are the ordinates of these intersections. For this example these points are shown in the graph as solid dots. The required voltage sources are $+V_r$ = +12V, $+V_{CC}$= +12V, $-V_{CC}$ = −12V. When these supply and reference voltages are applied, the range for VO is −3V to +9V, and CMIR ranges from −1V to +7V. The difference between the minimum and maximum voltages is constant, i.e. 12V for VO, only the midpoint has been shifted, i.e. from 0V to +3V for VO.

Note that in this example the $-V_r$ pin has been left open (or bypassed to reduce high-frequency noise). The difference between $+V_r$ and $-V_r$ is fixed by V_z. A level-shifting voltage can be applied to only one of the reference pins, not both. If extended operation were needed in the negative direction, *Figure 4* may be used by changing the signs, and applying the resultant negative voltage to the $-V_r$ pin. It is recommended that $+V_r$ be used for positive shifts, and $-V_r$ for negative shifts of input/output voltage range.

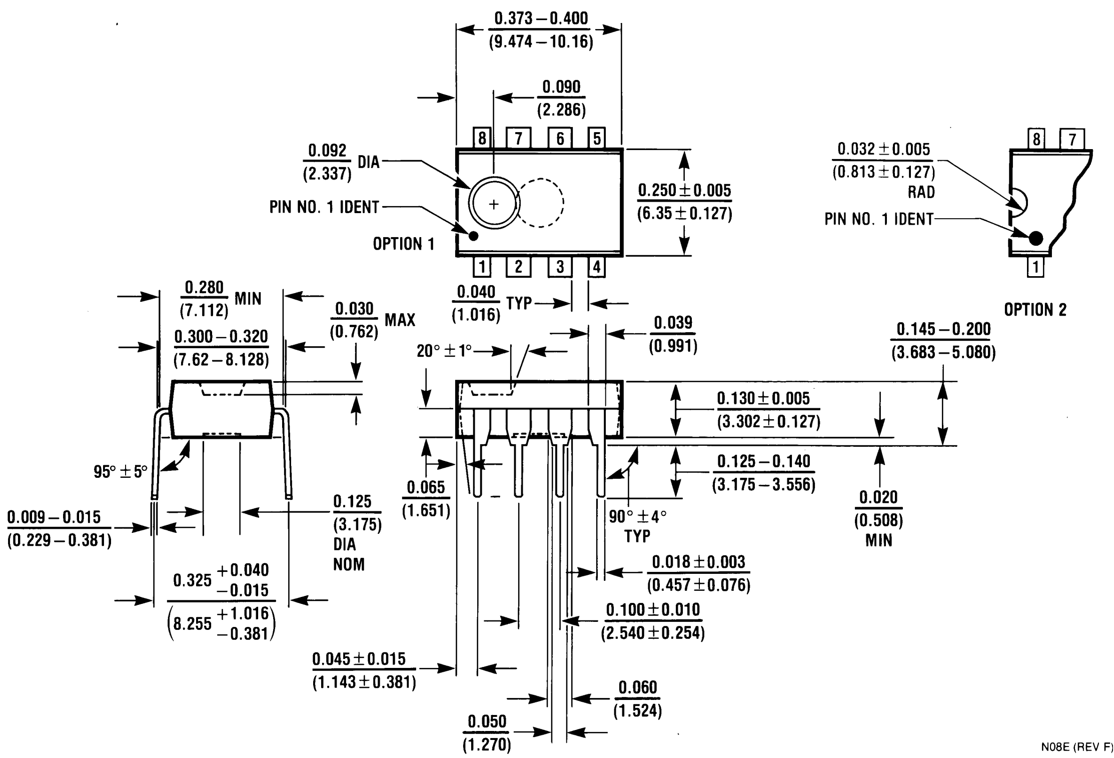
Printed Circuit Layout and Evaluation Board

Refer to application note OA-15, ″Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers,″ for board layout guidelines and construction techniques. Two very important points to consider before creating a layout which are found in the above application note are worth reiteration. First the input and output pins are sensitive to parasitic capacitances. These parasitic capacitances can cause frequency-response peaking or sustained oscillation. To minimize the adverse effect of parasitic capacitances, the ground plane should be removed from those pins to a distance of at least 0.25% Second, leads should be kept as short as possible in the finished layout. In particular, the feedback resistor should have its shortest lead on the inverting input side of the CLC411. The output is less sensitive to parasitic capacitance and therefore can drive the longer of the two feedback resistor connections. The evaluation board available for the CLC411 (part #730013 for through hold packages, 730027 for SO8) may be used as a reference for proper board layout. Application schematics for this evaluation board are in the product accessories section of the National databook.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A



8-Pin MDIP
NS Package Number N08E

Notes

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