DG200, DG201

CMOS Dual/Quad SPST Analog Switches

The DG200 and DG201 solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. They provide ease-of-use and performance advantages not previously available from solid state switches. Destructive latch-up of solid state analog gates has been eliminated by Harris' CMOS technology.

The DG200 and DG201 are completely specification and pinout compatible with the industry standard devices.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

HARRIS Semiconductor

DG200, DG201

CMOS Dual/Quad SPST Analog Switches

August 1997

Features

- Switches Greater than 28V_{P-P} Signals with ±15V Supplies
- Break-Before-Make Switching (Typ)
  - t_{OFF} 250ns
  - t_{ON} 700ns
- TTL, DTL, CMOS, PMOS Compatible
- Non-Latching with Supply Turn-Off
- Complete Monolithic Construction
- Industry Standard (DG200, DG201)

Applications

- Data Acquisition
- Sample and Hold Circuits
- Operational Amplifier Gain Switching Networks

Description

The DG200 and DG201 solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. They provide ease-of-use and performance advantages not previously available from solid state switches. Destructive latch-up of solid state analog gates has been eliminated by Harris' CMOS technology.

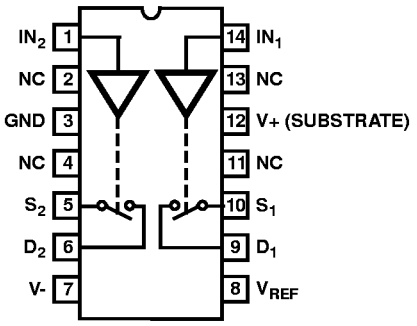
The DG200 and DG201 are completely specification and pinout compatible with the industry standard devices.

Ordering Information

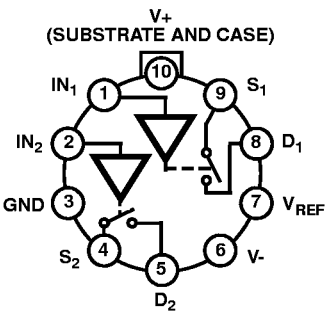
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG200AA	-55 to 125	10 Pin Metal Can	T10.B
DG200AK	-55 to 125	14 Ld CERDIP	F14.3
DG200BA	-25 to 85	10 Pin Metal Can	T10.B
DG200BK	-25 to 85	14 Ld CERDIP	F14.3
DG200CJ	0 to 70	14 Ld PDIP	E14.3
DG200AA/883B	-55 to 125	10 Pin Metal Can	T10.B
DG200AK/883B	-55 to 125	14 Ld CERDIP	F14.3
DG201AK	-55 to 125	16 Ld CERDIP	F16.3
DG201BK	-25 to 85	16 Ld CERDIP	F16.3
DG201CJ	0 to 70	16 Ld PDIP	E16.3
DG201AK/883B	-55 to 125	16 Ld CERDIP	F16.3

Pinouts

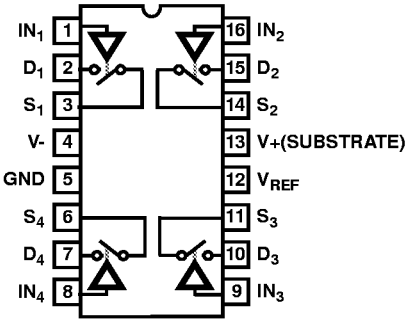
DG200 (CERDIP, PDIP)
TOP VIEW



DG200 (METAL CAN)
TOP VIEW



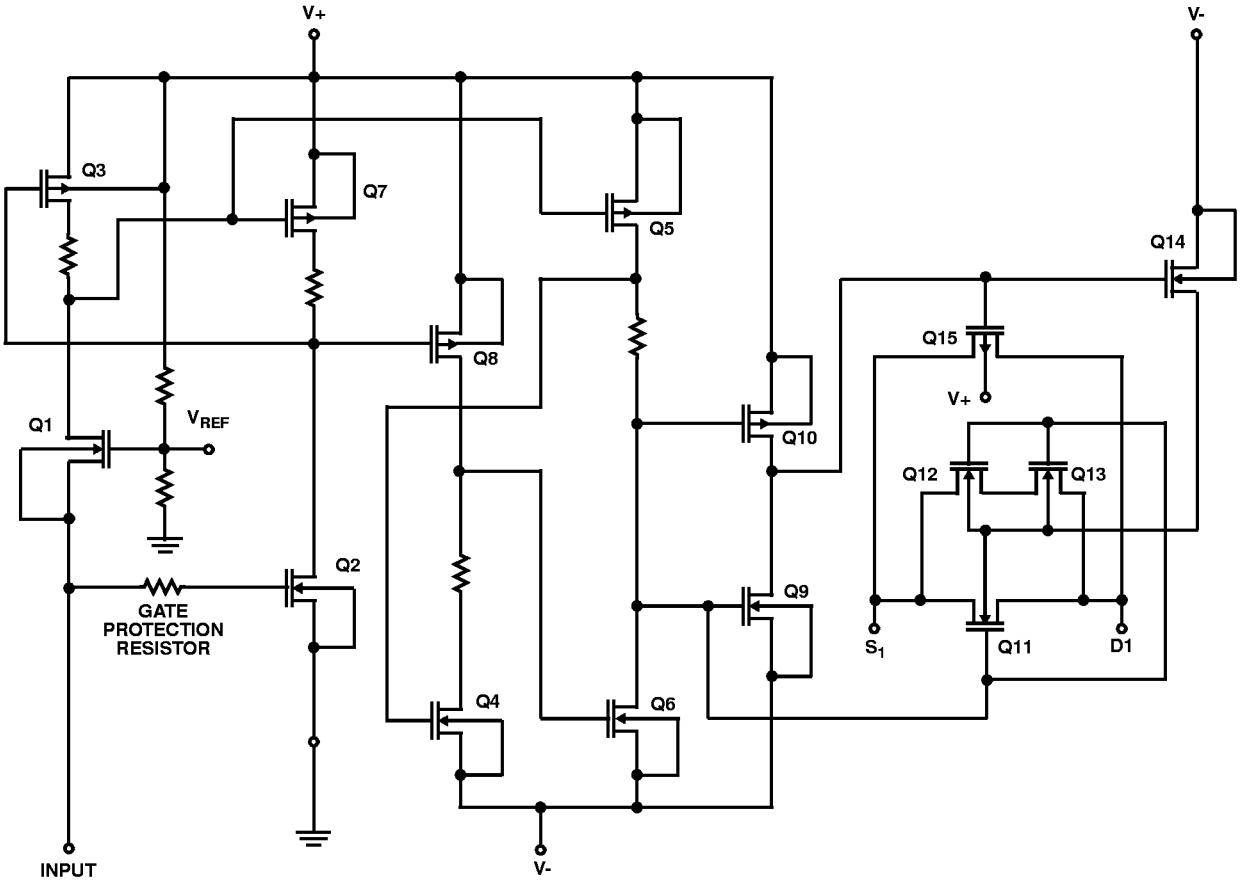
DG201 (CERDIP, PDIP)
TOP VIEW



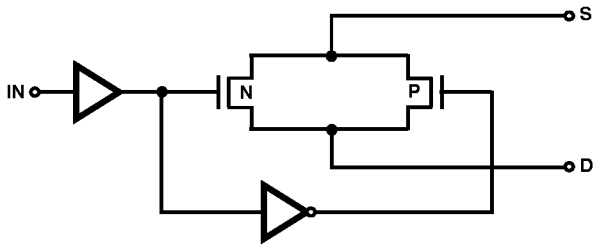
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3115.2**

Schematic Diagram ($^1/_2$ DG200, $^1/_4$ DG201)



Functional Diagram



DG200, DG201 SWITCH CELL

Absolute Maximum Ratings

V+, V- . . . . . <36V
V+ - V_D . . . . . <30V
V_D - V- . . . . . <30V
V_D - V_S . . . . . <28V
V_{IN} - GND . . . . . <20V

Operating Conditions

Temperature Range
"A" Suffix . . . . . -55°C to 125°C
"B" Suffix . . . . . -25°C to 85°C
"C" Suffix . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	75	20
PDIP Package	100	N/A
Metal Can Package	155	67

Maximum Junction Temperature
Plastic Package . . . . . 150°C
Ceramic Package . . . . . 175°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = 25°C, V+ = +15V, V- = -15V, GND = 0V

PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL/INDUSTRIAL			UNITS
		-55°C	25°C	125°C	0°C TO -25°C	25°C	70°C TO 85°C	
Input Logic Current, $I_{IN(ON)}$	V_{IN} = 0.8V (Notes 2, 3)	10	±1	±10	-	±10	±10	µA
Input Logic Current, $I_{N(OFF)}$	V_{IN} = 2.4V (Notes 2, 3)	±10	±1	±10	-	±10	±10	µA
Drain-Source On Resistance, $r_{DS(ON)}$	I_S = 10mA, V_{ANALOG} = ±10V	70	70	100	80	80	100	Ω
Channel-to-Channel $r_{DS(ON)}$ Match, $r_{DS(ON)}$		-	25 (Typ)	-	-	30 (Typ)	-	Ω
Minimum Analog Signal Handling Capability, V_{ANALOG}		-	±15V	-	-	±15V	-	V
Switch OFF Leakage Current, $I_{D(OFF)}$	V_{ANALOG} = -14V to +14V	-	±2	100	-	±5	100	nA
Switch OFF Leakage Current, $I_{S(OFF)}$	V_{ANALOG} = -14V to +14V	-	±2	100	-	±5	100	nA
Switch ON Leakage Current, $I_{D(ON)}$ + $I_{S(ON)}$	V_D = V_S = -14V to +14V	-	±2	200	-	±10	200	nA
Switch "ON" Time (Note 1), t_{ON}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V (Figure 5)	-	1.0	-	-	1.0	-	µs
Switch "OFF" Time, t_{OFF}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V (Figure 5)	-	0.5	-	-	0.5	-	µs
Charge Injection, $Q_{(INJ)}$	Figure 6	-	15 (Typ)	-	-	20 (Typ)	-	mV
Minimum Off Isolation Rejection Ratio, OIRR	f = 1MHz, R_L = 100Ω, C_L ≤ 5pF (Figure 7, Note 1)	-	54 (Typ)	-	-	50 (Typ)	-	dB
+Power Supply Quiescent Current, I_{V1}	V_{IN} = 0V to V_{IN} = 5V	1000	1000	2000	1000	1000	2000	µA
-Power Supply Quiescent Current, I_{V2}		1000	1000	2000	1000	1000	2000	µA
Minimum Channel to Channel Cross Coupling Rejection Ratio, CCRR	One Channel Off	-	54 (Typ)	-	-	50 (Typ)	-	dB

NOTES:

1. Pull Down Resistor must be ≤2kΩ.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.
3. All channels are turned off by high "1" logic inputs and all channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the minimum range for switching properly. Peak input current required for transition is typically -120µA.

Absolute Maximum Ratings

V+ to V- . . . . . <36V
V+ to V_D . . . . . <30V
V_D to V- . . . . . <30V
V_D to V_S . . . . . <28V
V_{REF} to V- . . . . . <33V
V_{REF} to V_{IN} . . . . . <30V
V_{REF} to GND . . . . . <20V
V_{IN} to GND . . . . . <20V
Current (Any Terminal) . . . . . <30mA

Operating Conditions

Temperature Range
"A" Suffix . . . . . -55°C to 125°C
"B" Suffix . . . . . -25°C to 85°C
"C" Suffix . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	75	20
PDIP Package	145	N/A

Maximum Junction Temperature
Plastic Package . . . . . 150°C
Ceramic Package . . . . . 175°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications T_A = 25°C, V+ = +15V, V- = -15V

PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL/INDUSTRIAL			UNITS
		-55°C	25°C	125°C	0°C TO -25°C	25°C	70°C TO 85°C	
Input Logic Current, $I_{IN(ON)}$	V_{IN} = 0.8V (Note 1)	±10	±1	10	±1	±1	±10	µA
Input Logic Current, $I_{N(OFF)}$	V_{IN} = 2.4V (Note 1)	±10	±1	10	±1	±1	±10	µA
Drain-Source On Resistance, $r_{DS(ON)}$	I_S = 10mA, V_{ANALOG} = ±10V	80	80	125	100	100	125	Ω
Channel-to-Channel $r_{DS(ON)}$ Match, $r_{DS(ON)}$		-	25 (Typ)	-	-	30 (Typ)	-	Ω
Minimum Analog Signal Handling Capability, V_{ANALOG}		-	±15 (Typ)	-	-	±15 (Typ)	-	V
Switch OFF Leakage Current, $I_{D(OFF)}$	V_{ANALOG} = -14V to +14V	-	±1	100	-	±5	100	nA
Switch OFF Leakage Current, $I_{S(OFF)}$	V_{ANALOG} = -14V to +14V	-	±1	100	-	±5	100	nA
Switch ON Leakage Current, $I_{D(ON)} + I_{S(ON)}$	$V_D = V_S$ = -14V to +14V	-	±2	200	-	±5	200	nA
Switch "ON" Time (Note 2), t_{ON}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V (Figure 5)	-	1.0	-	-	1.0	-	µs
Switch "OFF" Time (Note 2), t_{OFF}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V (Figure 5)	-	0.5	-	-	0.5	-	µs
Charge Injection, $Q_{(INJ)}$	Figure 6	-	15 (Typ)	-	-	20 (Typ)	-	mV
Minimum Off Isolation Rejection Ratio, OIRR	f = 1MHz, R_L = 100Ω, $C_L \leq$ 5pF, (Figure 7)	-	54 (Typ)	-	-	50 (Typ)	-	dB
+Power Supply Quiescent Current, $I+_Q$	V_{IN} = 0V to V_{IN} = 5V	2000	1000	2000	2000	1000	2000	µA
-Power Supply Quiescent Current, $I-_Q$		2000	1000	2000	2000	1000	2000	µA
Minimum Channel to Channel Cross Coupling Rejection Ratio, CCRR	One Channel Off	-	54 (Typ)	-	-	50 (Typ)	-	dB

NOTES:
1. Typical values are for design aid only, not guaranteed and not subject to production testing.
2. All channels are turned off by high "1" logic inputs and all channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the minimum range for switching properly. Peak input current required for transition is typically -120µA.

Performance Curves

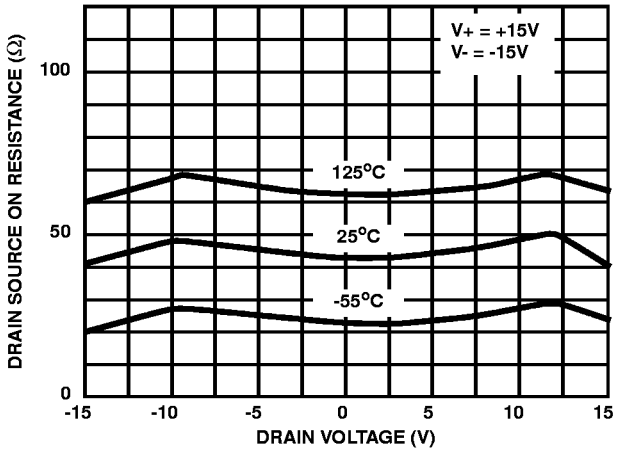


FIGURE 1. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

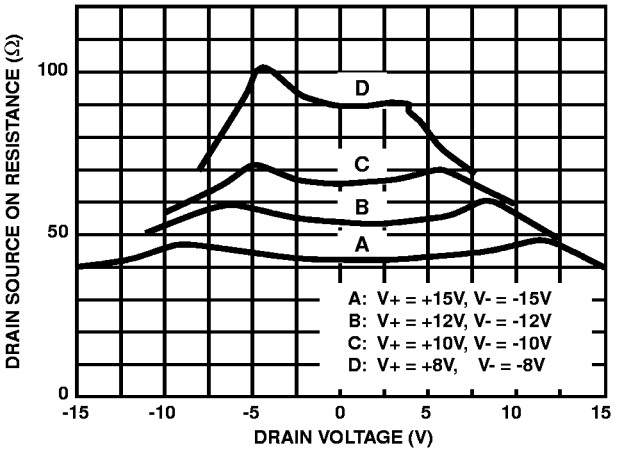


FIGURE 2. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

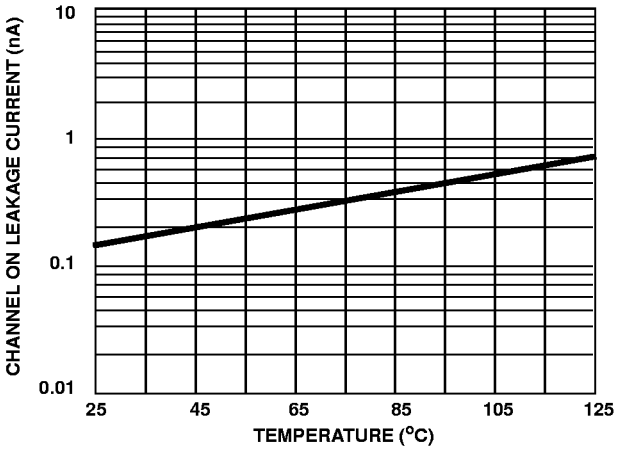


FIGURE 3. $I_{D(ON)}$ vs TEMPERATURE

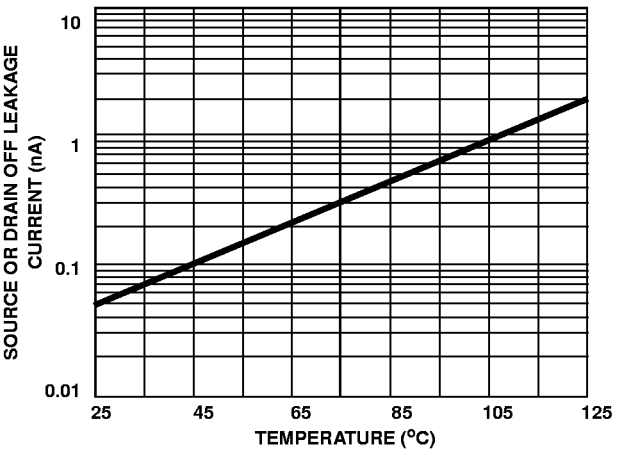


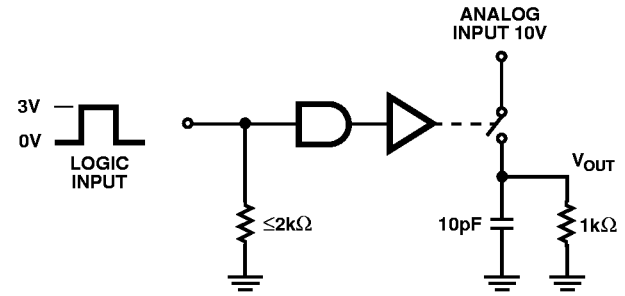
FIGURE 4. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE

Pin Descriptions

DG200 (14 LEAD DIP)		
PIN	**SYMBOL**	**DESCRIPTION**
1	IN_2	Logic Control for Switch 2
2	NC	No Connection
3	GND	Ground Terminal (Logic Common)
4	NC	No Connection
5	S_2	Source (Input) Terminal for Switch 2
6	D_2	Drain (Output) Terminal for Switch 2
7	V-	Negative Power Supply Terminal
8	V_{REF}	Logic Reference Voltage
9	D_1	Drain (Output) Terminal for Switch 1
10	S_1	Source (Input) Terminal for Switch 1
11	NC	No Connection
12	V+	Positive Power Supply Terminal (Substrate)
13	NC	No Connection
14	IN_1	Source (Input) Terminal for Switch 1

DG201 (16 LEAD DIP)		
PIN	**SYMBOL**	**DESCRIPTION**
1	IN_1	Logic Control for Switch 1
2	D_1	Drain (Output) Terminal for Switch 1
3	S_1	Source (Input) Terminal for Switch 1
4	V-	Negative Power Supply Terminal
5	GND	Ground Terminal (Logic Common)
6	S_4	Source (Input) Terminal for Switch 4
7	D_4	Drain (Output) Terminal for Switch 4
8	IN_4	Logic Control for Switch 4
9	IN_3	Logic Control for Switch 3
10	D_3	Drain (Output) Terminal for Switch 3
11	S_3	Source (Input) Terminal for Switch 3
12	V_{REF}	Logic Reference Voltage
13	V+	Positive Power Supply Terminal (Substrate)
14	S_2	Source (Input) Terminal for Switch 2
15	D_2	Drain (Output) Terminal for Switch 2
16	IN_2	Logic Control for Switch 2

Test Circuits



NOTE: All channels are turned off by high "1" logic inputs and all channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the minimum range for switching properly. Peak input current required for transition is typically -120µA.

FIGURE 5.

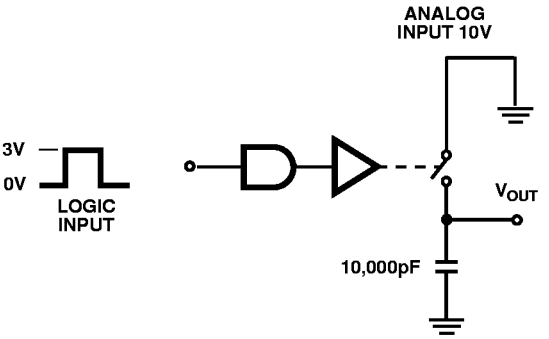
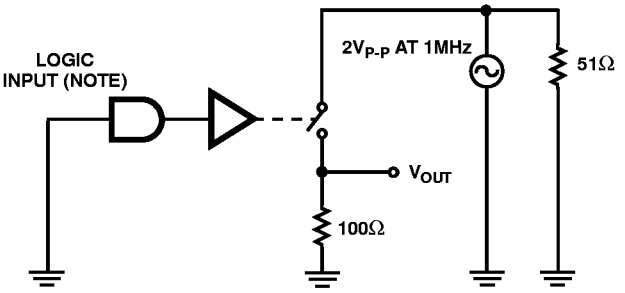


FIGURE 6.



NOTE: Pull-down resistor must be ≤2kΩ.

FIGURE 7.

Typical Applications

Using the V_{REF} Terminal

The DG200 and DG201 have an internal voltage divider setting the TTL threshold on the input control lines for V+ equal to +15V. The schematic shown in Figure 8 with nominal resistor values, gives approximately 2.4V on the V_{REF} pin. As the TTL input signal goes from +0.8V to +2.4V, Q1 and Q2 switch states to turn the switch ON and OFF.

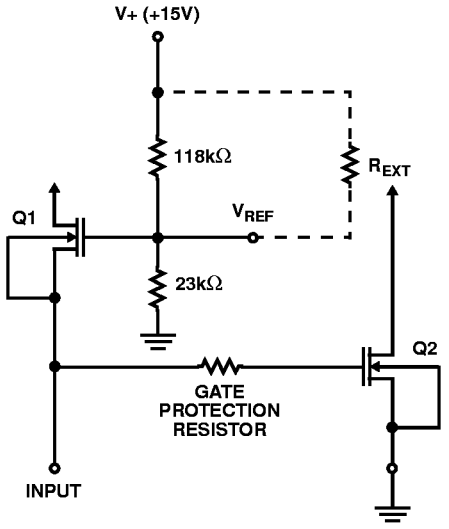


FIGURE 8.

If the power supply voltage is less than +15V, then a resistor must be added between V+ and the V_{REF} pin, to restore +2.4V at V_{REF}. The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels with a +5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of -5V to + 5V, no resistor is needed.

In general, the "low" logic level should be <0.8V to prevent Q1 and Q2 from both being ON together (this will cause incorrect switch function).

TABLE 1.

V+ SUPPLY (V)	TTL RESISTOR (kΩ)	CMOS RESISTOR (kΩ)
+15	-	-
+12	420	-
+10	190	-
+9	136	136
+8	98	98
+7	70	70

Die Characteristics

DIE DIMENSIONS:

75 mils x 78 mils x 14 mils

METALLIZATION:

Type: Al
Thickness: 10kÅ

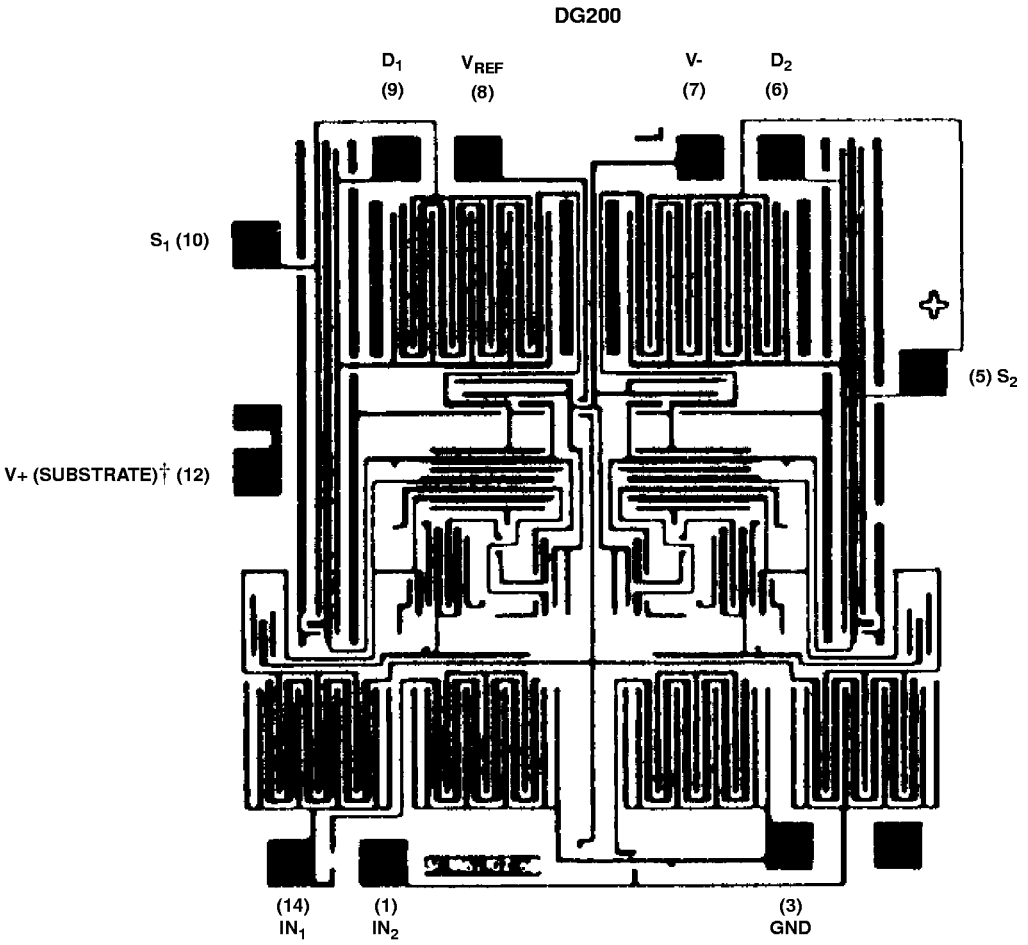
PASSIVATION:

Type: SiO_2/Si_3N_4
SiO_2 Thickness: 7kÅ
Si_3N_4 Thickness: 8kÅ

WORST CASE CURRENT DENSITY:

1×10^5 A/cm^2

Metallization Mask Layout



†BACKSIDE OF CHIP IS V+

Die Characteristics

DIE DIMENSIONS:

94 mils x 101 mils x 14 mils

METALLIZATION:

Type: Al
Thickness: 10kÅ

PASSIVATION:

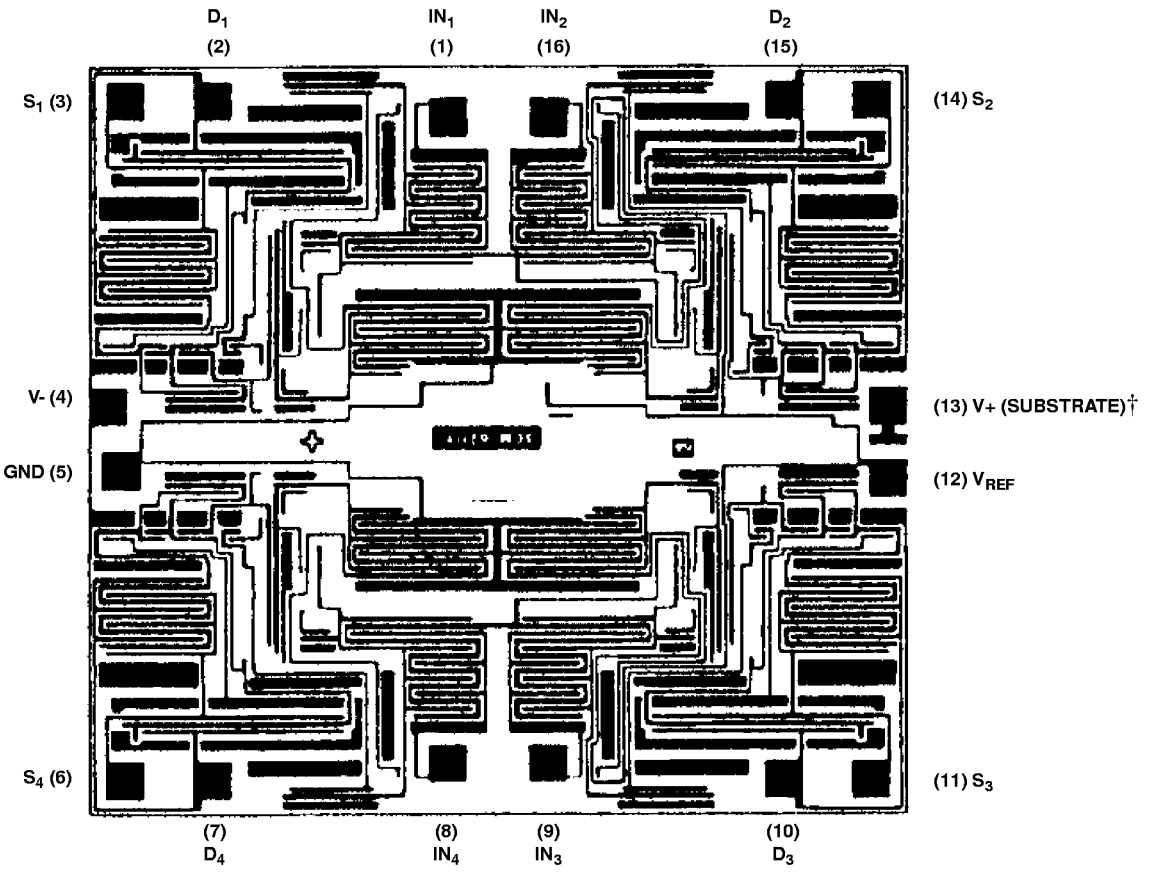
Type: SiO_2/Si_3N_4
SiO_2 Thickness: 7kÅ
Si_3N_4 Thickness: 8kÅ

WORST CASE CURRENT DENSITY:

1×10^5 A/cm^2

Metallization Mask Layout

DG201



† BACKSIDE OF CHIP IS V+