DM96LS02

Dual Retriggerable Resettable Monostable Multivibrator

The DM96LS02 is a dual retriggerable and resettable monostable multivibrator. The one-shot provides exceptionally wide delay range, pulse width stability, predictable accuracy and immunity to noise. The pulse width is set by an external resistor and capacitor. Resistor values up to 1.0 MΩ reduce required capacitor values. Hysteresis is provided on both trigger inputs of the DM96LS02 for increased noise immunity.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FAIRCHILD SEMICONDUCTOR™

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General Description

The DM96LS02 is a dual retriggerable and resettable monostable multivibrator. The one-shot provides exceptionally wide delay range, pulse width stability, predictable accuracy and immunity to noise. The pulse width is set by an external resistor and capacitor. Resistor values up to 1.0 MΩ reduce required capacitor values. Hysteresis is provided on both trigger inputs of the DM96LS02 for increased noise immunity.

Features

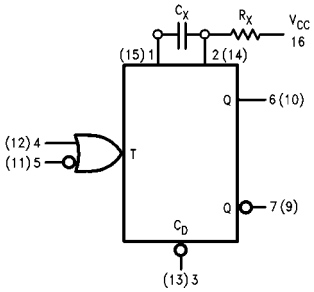
- Required timing capacitance reduced by factors of 10 to 100 over conventional designs
- Broad timing resistor range—1.0 kΩ to 2.0 MΩ
- Output Pulse Width is variable over a 2000:1 range by resistor control
- Propagation delay of 35 ns
- 0.3V hysteresis on trigger inputs
- Output pulse width independent of duty cycle
- 35 ns to ∞ output pulse width range

Ordering Code:

Order Number	Package Number	Package Description
DM96LS02M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM96LS02N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

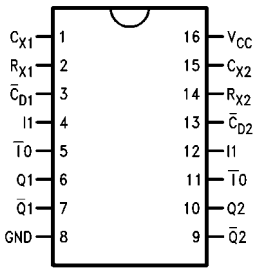
Logic Symbol



V_{CC} = Pin 16

GND = Pin 8

Connection Diagram



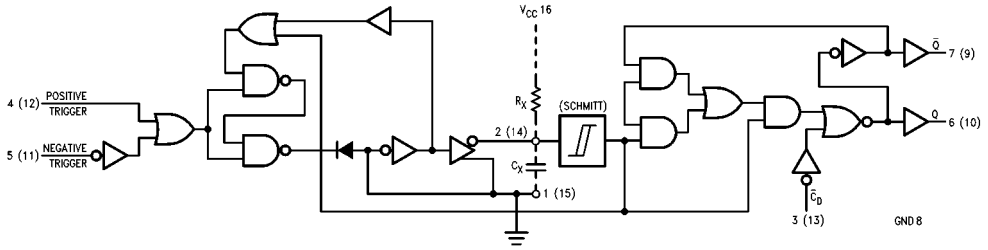
Pin Descriptions

Pin Names	Description
$\overline{I}0$	Trigger Input (Active Falling Edge)
$\overline{I}0$	Schmitt Trigger Input (Active Falling Edge)
I1	Schmitt Trigger Input (Active Rising Edge)
$\overline{C}_D$	Direct Clear Input (Active LOW)
Q	True Pulse Output
$\overline{Q}$	Complementary Pulse Output

Functional Description

The DM96LS02 dual retriggerable resettable monostable multivibrator has two DC coupled trigger inputs per function, one active LOW ($\overline{I0}$) and one active HIGH (I1). The I1 input and $\overline{I0}$ input of the DM96LS02 utilize an internal Schmitt trigger with hysteresis of 0.3V to provide increased noise immunity. The use of active HIGH and LOW inputs allows either rising or falling edge triggering and optional non-retriggerable operation. The inputs are DC coupled making triggering independent of input transition times. When input conditions for triggering are met, the Q output goes HIGH and the external capacitor is rapidly discharged and then allowed to recharge. An input trigger which occurs during the timing cycle will retrigger the circuit and result in Q remaining HIGH. The output pulse may be terminated (Q to the LOW state) at any time by setting the Direct Clear input LOW. Retriggering may be inhibited by tying the $\overline{Q}$ output to $\overline{I0}$ or the Q output to I1. Differential sensing techniques are used to obtain excellent stability over temperature and power supply variations and a feedback Darlington capacitor discharge circuit minimizes pulse width variation from unit to unit. Schottky TTL output stages provide high switching speeds and output compatibility with all TTL logic families.

Logic Diagram



Operation Notes

TIMING

1. An external resistor (R_X) and an external capacitor (C_X) are required as shown in the Logic Diagram. The value of R_X may vary from 1.0 kΩ to 1.0 MΩ.

2. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has significant leakage relative to V_{CC}/R_X the timing equations may not represent the pulse width obtained.

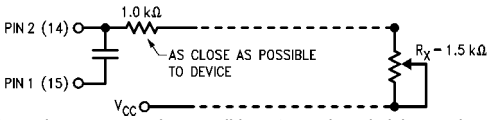
3. The output pulse width t_W for $R_X \geq 10$ kΩ and $C_X \geq 1000$ pF is determined as follows:

$$t_W = 0.43\ R_X C_X$$

Where R_X is in kΩ, C_X is in pF, t is in ns *or* R_X is in kΩ, C_X is in μF, t is in ms.

4. The output pulse width for $R_X < 10$ kΩ or $C_X < 1000$ pF should be determined from pulse width versus C_X or R_X graphs.

5. To obtain variable pulse width by remote trimming, the following circuit is recommended:



6. Under any operating condition, C_X and R_X (Min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.

7. V_{CC} and ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and ground leads do not cause interaction between one shots. Use of a 0.01 μF to 0.1 μF bypass capacitor between V_{CC} and ground located near the circuit is recommended.

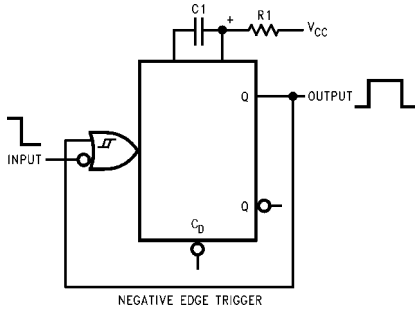
TRIGGERING

1. The minimum negative pulse width into $\overline{I0}$ is 8.0 ns; the minimum positive pulse width into I1 is 12 ns.

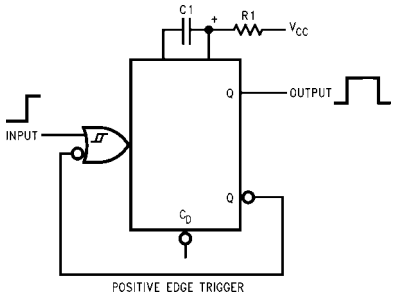
2. Input signals to the DM96LS02 exhibiting slow or noisy transitions can use either trigger as both are Schmitt triggers.

3. When non-retriggerable operation is required, i.e., when input triggers are to be ignored during quasi-stable state, input latching is used to inhibit retriggering.

4. An overriding active LOW level direct clear is provided on each multivibrator. By applying a LOW to the clear, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW. A LOW-to-HIGH transition on $\overline{C}_D$ will not trigger the DM96LS02. If the $\overline{C}_D$ input goes HIGH coincident with a trigger transition, the circuit will respond to the trigger.



Operation Notes (continued)



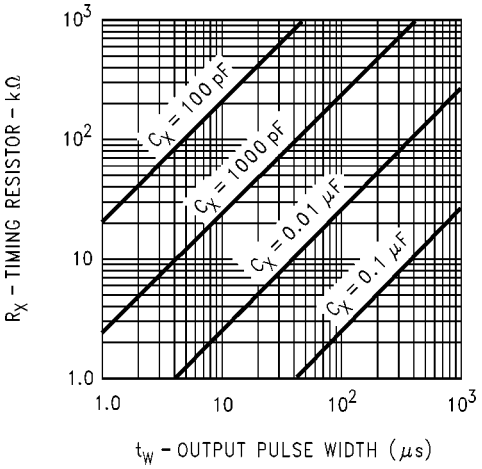
Triggering Truth Table

Pin Numbers			Operation
5(11)	4(12)	3(13)	
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

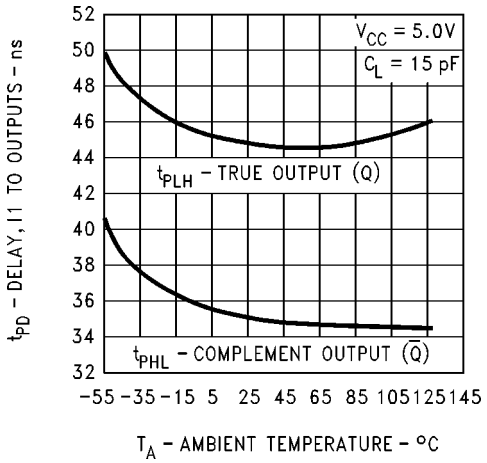
H = HIGH Voltage Level ≥ V_{IH}
L = LOW Voltage Level ≤ V_{IL}
X = Immaterial (either H or L)
H→L = HIGH-to-LOW Voltage Level Transition
L→H = LOW-to-HIGH Voltage Level Transition

Typical Performance Characteristics

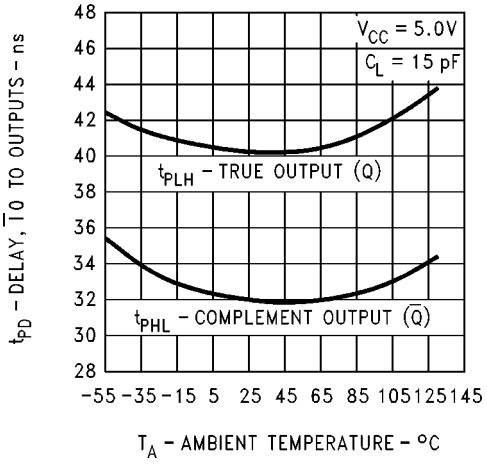
Output t_W vs. R_X and C_X



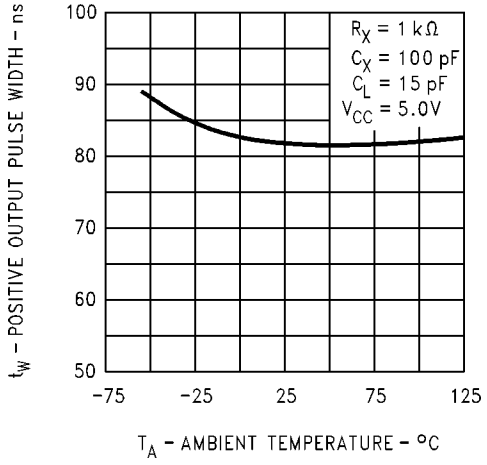
I1 Delay Time vs. T_A



$\overline{I0}$ Delay Time vs. T_A

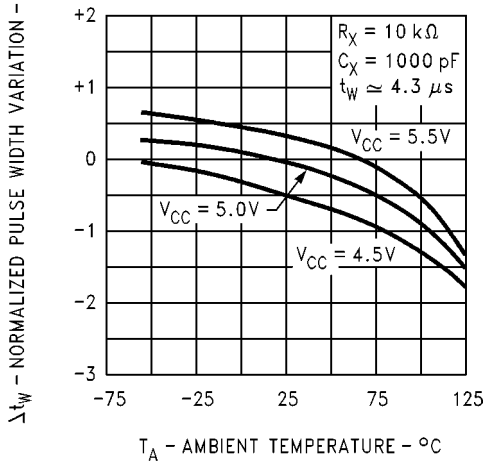


Output t_W vs. T_A

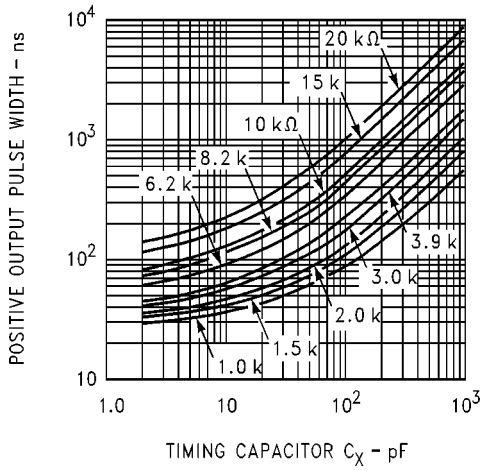


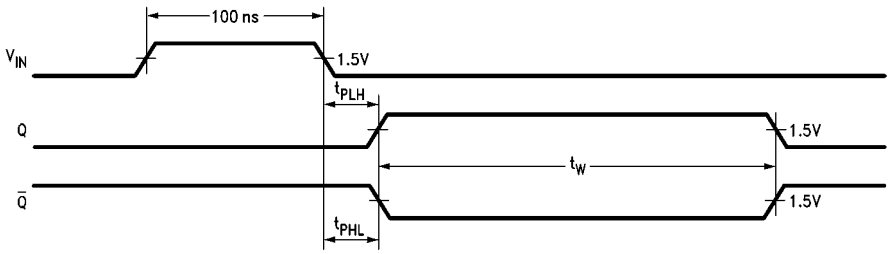
Typical Performance Characteristics (continued)

Normalized Δt_W vs. T_A



Pulse Width vs. R_X C_X





Input Pulse
f ≅ 100 kHz
Amp ≅ 3.0V
Width ≅ 100 ns
$t_r = t_f \leq 5$ ns

FIGURE 1.

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V V_I = 10V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max			36	mA
V_{T+}	Positive-Going Threshold Voltage, $\bar{I}0$, I1				2.0	V
V_{T-}	Negative-Going Threshold Voltage, $\bar{I}0$, I1		0.8			V

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

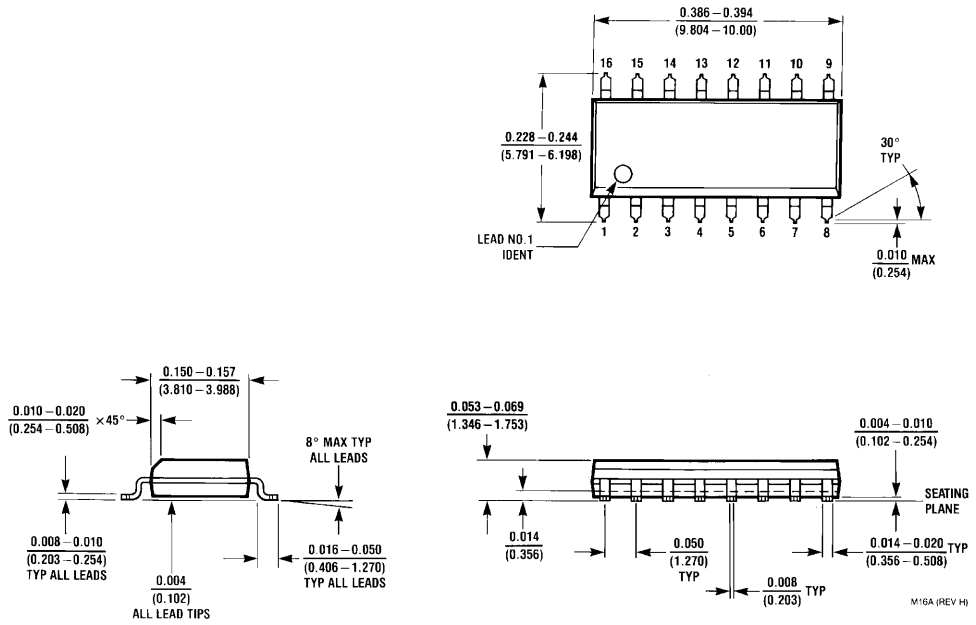
Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay $\overline{I0}$ to Q		55	ns
t_{PHL}	Propagation Delay $\overline{I0}$ to $\overline{Q}$		50	ns
t_{PLH}	Propagation Delay I1 to Q		60	ns
t_{PHL}	Propagation Delay I1 to $\overline{Q}$		55	ns
t_{PHL}	Propagation Delay $\overline{C}_D$ to Q		30	ns
t_{PLH}	Propagation Delay $\overline{C}_D$ to $\overline{Q}$		35	ns
$t_W(L)$	$\overline{I0}$ Pulse Width LOW	15		ns
$t_W(H)$	I1 Pulse With HIGH	30		ns
$t_W(L)$	$\overline{C}_D$ Pulse Width LOW	22		ns
$t_W(H)$	Minimum Q Pulse Width HIGH	25	55	ns
t_W	Q Pulse Width	4.1	4.5	µs
R_X	Timing Resistor Range (Note 4)	1	1000	kΩ
t	Change in Q Pulse Width over Temperature		1.0	%
t	Change in Q Pulse Width over V_{CC} Range		0.8 1.5	%

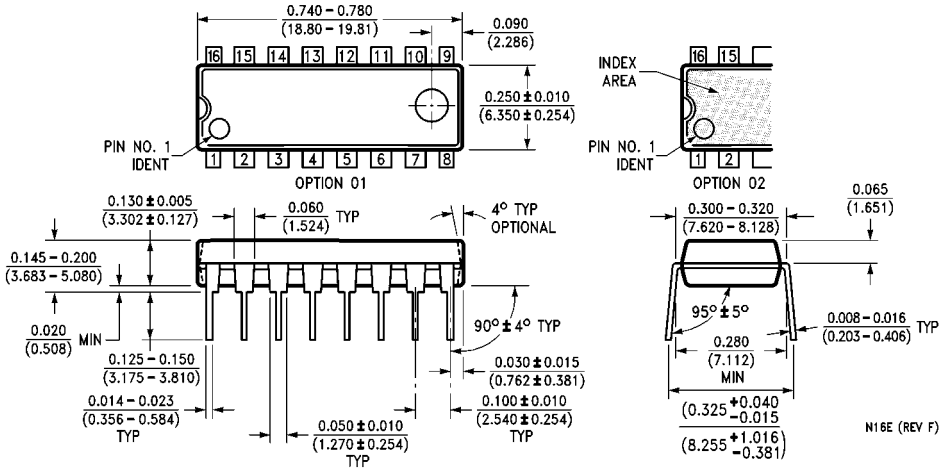
Note 4: Applies only over commercial V_{CC} and T_A range for 96S02.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E