IXF1002

Dual Port Gigabit Ethernet Controller

The Intel IXF1002 Dual Port Gigabit Ethernet Media Access Controller (MAC), provides two independent 1000 Mb/s intelligent, high-performance MAC ports. It includes Gigabit Physical Coding Sublayer (GPCS) interface network management support and is optimized for switch applications.

The IXF1002 handles Simple Network Management Protocol (SNMP) and Remove Monitoring (RMON) management counter sets, accessible through a generic CPU 8/16-bit interface, which is also used for mode programming. Each MAC port includes a 4 Kbyte FIFO for packet receive, and a 2 Kbyte FIFO for packet transmit. All the packets are transferred onto a high-performance, common IX Bus interface.

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Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

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Intel® IXF1002 Dual Port Gigabit Ethernet Controller

Datasheet

Product Features

The Intel® IXF1002 Dual Port Gigabit Ethernet Media Access Controller (MAC), provides two independent 1000 Mb/s intelligent, high-performance Media Access Control (MAC) ports. It includes Gigabit Physical Coding Sublayer (GPCS) interface network management support and is optimized for switch applications.

- Integration
  - — Offers two independent Ethernet 1000 Mb/s MAC ports
  - — Includes GPCS functions for 1000BASE-X connections
  - — Handles SNMP and RMON counters
- IX Bus
  - — Supports up to 5.12 Gbps memory bus bandwidth
  - — Variable bus speed of 33 MHz to 80 MHz
  - — 64-bit bus with three modes of operation:
    - Full — 64 bits for transmit or receive
    - Split —32 low bits for receive, and 32 high bits for transmit
    - Narrow —32 bits for transmit or receive
  - — Independent 2 Kbyte transmit FIFO and 4 Kbyte receive FIFO for each port
  - — Supports little or big endian byte ordering
  - — Supports receive packet fragmentation on byte boundaries (replay feature)
  - — Programmable transmit and receive bus thresholds
  - — Enables optional appending of packet status
- Performance
  - — Packet transfers are completed prior to servicing CPU interrupt requests
  - — Enables early address filtering ability, with packet header preprocessing
  - — IEEE P802.1Q Virtual Bridged Local Area Network (VLAN) tag append, strip and replace function on chip, during packet transmission
  - — Offers ignore or stop transmission options following packet transmission errors
  - — Provides programmable automatic discard of badly received packets such as cyclic redundancy (CRC) errors and too long packets
  - — Informs the system in case bad packets start to appear on the FIFO bus
  - — Allows interpacket gap (IPG) programming
- Serial
  - — Enables independent mode of operation in each port
  - — Supports IEEE 802.3x standard flow-control functionality
  - — Interfaces standard GPCS connections (10b interface)
  - — Interfaces standard GMII connections
  - — Supports 1000BASE-SX, 1000BASE-LX, 1000BASE-CX, and 1000BASE-T connections
  - — Provides programmable CRC generation and removal
  - — Supports Auto-Negotiation link protocol for 1000BASE-X
  - — Implements only full-duplex operation
  - — Complies with IEEE 802.3z standard
  - — Supports large packets of up to 64 Kbytes
- CPU Interface
  - — Supports fully programmable independent ports through a dedicated generic CPU port
  - — Supports interrupt programming
  - — Provides an 8- or 16-bit bus for register access
- Device
  - — CPU and FIFO interfaces are compatible with the IXF440 Multiport 10/100 Mbps Ethernet Controller and the IXP1200 Network Processor.
  - — Includes internal and external loopback capabilities
  - — Provides software reset support
  - — Supports JTAG boundary scan
  - — Implemented in a low-power 3.3 V and 5 V tolerant CMOS device
  - — 304-ESBGA package.

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Revision History

Date	Revision	Description
8/31/99	001	Initial release.
12/15/99	002	Format revision, electrical specification updates.
5/26/00	003	Updates for IXP1200 v1.0 release.
9/26/00	004	Changed to Intel branding with updates for IXP1200 v1.1 release.
12/13/00	005	Updates for IXP1200 v1.2 release.
05/18/01	006	Updates for the V1.3 SDK.
10/02/01	007	Changes to Table 16, Table 18, Section 9.0, Figure 56.
5/23/02	008	Change to Figure 31; removed extended temperature QDF references; added footnote to Table 5.

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1.0 Introduction

1.1 General Description

The Intel® IXF1002 Dual-Port Gigabit Ethernet Controller includes two full-duplex independent 1000 Mb/s Ethernet controllers and interfaces directly to Gigabit Ethernet standard transceivers through its Gigabit Media Independent Interface (GMII) or GPCS interface. The IXF1002 handles Simple Network Management Protocol (SNMP) and Remote Monitoring (RMON) management counter sets, accessible through a generic CPU 8/16-bit interface, which is also used for mode programming. Each MAC port includes a 4 Kbyte FIFO for packet receive, and a 2 Kbyte FIFO for packet transmit. All the packets are transferred onto a high-performance, common IX Bus interface. The IXF1002 CPU and IX Bus interfaces are compatible to the Intel® 21440 Octal Fast Ethernet Controller device.

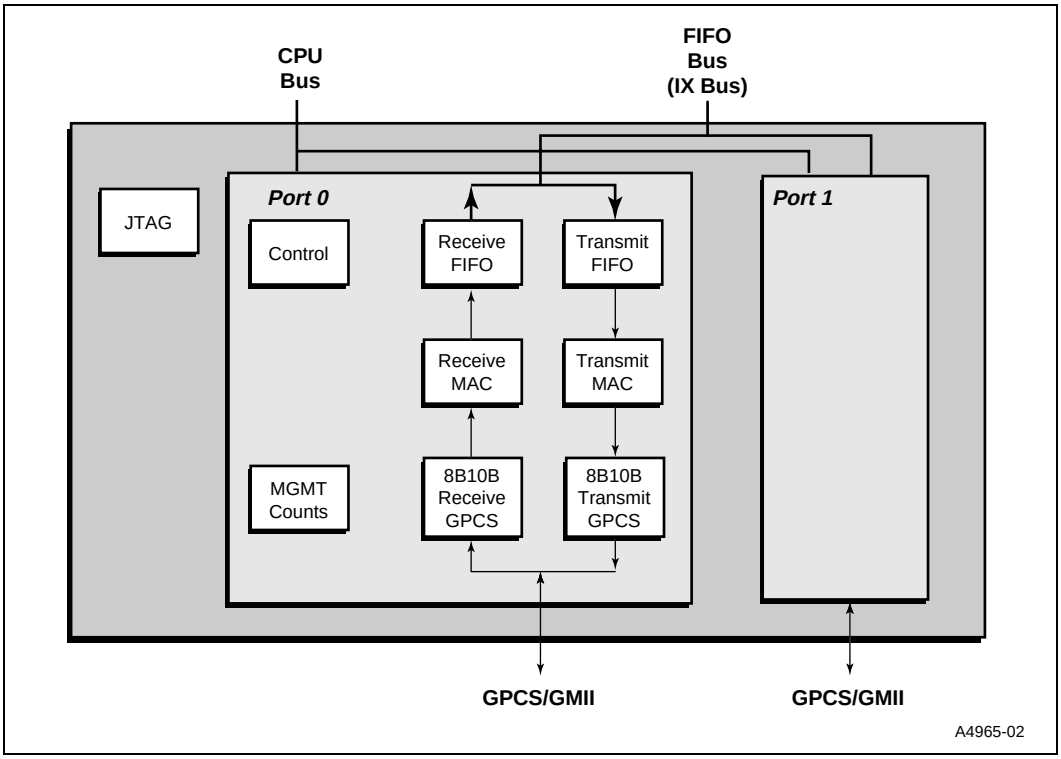
The IXF1002 is fully compatible with IEEE 802.3x and 802.3z standards, including Auto-Negotiation and flow-control support.

It is implemented in a low-power 3.3 V CMOS device within a 304-ESBGA package.

1.2 Block Diagram

Figure 1 shows the IXF1002 block diagram.

Figure 1. Block Diagram



1.3 Hardware Overview

Table 1 describes the IXF1002 components.

Table 1. Component Description

Component	Description
Transmit FIFO	A 2 Kbyte buffer for temporary storage of transmitted packets. The transmit FIFO has direct interface to the IX Bus.
Receive FIFO	A 4 Kbyte buffer for temporary storage of received packets. Supports packet deletion in case of errors. The receive FIFO has direct interface to the IX Bus.
Transmit MAC	Implements the IEEE 802.3 transmit full-duplex MAC functions while interfacing between the transmit FIFO and the GMII PHY or the GPCS function.
Receive MAC	Implements the IEEE 802.3 receive full-duplex MAC functions while interfacing between the receive FIFO and the GMII PHY or the GPCS function.
GPCS	Implementing the 1000BASE-X PCS layer that includes the Auto-Negotiation synchronization and encoding/decoding functions.
SNMP and RMON	Handles network statistic counters for SNMP and RMON.
Control	Handles the chip registers accessible through the CPU bus.
JTAG	Includes the JTAG technologies IEEE 1149.1 (JTAG) boundary scan logic.

2.0 Pinout

This chapter describes the IXF1002 pinouts.

2.1 Signal Description

Table 2 describes the IXF1002 signals.

The following conventions are used in the signal names:

_l:	Indicates that the pin is active low.
{i}:	The i subscript appended to pin names indicates that each port has its own pin (numbered from 0 to 1).
<m:l>:	Refers to a pin number within a bus (m is the most significant, l is the least significant).

The following abbreviations are used in Table 2:

I	=	Input
O	=	Output
OD	=	Open Drain
I/O	=	Input/Output

Table 2. Signal Descriptions (Sheet 1 of 6)

Signal Name	I/O	Pin Description
CPU Interface		
cs_l	I	Chip select. This pin must be asserted to enable CPU access to the chip registers.
cps	I	CPU port select. Selects one of the two internal ports for register accesses. When asserted, port number 1 is selected. when deasserted, port number 0 is selected.
crd_l	I	Read strobe. Upon assertion, the address signals cadd<9:0>, cs_l, and cps are latched by the chip. Deassertion occurs after the read data is latched from the cdat<15:0> bus.
cwr_l	I	Write strobe. Upon assertion, the address signals cadd<9:0>, cs_l, and cps are latched by the chip. Deassertion must occur while the data is valid on the cdat<15:0> bus.
crdy_l	OD	Ready indication. When asserted, indicates that either data is stable on the cdat<15:0> bus during read access or that data was latched by the chip during write access.
cadd<9:0>	I	Address bus. Selects one of the internal registers to be accessed.

Table 2. Signal Descriptions (Sheet 2 of 6)

Signal Name	I/O	Pin Description
cdat<15:0>	I/O	CPU data bus. In 8 bit mode (default): • cdat<7:0> carries data to be written to or read from the registers. • cdat<15:8> should be connected to pull up resistors. In 16 bit mode: • cdat<15:0> carries data to be written to or read from the registers.
cint{i}_l	OD	Interrupt lines. These signals are asserted following a variety of programmable conditions. Deassertion occurs after reading the events that cause the interrupt, unless another interrupt is registered meanwhile.
reset_l	I	General reset. Upon reset, all the registers are reset to their default values and the FIFOs are flushed. reset_l assertion time should be at least 1 ms.
IX Bus Interface		
clamp	I	Vdd clamp. Should be connected to the power of the highest signal level used on the IX Bus.
clk	I	System clock. All the FIFO data transfers are synchronized to this clock.
txsel_l	I	Transmit select. This pin must be asserted to enable transmit FIFO write access.
rxsel_l	I	Receive select. This pin must be asserted to enable receive FIFO read access. The following signals are driven by the IXF1002 upon assertion of rxsel_l: • fdat<63:0>, fbe_l<7:0>, sop, eop and rxfail in full-64 IX Bus mode. • fdat<31:0>, fbe_l<3:0>, sop_rxf, eop_rxf and rxfail in split IX Bus mode. • fdat<31:0>, fbe_l<3:0>, sop, eop and rxfail in narrow IX Bus mode.
fps/fps_rxf	I	FIFO port select. In full-64 mode and in narrow mode (fps): • When asserted, selects port no. 1 for data transfer through the IX Bus. • When deasserted, selects port no. 0 for data transfer through the IX Bus. In split mode(fps_rxf): • Selects one of the ports for reading data, through fdat<31:0>, from the receive FIFO of the selected port.
fps_txf	I	FIFO port select. In full-64 mode and in narrow mode: • Not in use, should be connected to pull up resistors. In split mode: • Selects one of the ports for writing data, through fdat<63:32>, to the transmit FIFO of the selected port.

Table 2. Signal Descriptions (Sheet 3 of 6)

Signal Name	I/O	Pin Description
fdat<63:0>	I/O	FIFO data bus. In full-64 mode: • fdat<63:0> (I/O) carries the data to be written to the transmit FIFO or read from the receive FIFO of the selected port. In split mode: • fdat<31:0> (output) carries the data to be read from the receive FIFO of the selected port. • fdat<63:32> (input) carries the data to be written to the transmit FIFO of the selected port. In narrow mode: • fdat<31:0> (I/O) carries the data to be written to the transmit FIFO or to be read from the receive FIFO of the selected port. • fdat<63:32> should be connected to pull up resistors.
fbe_l<7:0>	I/O	FIFO byte enable. In full-64 mode: • During transmit, fbe_l<7:0> indicates which of the bytes driven onto fdat<63:0> contain valid data (valid bytes need to be contiguous and at least one byte must be valid). During receive, fbe_l<7:0> indicates which bytes are valid. Each fbe_l signal relates to a different fdat byte (for example, fbe_l<0> relates to fdat<7:0> and fbe_l<5> relates to fdat<47:40>). In split mode: • fbe_l<3:0> (output) relates to fdat<31:0> that is directed out of the port (receive FIFO). • fbe_l<7:4> (input) indicates valid data on fdat<63:32> that is directed into the port (transmit FIFO). In narrow mode: • fbe_l<3:0> (I/O) relates to fdat<31:0> that is directed in/out of the port. • fbe_l<7:4> should be connected to pull up resistors.
rxkep	I	Receive keep. When asserted, this signal causes the last read data to be kept in the receive FIFO. May be asserted only with rxsel_l assertion.
sop/sop_rxf	I/O	Start of packet. In full-64 mode and in narrow mode (sop – I/O): • When asserted during transmit, indicates that the first data in the packet is transferred to the transmit FIFO. During receive, this signal is asserted when the first data in the packet is transferred from the receive FIFO to the IX Bus. In split mode (sop_rxf – output): • During receive, this signal is asserted when the first data in the packet is transferred from the receive FIFO to the IX Bus.
sop_txf	I	Start of packet. In full-64 mode and in narrow mode: • This signal is not in use and should be connected to a pull up resistor. In split mode: • During transmit, indicates that the first data in the packet is written to the transmit FIFO.

Table 2. Signal Descriptions (Sheet 4 of 6)

Signal Name	I/O	Pin Description
eop/eop_rxf	I/O	End of packet. In full-64 mode and in narrow mode (eop – I/O): • When asserted during transmit, indicates that the final data in the packet is written to the transmit FIFO. During receive, eop is asserted when the final data of the packet is transferred from the receive FIFO to the IX Bus. In split mode (eop_rxf – output): • During receive, eop_rxf is asserted when the final data of the packet is transferred from the receive FIFO to the IX Bus. In the following FIFO access cycle, the packet status is driven onto the bus (see Section 4.3.1.1).
eop_txf	I	End of packet. In full-64 mode and in narrow mode: • This signal is not in use and should be connected to a pull up resistor. In split mode: • During transmit, indicates that the final data in the packet is written to the transmit FIFO.
vtg	I	VLAN tag. When asserted during transmit before sop assertion, VLAN tag will be appended to the transmitted packet. When asserted during transmit together with sop assertion, VLAN tag will be stripped from the transmitted packet. When asserted during transmit before and also together with sop assertion, VLAN tag will be replaced. See Section 4.2.2 for more details. **NOTE:** In case of VLAN tag append, strip or replace, the frame check sequence (FCS) field will be calculated by the IXF1002 (see Section 4.2.2.1).
txasis/txerr	I	Transmit as is/Transmit error. When asserted during transmit, upon transfer of the packet's first data (together with sop assertion), no padding and/or CRC is appended to the packet even if the port was programmed to do so. When asserted upon transfer of the packet's final data (together with eop assertion), the packet is transmitted with a CRC error (if the port is programmed to append CRC), and a GMII error or a symbol error (GPCS mode).
rxfail	O	Receive packet failure. This signal is asserted if a packet was received with errors, had started to appear on the IX Bus, and was discarded from the receive FIFO.
rxabt	I	Receive abort. This signal forces a received packet, that is currently being transferred to the IX Bus, to be aborted and flushed from the receive FIFO. May be asserted only with rxsel_l assertion. Any following packets loaded onto the receive FIFO are not affected by rxabt assertion.
flct_{i}	I	Flow control. When asserted, a flow-control packet with the programmed pause time is transmitted. Upon deassertion, a flow-control packet with time equal to 0 is sent if programmed accordingly. For correct latch of flct pin in the chip - signal flct_{i} should be valid until 1 cycle after flct_lat deassertion.
flct_lat	I	Flow control pin enable When asserted the flct_{i} pin will be sampled by the IXF1002. When deasserted, the IXF1002 will latch the value of the flct_{i} pin, ignoring subsequent changes to the flct_{i} pin.
txctl_l	I	Transmit control enable. When asserted, this pin enables the txrdy_{i} output drivers to report the transmit FIFO status.
rxctl_l	I	Receive control enable. When asserted, this pin enables the rxrdy_{i} output drivers to report the receive FIFO status.

Table 2. Signal Descriptions (Sheet 5 of 6)

Signal Name	I/O	Pin Description
txrdy_{i}	O	Transmit FIFO ready. Indicates whether there is enough available space in the transmit FIFO to load data according to the programmable threshold value. Following transmission stop due to an error, the txrdy signal remains deasserted until the transmit error status is read.
rxrdy_{i}	O	Receive FIFO ready. Indicates whether there is enough available data in the receive FIFO to be stored according to the programmable threshold value or if the end of the transferred packet is in the FIFO. The rxrdy signal may also be programmed to assert when the packet header is in the FIFO. rxrdy can also be asserted to report packet discard from the receive FIFO due to an error together with the rxfail signal.
GMII / GPCS Interface		
NOTE: The following pins have various functions according to the port mode: GMII or GPCS. For a detailed description, turn to Section 6.0.		
tclk	I	125 MHz clock for reference.
gtxclk_{i}/pmatclk_{i}	O	GMII mode: 125 MHz Transmit clock. GPCS mode: 125 MHz Transmit clock.
txd_{i}<7:0>	O	GMII mode: Byte transmit data. GPCS mode: Eight low bits of the encoded transmit data.
ten{i}/txd{i}<8>	O	GMII mode: Transmit enable signal. GPCS mode: The ninth bit of the encoded transmit data.
terr{i}/txd{i}<9>	O	GMII mode: Transmit error signal. GPCS mode: The tenth bit of the encoded transmit data.
rclk_{i}	I	GMII mode: Receive recovered 125 MHz clock. GPCS mode: The 62.5 MHz recovered receive byte clock. Used to latch odd numbered bytes of the receive data.
pmarclk_{i}	I	GMII mode: Not in use, should be connected to a pull up resistor. GPCS mode: The 62.5 MHz recovered receive byte clock. Used to latch even numbered bytes of the receive data.
rxd_{i}<7:0>	I	GMII mode: Byte receive data. GPCS mode: Eight low bits of the encoded received data.
dv{i}/rxd{i}<8>	I	GMII mode: Receive enable signal. GPCS mode: The ninth bit of the encoded received data.
rerr{i}/rxd{i}<9>	I	GMII mode: Receive error signal. GPCS mode: The tenth bit of the encoded received data.
sd_{i}	I	GMII mode: Not in use, should be connected to a pull up resistor. GPCS mode: Signal detect. Indicates whether the PHY has detected an input signal at the serial input. If this signal is not driven into the IXF1002, PORT_MODE<SDDIS> bit should be set.
lnk_{i}	O	GMII mode: Not in use, should be connected to a pull up resistor. GPCS mode: Link indication. When asserted, indicates link up. Meaning the synchronization process and the Auto-Negotiation process were completed and the device is ready to transmit or receive data.
act_{i}	O	GMII mode: Not in use, should be connected to a pull up resistor. GPCS mode: Activity indication. When asserted, indicates that data is being transmitted or received.

Table 2. Signal Descriptions (Sheet 6 of 6)

Signal Name	I/O	Pin Description
ewrap_{i}	O	GMII mode: Not in use, should be connected to a pull up resistor. GPCS mode: Enable Wrap. When asserted, the PHY should loop the transmit serialized data to the receive section. This pin is controlled by bit LPBK in the GMII management control register (GMII_CTL).
lckref_l_{i}	O	GMII mode: Not in use, should be connected to a pull up resistor. GPCS mode: Lock to reference. When asserted, enables the PHY to lock its PLL to the 125 MHz reference clock. This pin is controlled by bit LCKE in the PORT_MODE register.
encdet_{i}	O	GMII mode: Not in use, should be left unconnected. GPCS mode: Enable comma detect. When asserted, enables the PHY for comma detect and word resynchronization. When deasserted, the PHY will keep current word alignment and will not try to detect new commas.
comdet_{i}	I	GMII mode: Not in use, should be connected to a pull up resistor. GPCS mode: Comma detect. An indication from the PHY layer that the data contains a valid comma character.
mdc	I/O	GMII management clock. This pin is output after reset. Should be connected to a pull-up resistor. MDC can be used as a general purpose pin according to the GMII_MGNG_ACC register. The mdc pin drives 0 by default and its output enable is controlled by bit MDCEN in register MII_MNG_ACC.
mdio	I/O	GMII management input/output serial data. Should be connected to a pull up resistor. MDIO can be used as a general purpose pin according to the GMII_MGNG_ACC register.
JTAG Interface		
tck	I	JTAG clock. If this pin is not used, it must be connected to 0.
tms	I	JTAG test mode. If this pin is not used, it must be connected to 1.
tdi	I	JTAG data serial input. If this pin is not used, it must be connected to 1.
tdo	O	JTAG data serial output.

2.2 Pin Count

Table 3 summarizes the IXF1002 pin count.

Table 3. IXF1002 Pin Count

Block	Common	Per Port	Total
CPU	32	1	34
FIFO	90	3	96
GMII/GPCS	3	30	63
JTAG	4		4
Total i/o	129	68	197
Gnd	36		36
Vdd	36		36
Reserved	35		35
Total	236	68	304

2.3 Connection Rules

- All the reserved pins must remain unconnected.
- All the Open Drain (OD) signals must be connected to a pull-up device.
- All signals connected to a fixed value should be connected through a resistive device. The following are recommended resistor values:
  - Unused I/O pins: 10 KΩ pull-up
  - Unused I pins: 1–10 KΩ pull-up or pull-down
  - Unused O pins: no pull-up required
  - OD pins: R=T/C (required signal deassertion time (T) divided by capacitive load (C))

Note: Unless otherwise specified, all defined pins that are not in use must be connected to a pull-up device.

2.4 Pin List

Table 4 lists the IXF1002 pins. Pins associated names are to be defined.

Table 4. Pin List (Sheet 1 of 3)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
AA11	act_0	H3	clamp	C1	fdat<5>
Y23	act_1	C12	clk	E4	fdat<6>
N22	cadd<0>	W2	comdet_0	D3	fdat<7>
N21	cadd<1>	AC13	comdet_1	D5	fdat<8>
N20	cadd<2>	T21	cps	A3	fdat<9>
P23	cadd<3>	T20	crd_l	B4	fdat<10>
P22	cadd<4>	V22	crdy_l	C5	fdat<11>
R23	cadd<5>	U22	cs_l	A4	fdat<12>
P20	cadd<6>	U21	cwr_l	B5	fdat<13>
R22	cadd<7>	AB5	dv_0/rxd0<8>	C6	fdat<14>
R21	cadd<8>	AB16	dv_1/rxd1<8>	D7	fdat<15>
T22	cadd<9>	Y7	encdet_0	B6	fdat<16>
U2	cdat<0>	AA17	encdet_1	C7	fdat<17>
T3	cdat<1>	H4	eop/eop_rxf	D8	fdat<18>
U1	cdat<2>	G3	eop_txf	B7	fdat<19>
T2	cdat<3>	AC5	ewrap_0	C8	fdat<20>
R2	cdat<4>	AB18	ewrap_1	A7	fdat<21>
P4	cdat<5>	L3	fbe_l<0>	B8	fdat<22>
R1	cdat<6>	L4	fbe_l<1>	B9	fdat<23>
P3	cdat<7>	K1	fbe_l<2>	D10	fdat<24>
P2	cdat<8>	K2	fbe_l<3>	A9	fdat<25>
P1	cdat<9>	J1	fbe_l<4>	C10	fdat<26>
N4	cdat<10>	J2	fbe_l<5>	B10	fdat<27>
N3	cdat<11>	J3	fbe_l<6>	A10	fdat<28>
N1	cdat<12>	H2	fbe_l<7>	C11	fdat<29>
M2	cdat<13>	F3	fdat<0>	B11	fdat<30>
M3	cdat<14>	E2	fdat<1>	A11	fdat<31>
L1	cdat<15>	D1	fdat<2>	A13	fdat<32>
U20	cint_1_l	E3	fdat<3>	C13	fdat<33>
W23	cint_0_l	D2	fdat<4>	D13	fdat<34>

Table 4. Pin List (Sheet 2 of 3)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
A14	fdat<35>	A6	gnd	AB6	gtxclk_0
B14	fdat<36>	A8	gnd	Y16	gtxclk_1
C14	fdat<37>	A12	gnd	AB11	lckref_l_0
A15	fdat<38>	A16	gnd	w22	lckref_l_1
D14	fdat<39>	A18	gnd	Y11	lnk_0
C15	fdat<40>	A22	gnd	W21	lnk_1
B16	fdat<41>	AA22	gnd	AC11	mdc
C16	fdat<42>	B1	gnd	AA12	mdio
A17	fdat<43>	B3	gnd	A21	nc
D16	fdat<44>	B21	gnd	B13	nc
C17	fdat<45>	B23	gnd	B15	nc
B18	fdat<46>	C2	gnd	B17	nc
A19	fdat<47>	C22	gnd	C20	nc
D17	fdat<48>	F1	gnd	C4	nc
C18	fdat<49>	F23	gnd	C9	nc
B19	fdat<50>	H1	gnd	D11	nc
A20	fdat<51>	H23	gnd	D19	nc
C19	fdat<52>	M1	gnd	E21	nc
B20	fdat<53>	M23	gnd	G2	nc
D21	fdat<54>	T1	gnd	G21	nc
E20	fdat<55>	T23	gnd	G4	nc
C23	fdat<56>	V1	gnd	J23	nc
D22	fdat<57>	V23	gnd	K23	nc
D23	fdat<58>	AA2	gnd	K3	nc
E22	fdat<59>	AB1	gnd	K4	nc
F21	fdat<60>	AB3	gnd	L2	nc
G20	fdat<61>	AB21	gnd	N2	nc
E23	fdat<62>	AB23	gnd	N23	nc
F22	fdat<63>	AC2	gnd	P21	nc
L23	flct_0	AC6	gnd	R3	nc
M22	flct_1	AC8	gnd	T4	nc
L22	flct_lat	AC12	gnd	U23	nc
G22	fps/fps_rxf	AC16	gnd	V3	nc
H20	fps_txf	AC18	gnd	Y13	nc
A2	gnd	AC22	gnd	Y14	nc

Table 4. Pin List (Sheet 3 of 3)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
Y19	nc	G23	rxfail	A1	vcc
AA4	nc	L20	rxrdy_0	A23	vcc
AA9	nc	L21	rxrdy_1	B2	vcc
AA20	nc	AB10	sd_0	B22	vcc
AC4	nc	Y22	sd_1	C3	vcc
AC10	nc	E1	sop/sop_rxf	C21	vcc
AC21	nc	F2	sop_txf	D4	vcc
V21	nc	U3	tck	D6	vcc
AA5	pmarclk_0	U4	tdo	D9	vcc
AA16	pmarclk_1	W1	tdi	D12	vcc
AB4	rclk_0	Y8	ten0/txd0<8>	D15	vcc
AC17	rclk_1	Y17	ten1/Txd1<8>	D18	vcc
AB12	tclk	AA7	terr0/txd0<9>	D20	vcc
AA6	rerr0/rxd0<9>	AC19	terr1/txd1<9>	F4	vcc
AB17	rerr1/rxd1<9>	V2	tms	F20	vcc
M21	reset_l	H21	txasis/txerr	J4	vcc
H22	rxkep	J22	txctl_l	J20	vcc
A5	rxsel_l	AA10	txd_0<0>	M4	vcc
J21	rxabt	AC9	txd_0<1>	M20	vcc
K20	rxctl_l	Y10	txd_0<2>	R4	vcc
Y1	rxd_0<0>	AB9	txd_0<3>	R20	vcc
W3	rxd_0<1>	AB8	txd_0<4>	V4	vcc
Y2	rxd_0<2>	AA8	txd_0<5>	V20	vcc
AA1	rxd_0<3>	AC7	txd_0<6>	Y4	vcc
W4	rxd_0<4>	AB7	txd_0<7>	Y6	vcc
Y3	rxd_0<5>	AA23	txd_1<0>	Y9	vcc
Y5	rxd_0<6>	W20	txd_1<1>	Y12	vcc
AC3	rxd_0<7>	Y21	txd_1<2>	Y15	vcc
AB13	rxd_1<0>	AB20	txd_1<3>	Y18	vcc
AA13	rxd_1<1>	AA19	txd_1<4>	Y20	vcc
AC14	rxd_1<2>	AC20	txd_1<5>	AA3	vcc
AB14	rxd_1<3>	AB19	txd_1<6>	AA21	vcc
AA14	rxd_1<4>	AA18	txd_1<7>	AB2	vcc
AC15	rxd_1<5>	K21	txrdy_0	AB22	vcc
AB15	rxd_1<6>	K22	txrdy_1	AC1	vcc
AA15	rxd_1<7>	B12	txsel_l	AC23	vcc
				G1	vtg

3.0 Registers Description

This section describes the IXF1002 registers. Each of the IXF1002 ports includes an independent register set, enabling maximum flexibility.

The registers in each port are divided into two groups:

- Control and status registers (CSRs)
- Network statistics counters

3.1 Register Conventions

All the registers in the IXF1002 are implemented in each of its two ports, unless mentioned otherwise in the text.

In the register description tables throughout this section, the following abbreviations are used to indicate register access modes:

R	=	Readable only.
W	=	Writable only.
R/W	=	Readable and writable.

3.1.1 Access Rules

The following access rules must be followed when accessing registers:

- Unlisted addresses are reserved and must not be accessed.
- The resolution of the addresses is in bytes.
- In 8-bit mode, access to the eight high or low bits of a register will be done directly to the address of the desired byte.
- In 16-bit mode, registers must be accessed with even addresses.
- Reserved bits on registers must be written as 0 and are unpredictable on read.
- All registers, except PORT_CTL, are writable only when the port is in stop state (as reported in the interrupt status register – INT_STT), following transmit and receive disable programming.
- Multibyte registers are ordered from low to high (the lower address points to the lower byte).

3.2 CSR Register

This describes the IXF1002 CSR register mapping.

3.2.1 Register Mapping

Table 5 lists each CSR register name, mnemonic, address, and the section that describes the register.

Table 5. CSR Register Mapping

Register Description	Mnemonic	I/O Address[1]	Section
Base Registers			3.2.2
Interrupt status register	INT_STT	00H – 01H	3.2.2.1
Interrupt enable register	INT_EN	02H – 03H	3.2.2.2
Port control register	PORT_CTR	04H – 05H	3.2.2.3
Identification and revision number register	ID_REV	06H – 07H	3.2.2.4
Transmit and receive status register	TX_RX_STT	08H – 09H	3.2.2.5
Transmit counter overflow status register	TX_OV_STT	0AH – 0DH	3.2.2.6
Receive counter overflow status register	RX_OV_STT	0EH – 11H	3.2.2.7
Configuration Registers			3.2.3
Transmit and receive error mode register	TX_RX_ERR	20H – 21H	3.2.3.1
FIFO threshold register	FFO_TSHD	22H – 23H	3.2.3.2
Port working mode register	PORT_MODE	24H – 25H	3.2.3.3
Transmit and receive parameter register	TX_RX_PARAM	26H – 27H	3.2.3.4
Transmit threshold register	TX_TSHD	28H – 29H	3.2.3.5
Transmit flow-control pause time register	PAUSE_TIME	2AH – 2BH	3.2.3.6
Maximum packet size register	PKT_MAX_SIZE	2CH – 2DH	3.2.3.7
Inter packet gap value	IPG_VAL	2EH – 2FH	3.2.3.8
MAC address register	MAC_ADD	30H – 35H	3.2.3.9
VLAN tag length/type register	VLAN_TAG	36H – 37H	3.2.3.10
Transmit counter overflow mask register	TX_OV_MSK	38H – 3BH	3.2.3.11
Receive counter overflow mask register	RX_OV_MSK	3CH – 3FH	3.2.3.12
GMII Management Access Registers (used in GMII mode)			3.2.4
GMII management access register	GMII_MNG_ACC	4AH – 4BH	3.2.4.1
GMII management data register	GMII_MNG_DAT	4CH – 4DH	3.2.4.2
GMII Management Register Set (used in GPCS mode)			3.2.5
GMII Control register	GMII_CTL	50H – 51H	3.2.5.1
GMII Status register	GMII_STT	52H – 53H	3.2.5.2
AN advertisement register	AN_ADV	58H – 59H	3.2.5.3
AN link partner ability base page register	AN_PRT_ABL	5AH – 5BH	3.2.5.4
AN expansion register	AN_EXP	5CH – 5DH	3.2.5.5
AN next page transmit register	AN_NP_TR	5EH – 5FH	3.2.5.6
AN link partner receive next page register	AN_PRT_NP	60H – 61H	3.2.5.7
Extended status register	GMII_EXT_STT	6EH – 6FH	3.2.5.8
GPCS status register	GPCS_STT	70H – 71H	3.2.5.9

1. The offset to the StrongArm® core is 0x38408000. This address is required to access the CSRs from the core.

3.2.2 Base Registers

The following sections describe the individual base registers.

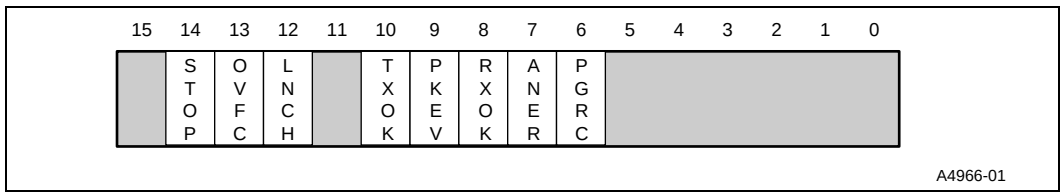
3.2.2.1 Interrupt Status Register

Mnemonic: INT_STT

Address: 00H – 01H

The interrupt status register handles information regarding events that cause an interrupt. A specific event sets a bit if it was programmed to generate an interrupt in the interrupt enable register (INT_EN).

Reading this register will reset all the bits, except for PKEV and OVFC bits. These bits are reset only when the asserted bits in the relevant status registers are reset by read.



Bit Name	Bit #	Bit Description
—	15	RESERVED
STOP	14	**Port stop.** Indicates that transmit or receive path is in the stop state, following disable programming in the port control register. If both transmit and receive paths are programmed to be stopped, this bit is set when they both reach the stop state.
OVFC	13	**Counter overflow.** Indicates that at least one network statistic counter has reached its highest possible value. This bit is a logical OR of all bits in the counter overflow status registers (see Section 3.2.2.6 and Section 3.2.2.7).
LNCH	12	**Link change.** Indicates that a link change has occurred while working in GPCS mode. The actual link status is reported in the GMII status register GMII_STT<LNKSTT> (see Section 3.2.5.2).
—	11	RESERVED
TXOK	10	**Transmit OK.** Indicates successful packet transmission.
PKEV	9	**Packet event.** A logical OR of all the bits in the transmit and receive status register (TX_RX_STT), excluding the packet count (PKC) bits. Upon receive events, this bit is set only after the packet is fully received by the chip.
RXOK	8	**Receive OK.** Indicates that a packet has been received without error. This bit is set only after the packet is fully received by the chip.
ANER	7	**Auto-Negotiation error.** Indicates that the link partner advertises that it does not support full-duplex operation, and that Auto-Negotiation was restarted.
PGRC	6	**Page received.** Indicates that a base or next page has been received during Auto-Negotiation process.
—	5:0	RESERVED

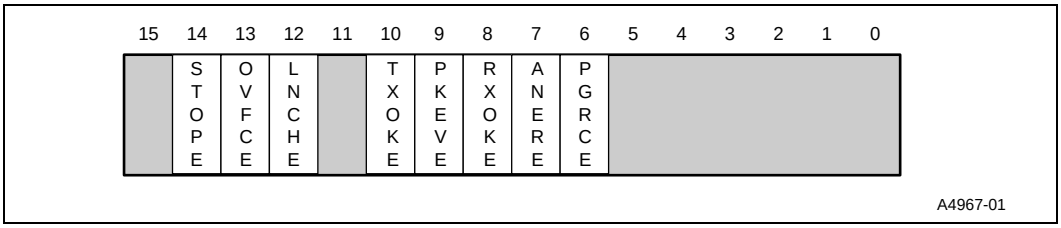
Bit Name	Bit #	Bit Description
Access Rules		
Register access		R
Value after reset		0000H

3.2.2.2 Interrupt Enable Register

Mnemonic: INT_EN

Address: 02H – 03H

Each bit in this register, when set to 1, enables the generation of an interrupt when the corresponding event occurs. The event causing the interrupt will be reported in the interrupt status register (INT_STT).



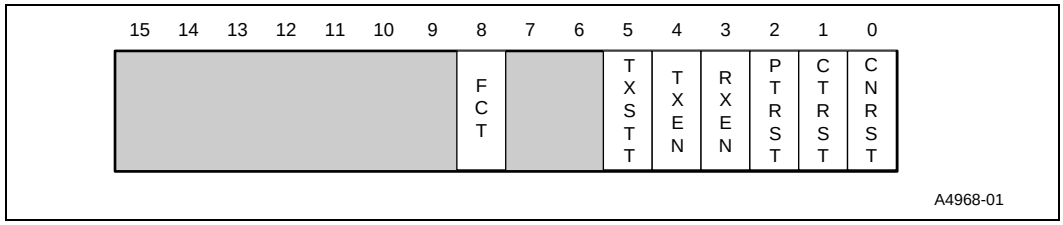
Bit Name	Bit #	Bit Description
—	15	RESERVED
STOPE	14	Port stop interrupt enable.
OVFCE	13	Counter overflow interrupt enable.
LNCHE	12	Link change interrupt enable.
—	11	RESERVED
TXOKE	10	Transmit OK interrupt enable.
PKEVE	9	Packet event interrupt enable.
RXOKE	8	Receive OK interrupt enable.
ANERE	7	Auto-Negotiation error interrupt enable.
PGRCE	6	Page received interrupt enable.
—	5:0	RESERVED
Access Rules		
Register access		R/W
Value after reset		0000H

3.2.2.3 Port Control Register

Mnemonic: PORT_CTR

Address: 04H – 05H

The port control register handles all the control bits of the port.



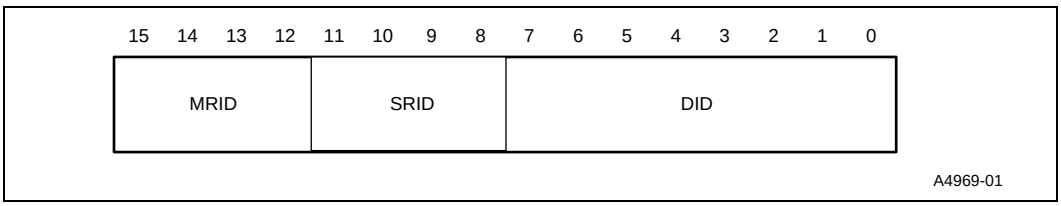
Bit Name	Bit #	Bit Description
—	15:9	RESERVED
FCT	8	**Flow-control packet trigger.** When set, initiates a flow-control packet transmission to the remote node, as defined in the 802.3x IEEE Standard. The pause time field in the transmitted packet will be copied from the PAUSE_TIME register (see Section 3.2.3.6).
—	7:6	RESERVED
TXSTT	5	**Transmit restart.** When set, the chip restarts the transmission process after stopping due to a transmit error. The TXSTT is a trigger bit (does not require reset before setting).
TXEN	4	**Transmit enable.** When this bit is set, the port enters the transmit working mode. When reset, the port completes transmission of the packet currently processed, and then stops. Stop state is reported in the STOP bit located in the interrupt status register (INT_STT).
RXEN	3	**Receive enable.** When this bit is set, the port enters the receive working mode. When reset, the port completes reception of the packet currently processed, and then stops. Stop state is reported in the STOP bit located in the interrupt status register (INT_STT).
PTRST	2	**Port reset.** When set, this bit causes the transmit and receive logic to reset. setting this bit will not reset the control registers.
CTRST	1	**Control reset.** When set, this bit resets all the registers, except PORT_CTR, to their default values. Transmit and receive logic are also reset. This bit is not self clearing, it requires set and then reset.
CNRST	0	**Counter reset.** When set, this bit resets all the network statistic counters. The CNRST is a trigger bit (does not require resetting before setting.)
Access Rules		
Register access		R/W Bit 5 and Bit 8 are trigger bits and are Write only.
Value after reset		0000H

3.2.2.4 Identification and Revision Register

Mnemonic: ID_REV

Address: 06H – 07H

The identification and revision register is valid only in port 0.



Bit Name	Bit #	Bit Description
MRID	15:12	Main revision ID. This number is incremented for subsequent IXF1002 revisions.
SRID	11:8	Sub revision ID. This number is incremented for subsequent IXF1002 steps within the current revision.
DID	7:0	Device ID.
Access Rules		
Register access		R
Value after reset		-EC = 1105H -ED = 2005H

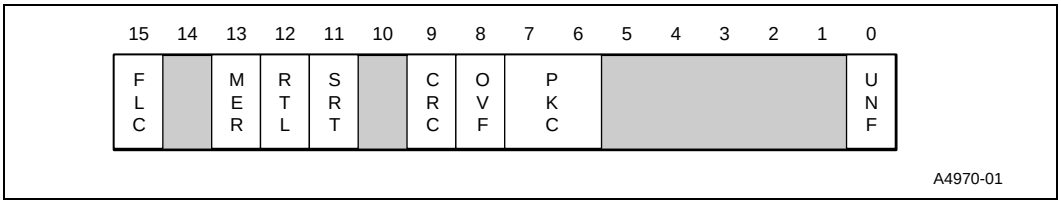
3.2.2.5 Transmit and Receive Status Register

Mnemonic: TX_RX_STT

Address: 08H – 09H

This register reports events that have occurred during packet reception and transmission. All bits, except PKC bit, are reset upon reading this register. The UNF bit is set only if packet transmission is programmed to be stopped following FIFO underflow in the transmit and receive error mode register (TX_RX_ERR<UNFS>).

The receive error bits (TX_RX_STT<15:8>) in this register, are set only if the receive logic is programmed to pass packets with the corresponding event in the transmit and receive error mode register (TX_RX_ERR<15:8>). If a receive packet with multiple errors is to be passed and not all the corresponding bits in the transmit and receive error mode register (TX_RX_ERR) are set, none of the bits in this register are set. The receive status is also appended to the end of the packet in the receive FIFO in packet status append mode (see Section 4.3.1.1).



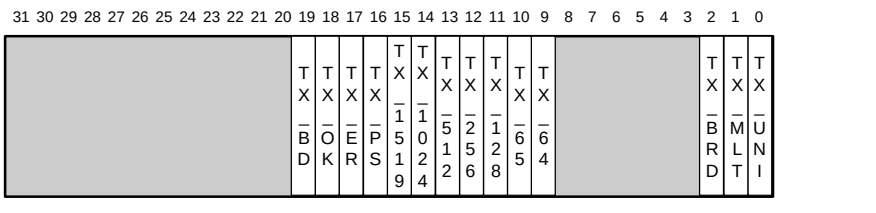
Bit Name	Bit #	Bit Description
FLC	15	**Flow-control packet.** Indicates that a flow-control packet was received.
—	14	RESERVED
MER	13	**GMII error.** Indicates either that a symbol error was detected in the GPCS mode or that an GMII error signal was asserted in the GMII mode during packet reception.
RTL	12	**Too long packet.** Indicates that a packet longer than the maximum allowable packet size specified in the PKT_MAX_SIZE register, has been received.
SRT	11	**Short packet.** Indicates that a packet shorter than 64 bytes has been received.
—	10	RESERVED
CRC	9	**CRC error.** Indicates that a packet was received with a CRC error.
OVF	8	**FIFO overflow.** Indicates that there was not enough space available in the receive FIFO during packet reception.
PKC	7:6	**Packet count.** Indicates the number of packets currently stored in the transmit FIFO. The packet count is incremented while loading the first byte of a packet and decremented following transmission of a packet. The maximum number of packets that can be in the transmit FIFO is two.
—	5:1	RESERVED
UNF	0	**FIFO underflow.** Indicates that data was not available in the transmit FIFO during packet transmission.
Access Rules		
Register access		R
Value after reset		0000H

3.2.2.6 Transmit Counter Overflow Status Register

Mnemonic: TX_OV_STT

Address: 0AH – 0DH

The transmit counter overflow status register reports overflow events of each transmit counter. When a counter reaches its highest possible value, it will continue to count from zero, and the corresponding status bit will be set. Reading this register will reset all the bits, and will clear the interrupt if it was activated.



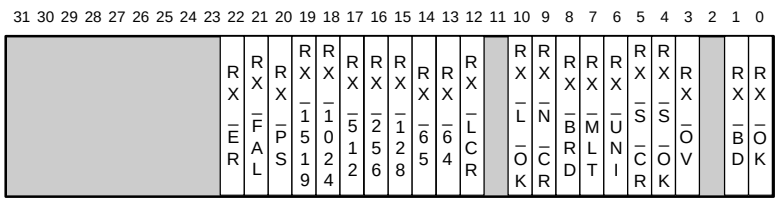
Bit Name	Bit #	Bit Description
—	31:20	RESERVED
TX_BD	19	TX_OCT_BAD_CNT counter overflow.
TX_OK	18	TX_OCT_OK_CNT counter overflow.
TX_ER	17	TX_ERR_CNT counter overflow.
TX_PS	16	TX_PAUSE_CNT counter overflow.
TX_1519	15	TX_PKT_1519_CNT counter overflow.
TX_1024	14	TX_PKT_1024_CNT counter overflow.
TX_512	13	TX_PKT_512_CNT counter overflow.
TX_256	12	TX_PKT_256_CNT counter overflow.
TX_128	11	TX_PKT_128_CNT counter overflow.
TX_65	10	TX_PKT_65_CNT counter overflow.
TX_64	9	TX_PKT_64_CNT counter overflow.
—	8:3	RESERVED
TX_BRD	2	TX_BRD_OK_CNT counter overflow.
TX_MLT	1	TX_MLT_OK_CNT counter overflow.
TX_UNI	0	TX_UNI_OK_CNT counter overflow.
Access Rules		
Register access		R
Value after reset		0000H

3.2.2.7 Receive Counter Overflow Status Register

Mnemonic: RX_OV_STT

Address: 0EH – 11H

The receive counter overflow status register reports overflow events of each receive counter. When a counter reaches its highest possible value, it will continue to count from zero, and the corresponding status bit will be set. Reading this register will reset all the bits, and will clear the interrupt if it was activated.



Bit Name	Bit #	Bit Description
—	31:23	RESERVED
RX_ER	22	RX_GPCS_ERR_CNT counter overflow.
RX_FAL	21	RX_FALS_CRS_CNT counter overflow.
RX_PS	20	RX_PAUSE_CNT counter overflow.
RX_1519	19	RX_PKT_1519_CNT counter overflow.
RX_1024	18	RX_PKT_1024_CNT counter overflow.
RX_512	17	RX_PKT_512_CNT counter overflow.
RX_256	16	RX_PKT_256_CNT counter overflow.
RX_128	15	RX_PKT_128_CNT counter overflow.
RX_65	14	RX_PKT_65_CNT counter overflow.
RX_64	13	RX_PKT_64_CNT counter overflow.
RX_L_CR	12	RX_LONG_CRC_CNT counter overflow.
—	11	RESERVED
RX_L_OK	10	RX_LONG_OK_CNT counter overflow.
RX_N_CR	9	RX_NORM_CRC_CNT counter overflow.
RX_BRD	8	RX_BRD_OK_CNT counter overflow.
RX_MLT	7	RX_MLT_OK_CN counter overflow.
RX_UNI	6	RX_UNI_OK_CNT counter overflow.
RX_S_CR	5	RX_SHORT_CRC_CNT counter overflow.
RX_S_OK	4	RX_SHORT_OK_CNT counter overflow.
RX_OV	3	RX_OVF_CNT counter overflow.
—	2	RESERVED
RX_BD	1	RX_OCT_BAD_CNT counter overflow.
RX_OK	0	RX_OCT_OK_CNT counter overflow.
Access Rules		
Register access		R
Value after reset		0000H

3.2.3 Configuration Registers

The following sections describe the individual configuration registers.

3.2.3.1 Transmit and Receive Error Mode Register

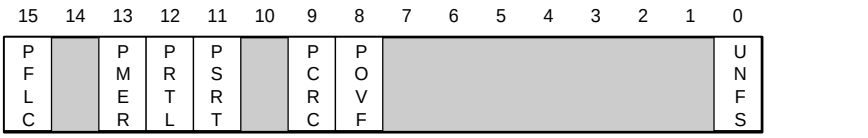
Mnemonic: TX_RX_ERR

Address: 20H – 21H

This register defines the actions to be performed following a transmit or receive error.

When a receive packet with a specific event is programmed to be passed, the corresponding packets are not discarded and are transferred as regular packets. The transmit and receive events are reported in the transmit and receive status register (TX_RX_STT) and can generate an interrupt according to the interrupt enable register (INT_EN).

If a specific event is not programmed to enable reception of a packet, the corresponding packets are discarded from the receive FIFO. Failure will be reported onto the rxfail signal if the packet has already started to be transferred onto the IX Bus. If a packet with multiple errors is to be passed, all corresponding bits must be set.



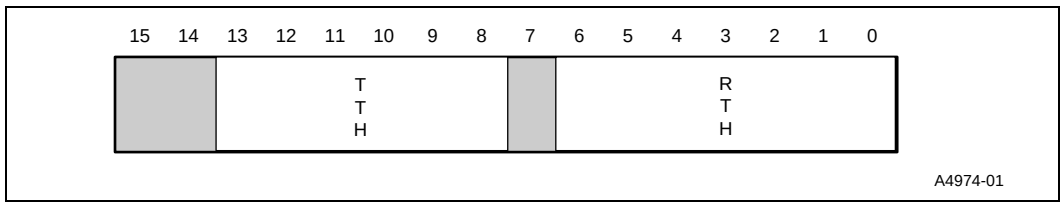
Bit Name	Bit #	Bit Description
PFLC	15	Pass flow-control packets.
—	14	RESERVED
PMER	13	Pass packets with GMII error.
PRTL	12	Pass too long packets.
PSRT	11	Pass short packets.
—	10	RESERVED
PCRC	9	Pass CRC error packets.
POVF	8	Pass FIFO overflow.
—	7:1	RESERVED
UNFS	0	**Stop transmission after FIFO underflow.** When set, the transmit FIFO is flushed and transmission stops if an underflow occurs. When transmission is stopped after FIFO underflow, flow-control packets can still be transmitted. A value of 1 in this bit will be followed by activation of PKEV interrupt if it is enabled (see Section 3.2.2.1), and not by the port stop interrupt. When reset, if an underflow occurs the packet will be flushed from the transmit FIFO, and the following packet will be transmitted.
Access Rules		
Register access		R/W
Value after reset		0000H

3.2.3.2 FIFO Threshold Register

Mnemonic: FFO_TSHD

Address: 22H – 23H

The FIFO register handles the transmit and receive FIFO threshold.



Bit Name	Bit #	Bit Description
—	15:14	RESERVED
TTH	13:8	This field defines the minimum amount of free space required in the transmit FIFO in order to assert the txrdy signal. The effective threshold in bytes is equal to 16 × (TTH + 1).
—	7	RESERVED
RTH	6:0	This field defines the minimum amount of data required in the receive FIFO in order to assert the rxrdy signal. The effective threshold in bytes is equal to 16 × (RTH + 1).
Access Rules		
Register access		R/W
Value after reset		0303H

3.2.3.3 Port Working Mode Register

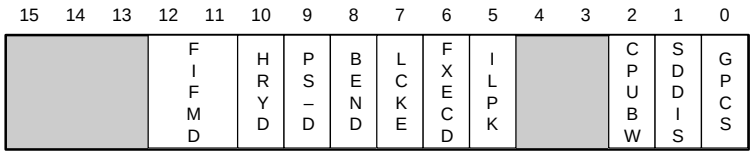
Mnemonic: PORT_MODE

Address: 24H – 25H

The port mode register controls the CPU bus, IX Bus, and serial interface modes of work.

Note: Details on Multi-Packet Mode (available with the GCIXF1002ED) are contained in Appendix C.4.

Note: Bits 12, 11, 2, and 0 must have the same value in both ports.



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Bit Name	Bit #	Bit Description
—	15:13	RESERVED
FIFMD	12:11	**IX Bus mode:** This field sets the IX Bus mode. Both ports of the IXF1002 must be operating in the same IX Bus mode. The table below shows the IX Bus mode according to bits 12 and 11. **Bit 12** **Bit 11** **Mode** 0 0 Narrow-32 bit mode 0 1 Full-64 bit mode 1 0 Split mode 1 1 Reserved In the full-64 bit mode, the 64 bits fdat<63:0> are used for either transmitting or receiving data. In the split mode, the 32 lower bits fdat<31:0> are used for receiving packets from the receive FIFO and the 32 higher bits fdat<63:32> are used for transmitting packets to the transmit FIFO. In the narrow mode, the lower 32 bits fdat<31:1> are used for either transmitting or receiving packets.
HRYD	10	**Header ready disable.** When set, the **rxrdy** signal will not be asserted when a packet header is in FIFO, but only according to FIFO threshold values.
PS_D	9	**Packet status disable.** When set, the packet status will not be appended to received packets that are transferred onto the IX Bus. When reset, The packet status is appended to any packet completely transferred onto the IX Bus, and is driven onto the IX Bus in the access following the last byte transfer (see 4.3.1.1).
BEND	8	**Big or little endian mode.** Defines the byte ordering mode on the IX Bus. When set, the port uses the big endian mode. When reset, the little endian mode is used.

Bit Name	Bit #	Bit Description
LCKE	7	**Enable activation of lock to reference signal.** When set, the lckref_{i} signal will be asserted to the PHY when there is no activity (no signal detected) on the line. Used only in GPCS mode.
FXECD	6	**Fix enable comma detect signal.** When set, the encdet_{i} signal to the PHY will be continuously asserted. When cleared, the encdet_{i} signal will be asserted only during loss of synchronization. Used only in GPCS mode.
ILPK	5	**Internal loopback mode.** When set, the port is disconnected from the line and all the transmitted packets are sent back to the receive side. Packets are not transmitted onto the line and packets received from the line are rejected.
—	4:3	RESERVED
CPUBW	2	**CPU data bus width.** When asserted, bus width is 16, all **cdat<15:0>** bits are in use. When deasserted, bus width is 8, indicating that the 8 low bits **cdat<7:0>** are in use.
SDDIS	1	**Signal detect disable.** Setting this bit will cause IXF1002 to consider the value of the sd{i} input signal as high, regardless to the actual value on the pin. Used only in GPCS mode.
GPCS	0	**GPCS port mode.** This bit defines the GMII/GPCS port mode. If a GPCS PHY device is connected, this bit must be set. If a GMII PHY device is connected, this bit must be reset.
Access Rules		
Register access		R/W
Value after reset		0000H

3.2.3.4 Transmit and Receive Parameters Register

Mnemonic: TX_RX_PARAM

Address: 26H – 27H

The transmit and receive parameters register handles the control of the serial interface.

Bit Name	Bit #	Bit Description
CRCR	15	**CRC remove.** When set, the last four bytes of the received packet will not be transferred onto the IX Bus. Packets shorter than 4 bytes will be discarded.
HRPL	14	**Header replay.** When set, packet header is transferred twice onto the IX Bus.
HDRS	13:8	**Header size.** Header size is used for the header replay function and for rxrdy signal assertion (even if the header replay function is disabled). The header size is calculated in bytes as 4 × HDRS (HDRS > 4).
—	7:6	RESERVED
ADFC	5	**Additional flow control.** When this bit is asserted, the IXF1002 will send an additional flow-control packet if a flow-control packet was sent upon assertion of the flct_{i} signal, and while this signal was asserted, the link partner's pause time period was about to end. This will cause the link partner to receive the additional flow-control packet before its pause time counting ends. **NOTE:** This feature is operative only if XOND bit is equal to 0.
SPM	4	**Single packet mode.** When set, a packet is loaded in the transmit FIFO only after the previous packet was transmitted onto the serial line. When not set, the transmit FIFO can contain a maximum of two packets.
XOND	3	**XON disable.** When set, a flow-control packet with pause time equal to zero, will not be sent upon flct_{i} signal deassertion.
RFLCE	2	**Receive flow-control mode enable.** When set, transmission is paused upon receiving flow-control packets. **NOTE:** This bit is used only in GMII mode and in GPCS mode when Auto-Negotiation is disabled (GMII_CTL<ANENBL=0>). In GPCS mode when Auto-Negotiation is enabled, the desired mode should be written in the AN_ADV<PAUSE> bit, and the final mode after the Auto-Negotiation will be reported in the GPCS_STT<RFC> bit.
CRCD	1	**CRC appending disable.** When set, packets are transmitted without padding or CRC appending to the end of the packet. This field is ignored if the txasis signal is asserted during the start of packet loading. **NOTE:** In case of VLAN tag append, strip or replace, the frame check sequence (FCS) field will be calculated by the IXF1002 (see 4.2.2.1).
PADD	0	**Padding appending disable.** When set, short packets are transmitted without the addition of bytes complementing their sizes to 64 bytes. When the CRCD bit is set, this bit is ignored. This field is ignored if the **txasis** signal is asserted during the start of packet loading.

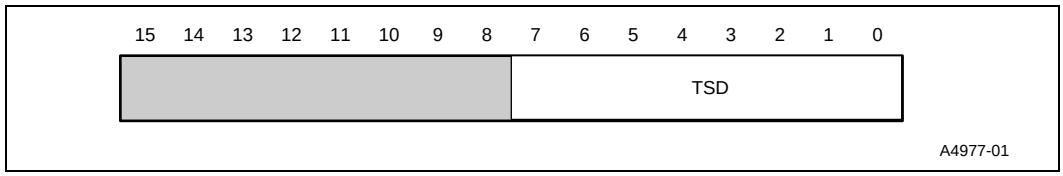
Bit Name	Bit #	Bit Description
Access Rules		
Register access		R/W
Value after reset		1004H

3.2.3.5 Transmit Threshold Register

Mnemonic: TX_TSHD

Address: 28H – 29H

The transmission threshold register handles the packet transmission threshold.



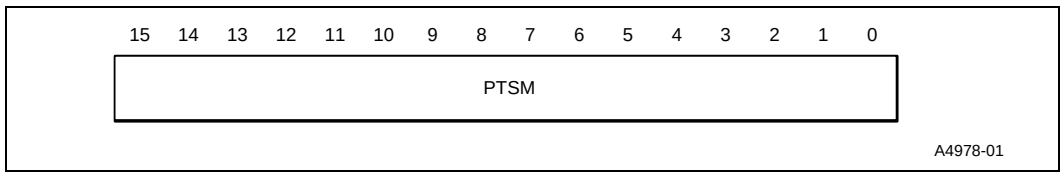
Bit Name	Bit #	Bit Description
—	15:8	RESERVED
TSD	7:0	**Packet transmission threshold.** Packet transmission starts when the amount of data in the transmit FIFO is larger than or equal to the threshold, or the entire packet enters onto the FIFO. The effective threshold in bytes is equal to 8 × TSD + 4. If the sum of the effective serial threshold and the effective parallel threshold bring the system to a deadlock, the transmission can start before threshold is reached to prevent deadlock. (TSD > 1)
Access Rules		
Register access		R/W
Value after reset		0003H

3.2.3.6 Transmit Flow-Control Pause Time Register

Mnemonic: PAUSE_TIME

Address: 2AH – 2BH

The transmit flow-control pause time register handles the time field used in the transmitted flow-control packets.



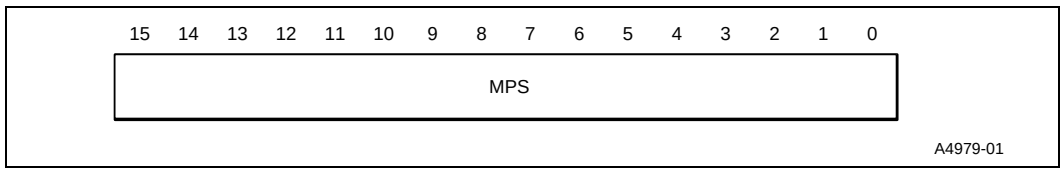
Bit Name	Bit #	Bit Description
PSTM	15:0	Indicates the number of units of 512 bit time (512 ns), during which the remote node cannot send packets. This field is inserted into the transmitted flow-control packets.
Access Rules		
Register access		R/W
Value after reset		0000H

3.2.3.7 Maximum Packet Size Register

Mnemonic: PKT_MAX_SIZE

Address: 2CH – 2DH

This register controls the maximum allowed received packet size.



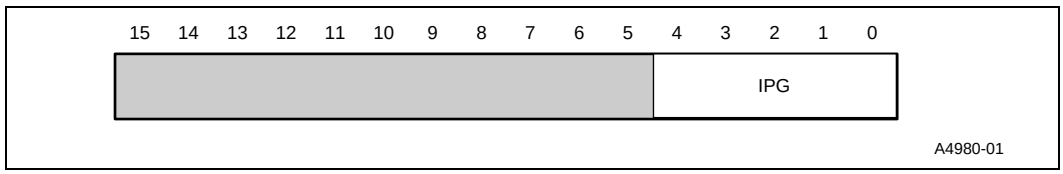
Bit Name	Bit #	Bit Description
MPS	15:0	Packets received with a longer size are treated as too long packets.
Access Rules		
Register access		R/W
Value after reset		05EEH (1518 decimal)

3.2.3.8 Inter Packet Gap Value Register

Mnemonic: IPG_VAL

Address: 2EH – 2FH

This register controls the inter packet gap value between transmitted packets.



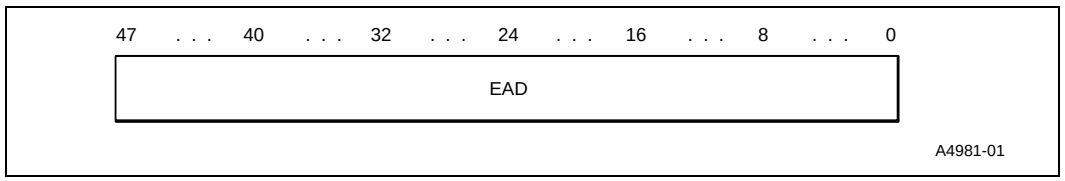
Bit Name	Bit #	Bit Description
—	15:5	RESERVED
IPG	4:0	Interpacket gap value in units of 8 bit time. This field must get a minimum value of 6H (48-bit time).
Access Rules		
Register access		R/W
Value after reset		000CH (96-bit time)

3.2.3.9 MAC Address Registers

Mnemonic: MAC_ADD

Address: 30H – 35H

The MAC address register contains the Ethernet physical address of the port. This address is inserted into transmitted flow-control packets in the source address field.



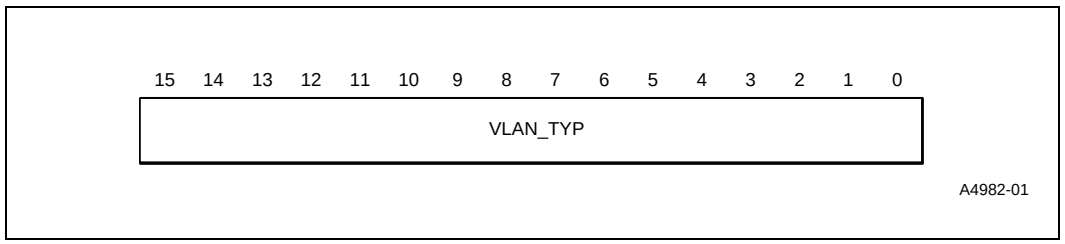
Bit Name	Bit #	Bit Description
EAD	47:0	**Port Ethernet address.** Bit 47 is the most significant bit, and bit 0 is the least significant bit and is the first bit of the MAC serial bit stream.
Access Rules		
Register access		R/W
Value after reset		0000H

3.2.3.10 VLAN Tag Length/Type Register

Mnemonic: VLAN_TAG

Address: 36H – 37H

The VLAN length/type register is used to define the VLAN tag length/type field.



Bit Name	Bit #	Bit Description
VLAN_T YP	15:0	**VLAN type** This field defines length/type field of the VLAN tag when inserted into transmitted frames.

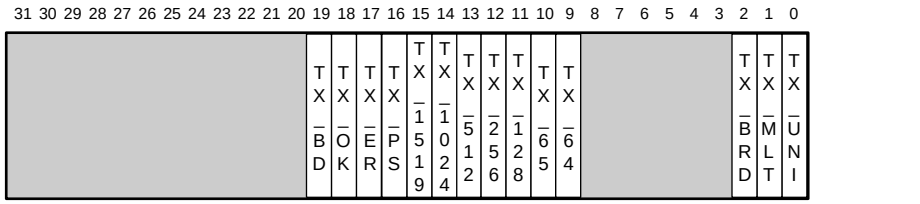
Bit Name	Bit #	Bit Description
Access Rules		
Register access		R/W
Value after reset		8100H

3.2.3.11 Transmit Counter Overflow Mask Register

Mnemonic: TX_OV_MSK

Address: 38H – 3BH

The transmit counter overflow mask register enables masking of specific transmit counters overflow interrupt. Masking a counter does not influence the setting of the counter overflow status bit in TX_OV_STT.



Bit Name	Bit #	Bit Description
—	31:20	RESERVED
TX_BD	19	Mask TX_OCT_BAD_CNT counter overflow.
TX_OK	18	Mask TX_OCT_OK_CNT counter overflow.
TX_ER	17	Mask TX_ERR_CNT counter overflow.
TX_PS	16	Mask TX_PAUSE_CNT counter overflow.
TX_1519	15	Mask TX_PKT_1519_CNT counter overflow.
TX_1024	14	Mask TX_PKT_1024_CNT counter overflow.
TX_512	13	Mask TX_PKT_512_CNT counter overflow.
TX_256	12	Mask TX_PKT_256_CNT counter overflow.
TX_128	11	Mask TX_PKT_128_CNT counter overflow.
TX_65	10	Mask TX_PKT_65_CNT counter overflow.
TX_64	9	Mask TX_PKT_64_CNT counter overflow.
—	8:3	RESERVED
TX_BRD	2	Mask TX_BRD_OK_CNT counter overflow.
TX_MLT	1	Mask TX_MLT_OK_CNT counter overflow.
TX_UNI	0	Mask TX_UNI_OK_CNT counter overflow.

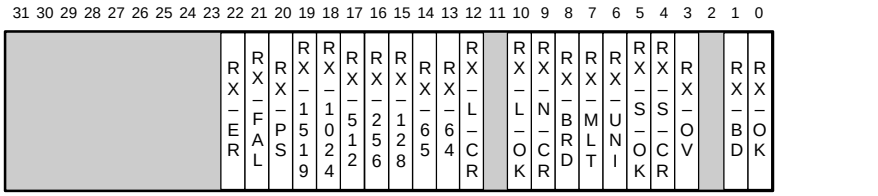
Bit Name	Bit #	Bit Description
Access Rules		
Register access		R/W
Value after reset		0000H

3.2.3.12 Receive Counter Overflow Mask Register

Mnemonic: RX_OV_MSK

Address: 3CH – 3FH

The receive counter overflow mask register enables masking of specific receive counters overflow interrupt. Masking a counter does not influence the setting of the counter overflow status bit in RX_OV_STT



Bit Name	Bit #	Bit Description
—	31:23	RESERVED
RX_ER	22	Mask RX_GPCS_ERR_CNT counter overflow.
RX_FAL	21	Mask RX_FALS_CRS_CNT counter overflow.
RX_PS	20	Mask RX_PAUSE_CNT counter overflow.
RX_1519	19	Mask RX_PKT_1519_CNT counter overflow.
RX_1024	18	Mask RX_PKT_1024_CNT counter overflow.
RX_512	17	Mask RX_PKT_512_CNT counter overflow.
RX_256	16	Mask RX_PKT_256_CNT counter overflow.
RX_128	15	Mask RX_PKT_128_CNT counter overflow.
RX_65	14	Mask RX_PKT_65_CNT counter overflow.
RX_64	13	Mask RX_PKT_64_CNT counter overflow.
RX_L_CR	12	Mask RX_LONG_CRC_CNT counter overflow.
—	11	RESERVED
RX_L_OK	10	Mask RX_LONG_OK_CNT counter overflow.
RX_N_CR	9	Mask RX_NORM_CRC_CNT counter overflow.
RX_BRD	8	Mask RX_BRD_OK_CNT counter overflow.
RX_MLT	7	Mask RX_MLT_OK_CN counter overflow.
RX_UNI	6	Mask RX_UNI_OK_CNT counter overflow.
RX_S_CR	5	Mask RX_SHORT_CRC_CNT counter overflow.
RX_S_OK	4	Mask RX_SHORT_OK_CNT counter overflow.
RX_OV	3	Mask RX_OVF_CNT counter overflow.
—	2	RESERVED
RX_BD	1	Mask RX_OCT_BAD_CNT counter overflow.
RX_OK	0	Mask RX_OCT_OK_CNT counter overflow.

Bit Name	Bit #	Bit Description
Access Rules		
Register access		R/W
Value after reset		0000H

3.2.4 GMII Management Access Registers

This set of registers is intended to simplify access to the GMII management registers in the PHY, while working in GMII mode.

In order to access a GMII management register in the PHY, an access command should be written in the GMII management access register (GMII_MNG_ACC). The IXF1002 carries out the command and accesses the PHY through the mdc and mdio pins.

In GPCS mode, the set of GMII management registers is provided on the IXF1002 in addresses 50H – 71GH, and these addresses should be accessed directly.

Note: These registers are valid only in port 0.

3.2.4.1 GMII Management Access Register

Mnemonic: GMII_MNG_ACC

Address: 4AH – 4BH (only in port 0)

The GMII Management Access register controls the mdc and mdio I/O pins. Two modes of access to the PHY are available

- Direct access mode: In this mode each of the mdc and mdio I/O pins are set to be input or output, and can be read or written through this register.
- Automatic access mode: This mode is used to access the GMII management register set in the PHY. The address of the desired PHY and register, and the mode of access (R/W), are defined in this register. In this mode the IXF1002 will transmit and receive frames to/from the PHY through the mdc and mdio pins, as defined in the 802.3u standard.

The automatic access will begin after writing a value of 1 to the AMAM bit, if the CPU is in the 16-bit mode, or after a write access to the high byte of this register if the value of the AMAM bit is 1 and the CPU is in 8-bit mode.

Use bits MDC/MDIO as GPIO by writing to register GMII_MNG_ACC.

They are used in the direct access mode as follows:

AMA (bit 0) = 0

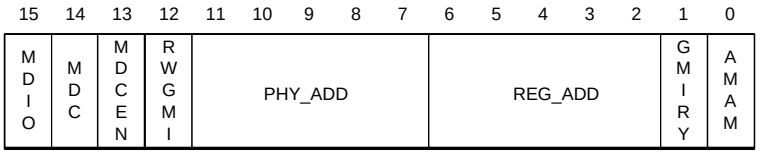
MDIO (bit 15) is used to drive the mdio pin (or read from it)

MDC (bit 14) is used to drive the mdio pin

MDCEN (bit 13) enables the mdc pin as an output

RWGMI (bit 12) enables the mdio pin as an output

You can write to the register and drive these pins, and read the pin’s value by reading the register (with enable bits reset).



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Bit Name	Bit #	Bit Description
MDIO	15	**GMII data IO** In direct access mode (AMAM=0): During mdio write access (RWGMI=1), the value written to this bit is driven onto the mdio signal. During mdio read access (RWGMI=0), the mdio signal value is latched into this bit. In automatic access mode (AMAM=1): This bit is not valid.
MDC	14	**MDC clock value** In direct access mode (AMAM=0): During mdc write access (MDCEN=1), the value written to this bit is driven onto the mdc signal. When access to the PHY is done using this bit, each new value must remain stable for at least 200 ns. During mdc read access (MDCEN=0), the mdc signal value is latched into this bit. In automatic access mode (AMAM=1): This bit is not valid
MDCEN	13	**Enable MDC output** In direct access mode (AMAM=0): When set enables mdc output. In automatic access mode (AMAM=1): This bit is not valid.
RWGMI	12	**Read/write GMII management registers.** In direct access mode (AMAM=0): When set enables mdio output. In automatic access mode (AMAM=1): Set this bit for writing the data from the GMII_MNG_DAT register into the GMII management desired register. Reset this bit for reading the GMII management desired register into the GMII_MNG_DAT register.
PHY_ADD	11:7	**GMII PHY address.** The address of the desired PHY. Bit 11 is the most significant bit and is the first PHY address bit to be transmitted and received.
REG_ADD	6:2	**GMII register address.** The address of the desired register. Bit 6 is the most significant bit and is the first register address bit to be transmitted and received.

Bit Name	Bit #	Bit Description
GMIRY	1	**GMII management access registers are ready.** This bit indicates whether the access to the GMII management registers had been completed. During the access process, the value of this bit will be 0. The bit will be set at the end of the process. Writing to the GMII management access registers while this bit is cleared will be ignored, although the crdy_l signal will be asserted.
AMAM	0	**Automatic mdio access mode** Setting this bit will begin the Automatic access. **Note:** If the cpu bus is in 8-bit mode the automatic access will occur after a write access to the high byte of the register.
Access Rules		
Register access		During GMII automatic access (GMIRY = 0) R, otherwise R/W.
Value after reset		0003H

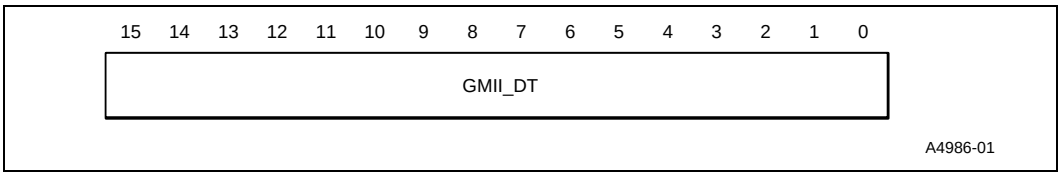
3.2.4.2 GMII Management Data Register

Mnemonic: GMII_MNG_DAT

Address: 4CH – 4DH (only in port 0)

In read mode, this register will get the value of the desired GMII management register. In write mode, the desired management register will get the value of this register.

Note: When CPU bus is in 8 bit mode, write access to this register must be done to both addresses, starting at the low address.



Bit Name	Bit #	Bit Description
GMII_DT	15:0	**GMII data.** Bit 15 is the most significant bit, corresponding to bit 15 of the accessed register. Bit 0 is the least significant bit.
Access Rules		
Register access		Bits 12:2 , during GMII automatic access (GMII_MNG_ACC<GMIRY> = 0) R, otherwise R/W Bit 1 is always read only.
Value after reset		0000H

3.2.5 GMII Management Register Set

The following sections describe the individual GMII management register set as defined in the IEEE 802.3z standard.

Any bit in these registers that has a fixed value is not writable.

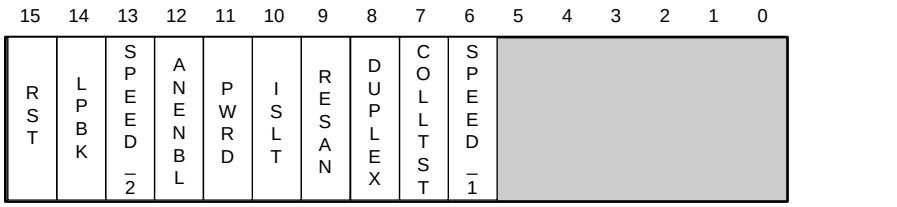
Note: These registers are accessible only in GPCS mode.

3.2.5.1 GMII Control Register

Mnemonic: GMII_CTL

Address: 50H – 51H

The control register provides the mechanism to enable or disable Auto-Negotiation, restart Auto-Negotiation, and allow for manual configuration when Auto-Negotiation is disabled.



Bit Name	Bit #	Bit Description
RST	15	**Reset.** When set, causes reset to the GPCS logic and to the GMII management registers. When reset, indicates normal operation. This bit is self clearing. The value of this bit remains at 1, until the reset process is completed.
LPBK	14	**External loopback.** When set, enables external loopback mode, and causes assertion of ewrap_{i} signal. When reset, disables external loopback mode, and causes deassertion of ewrap_{i} signal.
SPEED_2	13	**Speed selection.** This bit is fixed at the value of 0 and the value of bit 6 is fixed to 1, determining a speed selection of 1000 Mb/s.
ANENBL	12	**Auto-Negotiation enable.** When set, Auto-Negotiation process is enabled. When reset, Auto-Negotiation process is disabled.
PWRD	11	**Power down.** This bit is fixed at the value of 0. The IXF1002 GPCS does not support the power down function.
ISLT	10	**Isolate.** This bit is fixed at the value of 0. The IXF1002 GPCS does not support the isolate function.

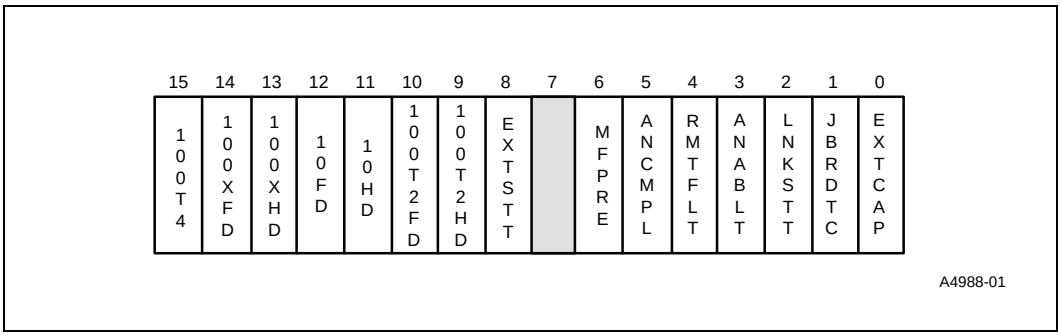
Bit Name	Bit #	Bit Description
RESAN	9	**Restart Auto-Negotiation.** When set, restarts Auto-Negotiation process. When reset, indicates normal operation. This bit is self clearing. The value of this bit will change back to 0 when the Auto-Negotiation process is initiated. If Auto-Negotiation is disabled (ANENBL=0), this bit should be at a value of 0.
DUPLEX	8	**Duplex mode.** This bit is fixed at the value of 1. The IXF1002 is operating only in the full-duplex mode.
COLLTST	7	**Collision test.** This bit is fixed at the value of 0. The IXF1002 GPCS does not support the collision signal test.
SPEED_1	6	**Speed selection.** This bit is fixed at the value of 1 and the value of bit 13 is fixed at 0, determining a speed selection of 1000 Mb/s
—	5:0	RESERVED.
Access Rules		
Register access		Bits 9, 12, 14, 15 R/W, bits 6, 7, 8, 10, 11, 13 R.
Value after reset		1140H

3.2.5.2 GMII Status Register

Mnemonic: GMII_STT

Address: 52H – 53H

The GMII status register includes information about all modes of operations supported by the local device and the status of Auto-Negotiation.



Bit Name	Bit #	Bit Description
100T4	15	**100BASE-T4 ability.** This bit is fixed at the value of 0.
100XFD	14	**100BASE-X full-duplex ability.** This bit is fixed at the value of 0.
100XHD	13	**100BASE-X half-duplex ability.** This bit is fixed at the value of 0.

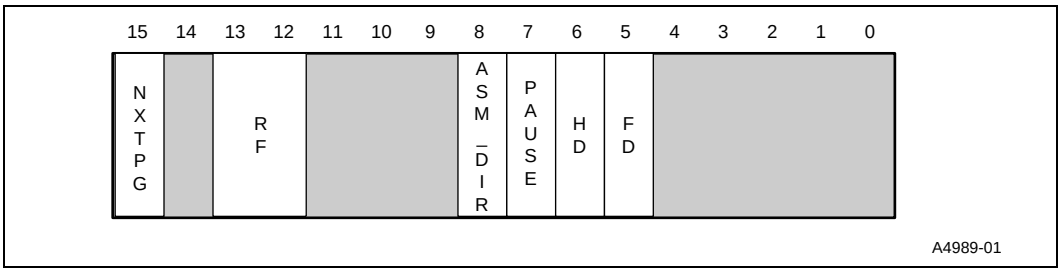
Bit Name	Bit #	Bit Description
10FD	12	**10 Mb/s full-duplex ability.** This bit is fixed at the value of 0.
10HD	11	**10 Mb/s half-duplex ability.** This bit is fixed at the value of 0.
100T2FD	10	**100BASE-T2 full-duplex ability.** This bit is fixed at the value of 0.
100T2HD	9	**100BASE-T2 half-duplex ability.** This bit is fixed at the value of 0.
EXTSTT	8	**Extended status.** This bit is fixed at the value of 1, indicating additional status information in the extended status register (GMII_EXT_STT).
—	7	RESERVED
MFPRE	6	**MF preamble suppression.** This bit is fixed at the value of 0. The IXF1002 registers cannot be accessed through the mdio pin.
ANCMPL	5	**Auto-Negotiation complete.** A value of 1 indicates that Auto-Negotiation process is completed. A value of 0 indicates that Auto-Negotiation process is not completed.
RMTFLT	4	**Remote fault.** A value of 1 indicates that a remote fault condition was detected in the link partner's base page. A value of 0 indicates that a remote fault condition was not detected.
ANABLT	3	**Auto-negotiation ability.** This bit is fixed at the value of 1, indicating that the GPCS is able to perform Auto-Negotiation.
LNKSTT	2	**Link status.** A value of 1 indicates that the link is up. A value of 0 indicates that the link is down. Link up is defined as a status in which the synchronization process and the Auto-Negotiation process were completed and the device is ready to transmit or receive data.
JBRDTC	1	**Jabber detect.** This bit is fixed at the value of 0. The IXF1002 GPCS does not support jabber detection.
EXTCAP	0	**Extended capability.** This bit is fixed at the value of 0, indicating basic register set capabilities only.
Access Rules		
Register access		R
Value after reset		0108H

3.2.5.3 AN Advertisement Register

Mnemonic: AN_ADV

Address: 58H – 59H

The AN advertisement register contains the advertised ability of the local device. If another value than the default value is written into this register, then Auto-Negotiation should be restarted by setting bit GMII_CTL<RESAN>. In GPCS mode when Auto-Negotiation is not disabled, the ASM_DIR and PAUSE bits contain the desired flow-control mode of operation. The actual flow-control mode will be figured during the Auto-Negotiation process and will be reported in the GPCS status register GPCS_STT.



Bit Name	Bit #	Bit Description
NXTPG	15	**Next page.** When set, indicates a request for next page exchange.
—	14	RESERVED
RF	13:12	**Remote fault.** The remote fault bits are used to notify the link partner about a fault that had occurred. These bits are cleared after successful page exchanging. The table below specifies the remote fault encoding. **<12> <13> Description** 0 0 No error, link OK 0 1 Off line 1 0 Link failure 1 1 Auto-Negotiation error
—	11:9	RESERVED
ASM_DIR	8	**Asymmetric PAUSE connection is desired.** When set, results in independent enabling/disabling of the flow-control receive and transmit. When reset, results in symmetric enabling/disabling of the flow-control receive and transmit.
PAUSE	7	**PAUSE function.** When set, indicates that the local device is capable and intends to stop upon reception of flow-control packets as defined in IEEE 802.3x. When reset, indicates that the local device is not capable or does not intend to stop upon reception of a flow-control packet.
HD	6	**half-duplex ability.** This bit is fixed at a value of 0.
FD	5	**full-duplex ability.** This bit is fixed at a value of 1.
—	4:0	RESERVED
Access Rules		
Register access		Bits 7, 8, 12, 13, 15 R/W. Bits 6:0, 9, 10, 11, 14, R.
Value after reset		01A0H

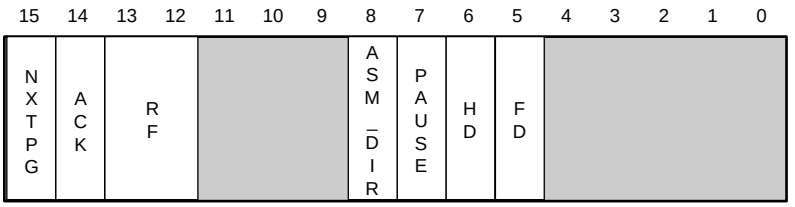
3.2.5.4 AN Link Partner Ability Base Page Register

Mnemonic: AN_PRT_ABL

Address: 5AH – 5BH

The AN link partner ability base page register contains the advertised ability of the partner's device.

This register is updated once every Auto-Negotiation process, at the end of the page exchange state.



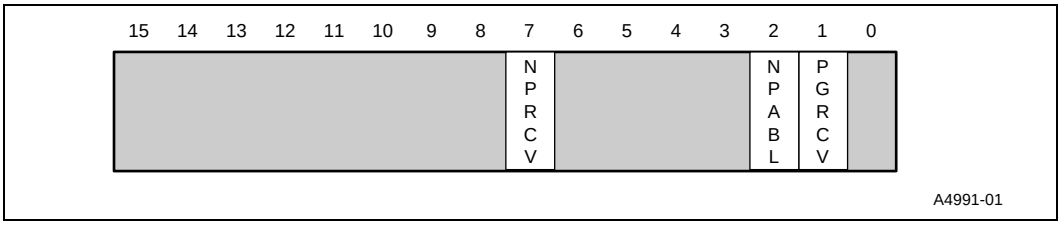
Bit Name	Bit #	Bit Description
NXTPG	15	**Next page.** When set, indicates a request for next page exchange was made by the link partner.
ACK	14	**Acknowledge**. When set, indicates that the link partner has successfully received the base page of the local device.
RF	13:12	**Remote fault.** The remote fault bits are used to notify the local device about a fault that had occurred at the link partner device. The table below specifies the remote fault encoding. <12> <13> **Description** 0 0 No error, link OK 0 1 Off line 1 0 Link failure 1 1 Auto-Negotiation error
	11:9	RESERVED
ASM_DIR	8	**Asymmetric PAUSE connection is desired.** When set, results in independent enabling of the flow-control receive and transmit. When reset, results in symmetric enabling of the flow-control receive and transmit.
PAUSE	7	**Capable of configuring the PAUSE function.** When set, indicates that the link partner's device is capable and intends to stop upon reception of flow-control packets, as defined in IEEE 802.3x.
HD	6	**Half duplex.** When set, indicates link partner's half-duplex capability.
FD	5	**Full duplex.** When set, indicates link partner's full-duplex capability.
—	4:0	RESERVED
Access Rules		
Register access		R
Value after reset		0000H

3.2.5.5 AN Expansion Register

Mnemonic: AN_EXP

Address: 5CH – 5DH

The AN expansion register includes information about page reception and ability of next page function.



Bit Name	Bit #	Bit Description
	15:8	RESERVED
NPRCV	7	**Next page received.** A value of 1 in this bit, indicates that the link partner's current received page is a next page. A value of 0 in this bit indicates that the link partner's current received page is the base page.
	6:3	RESERVED
NPABL	2	**Next page able.** This bit is fixed at the value of 1. The IXF1002 has next page ability.
PGRCV	1	**Page received.** A value of 1 in this bit indicates that the link partner's base or next page has been received. Bit #7 in this register indicates whether the received page is a base or next page. This bit is reset by read.
	0	RESERVED
Access Rules		
Register access		R
Value after reset		0004H

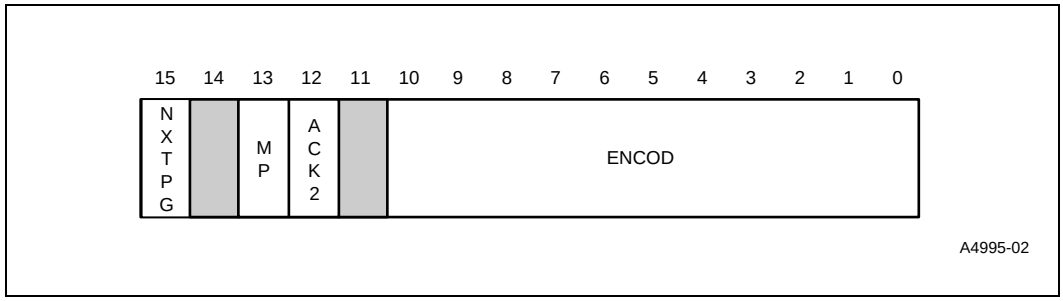
3.2.5.6 AN Next Page Register

Mnemonic: AN_NP_TR

Address: 5EH – 5FH

The AN next page transmit register contains the data that will be transmitted during next page exchange.

Note: When CPU bus is in 8 bit mode, write access to this register must be done to both addresses, starting at the low address.



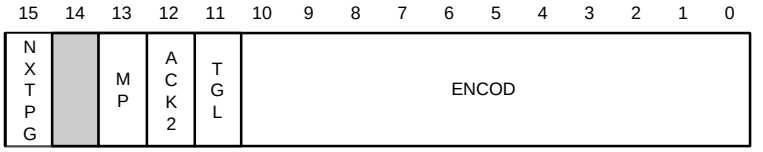
Bit Name	Bit #	Bit Description
NXTPG	15	**Next page.** When set, indicates a request for an additional next page exchange was made by the link partner.
—	14	RESERVED
MP	13	**Message page.** This bit indicates whether this page is a message page or an unformatted page.
ACK2	12	**Acknowledge 2.** This bit is used to indicate whether the device has the ability to comply with the message.
—	11	RESERVED
ENCOD	10:0	**Next page encoding.**
Access Rules		
Register access		Bits 15, 13:0 R/W. Bit 11 R.
Value after reset		0000H

3.2.5.7 AN Link Partner Receive Next Page Register

Mnemonic: AN_PRT_NP

Address: 60H – 61H

The AN link partner receive next page register contains the data of the link parameter next page.



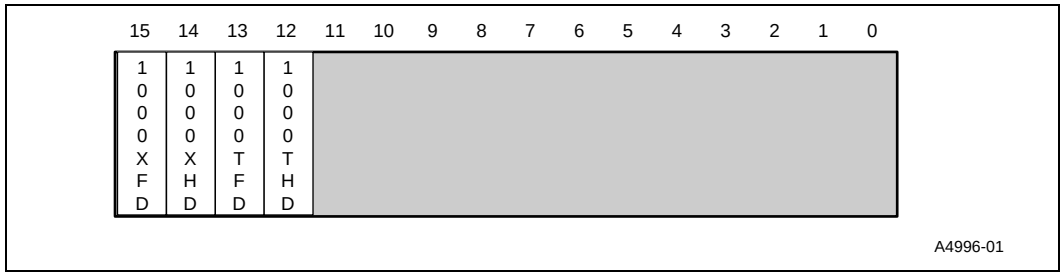
Bit Name	Bit #	Bit Description
NXTPG	15	**Next page.** When set, indicates a request for an additional next page exchange was made by the link partner.
—	14	RESERVED
MP	13	**Message page.** This bit indicates whether this page is a message page or an unformatted page.
ACK2	12	**Acknowledge 2.** This bit is used to indicate whether the link partner's device has the ability to comply with the message.
TGL	11	**Toggle**. This bit should get the opposite value of the toggle bit in the previously exchanged page.
ENCOD	10:0	**Next page encoding.**
Access Rules		
Register access		R
Value after reset		0000H

3.2.5.8 Extended Status Register

Mnemonic: GMII_EXT_STT

Address: 6EH – 6FH

The extended status register includes information about Giga bit modes of operations supported by the local device.



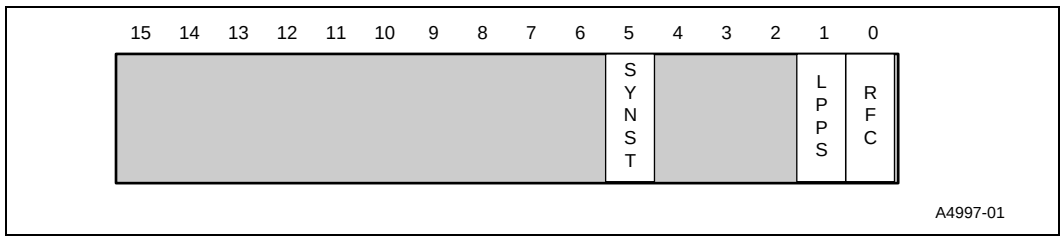
Bit Name	Bit #	Bit Description
1000XFD	15	**1000BASE-X full-duplex ability.** This bit is fixed at the value of 1.
1000XHD	14	**1000BASE-X half-duplex ability.** This bit is fixed at the value of 0.
1000TFD	13	**1000BASE-T full-duplex ability.** This bit is fixed at the value of 0.
1000THD	12	**1000BASE-T half-duplex ability.** This bit is fixed at the value of 0.
	11:0	RESERVED
Access Rules		
Register access		R
Value after reset		8000H

3.2.5.9 GPCS Status Register

Mnemonic: GPCS_STT

Address: 70H – 71H

The GPCS status register reports the parameters of the Auto-Negotiation and synchronization process. This register is used only in GPCS mode.



Bit Name	Bit #	Bit Description
—	15:6	RESERVED
SYNST	5	**Synchronization status.** A value of “0” indicates out of synchronization status. A value of “1” indicates that synchronization was acquired.
—	4:2	RESERVED
LPPS	1	**Link partner flow-control status.** A value of “0” indicates that link partner’s transmission will not be stopped upon reception of flow-control packets. A value of “1” indicates that link partner’s transmission will be stopped upon reception of flow-control packets.
RFC	0	**Receive flow-control status.** A value of “0” indicates that transmission will not be stopped upon reception of flow-control packets. A value of “1” indicates that transmission will be stopped upon reception of flow-control packets.
Access Rules		
Register access		R
Value after reset		0000H

3.3 Network Statistic Counter Mapping

This section describes the IXF1002 statistic counter mapping.

3.3.1 Register Mapping

Table 6 lists each network statistic IXF1002 register name, mnemonic, and offset.

I/O Base address: 100H or 200H.

Table 6. Network Statistic Register Mapping (Sheet 1 of 2)

Register Description	Mnemonic	I/O Address Offset
Transmit Statistic Counters		
The number of unicast packets transmitted without any errors.	TX_UNI_OK_CNT	00H – 03H
The number of multicast packets that are not broadcast, transmitted without any errors.	TX_MLT_OK_CNT	04H – 07H
The number of broadcast packets transmitted without any errors.	TX_BRD_OK_CNT	08H – 0BH
The number of transmitted packets, 64 bytes in length, including bad packets.	TX_PKT_64_CNT	24H – 27H
The number of transmitted packets, 65 to 127 bytes in length, including bad packets.	TX_PKT_65_CNT	28H – 2BH
The number of transmitted packets, 128 to 255 bytes in length, including bad packets.	TX_PKT_128_CNT	2CH – 2FH
The number of transmitted packets, 256 to 511 bytes in length, including bad packets.	TX_PKT_256_CNT	30H – 33H
The number of transmitted packets, 512 to 1023 bytes in length, including bad packets.	TX_PKT_512_CNT	34H – 37H
The number of transmitted packets, 1024 to 1518 bytes in length, including bad packets.	TX_PKT_1024_CNT	38H – 3BH
The number of transmitted packets larger than 1518 bytes, including bad packets.	TX_PKT_1519_CNT	3CH – 3FH
The number of correct transmitted flow-control packets.	TX_PAUSE_CNT	40H – 43H
The number of packets transmitted with an error due to transmit FIFO underflow or txerr signal assertion.	TX_ERR_CNT	44H – 47H
Transmit Byte Counters		
The number of bytes transmitted in good packets.	TX_OCT_OK_CNT	60H – 65H
The number of bytes transmitted in packets with errors.	TX_OCT_BAD_CNT	68H – 6DH
Receive Byte Counters		
The number of bytes received in good packets.	RX_OCT_OK_CNT	70H – 75H
The number of bytes received in packets with errors.	RX_OCT_BAD_CNT	78H – 7DH
Receive Statistic Counters		
The number of receive packets not fully accepted due to receive FIFO overflow.	RX_OVF_CNT	84H – 87H

Table 6. Network Statistic Register Mapping (Sheet 2 of 2)

Register Description	Mnemonic	I/O Address Offset
The number of packets, less than 64 bytes in length, received without any error.	RX_SHORT_OK_CNT	88H – 8BH
The number of packets less than 64 bytes in length, received with CRC error.	RX_SHORT_CRC_CNT	8CH – 8FH
The number of unicast packets with lengths between 64 bytes and the maximum packet size, received without any errors.	RX_UNI_OK_CNT	90H – 93H
The number of multicast packets with lengths between 64 bytes and the maximum packet size, received without any errors.	RX_MLT_OK_CN	94H – 97H
The number of broadcast packets with lengths between 64 bytes and the maximum packet size, received without any errors.	RX_BRD_OK_CNT	98H – 9BH
The number of packets with lengths between 64 bytes and the maximum packet size, received with an integral number of bytes and a CRC error.	RX_NORM_CRC_CNT	9CH – 9FH
The number of packets, larger than the maximum packet size, received without any error.	RX_LONG_OK_CNT	A4H – A7H
The number of packets, larger than the maximum packet size, received with a CRC error.	RX_LONG_CRC_CNT	A8H – ABH
The number of received packets, 64 bytes in length, including bad packets.	RX_PKT_64_CNT	ACH – AFH
The number of received packets, 65 to 127 bytes in length, including bad packets.	RX_PKT_65_CNT	B0H – B3H
The number of received packets, 128 to 255 bytes in length, including bad packets.	RX_PKT_128_CNT	B4H – B7H
The number of received packets, 256 to 511 bytes in length, including bad packets.	RX_PKT_256_CNT	B8H – BBH
The number of received packets, 512 to 1023 bytes in length, including bad packets.	RX_PKT_512_CNT	BCH – BFH
The number of received packets, 1024 to 1518 bytes in length, including bad packets.	RX_PKT_1024_CNT	C0H – C3H
The number of received packets, with lengths between 1519 bytes and the maximum packet size (programmable value), including bad packets.	RX_PKT_1519_CNT	C4H – C7H
The number of correct received flow-control packets.	RX_PAUSE_CNT	C8H – CBH
The number of false carrier events detected.	RX_FALS_CRS_CNT	CCH – CFH
The number of received packets during which PHY symbol errors were detected.	RX_GPCS_ERR_CNT	D0H – D3H

3.3.2 Network Statistic Counters Access Rules

The network statistic counters access rules are as follows:

- The counters can be accessed with a base address equal to 100H or 200H. Accessing the counters with the 100H base address causes them to reset. Accessing them with the 200H will not reset the counter.
- When the CPU data bus is in 16 bit mode, access to network statistic counters should be done only with even numbered addresses.
- The counters must be read from the lower to the upper bytes, in consecutive accesses.
- The statistic counters are not writable.

Note: When a counter reaches its highest possible value, it will continue to count from zero, and the corresponding counter overflow status bit will be set.

Note: Receive statistic counters are updated even if the receive FIFO overflows.

Note: All the byte counters take CRC bytes into account, but exclude the framing bits in the packets.

3.4 Access Sequences

This section describes the initialization, mode change, and interrupt handling sequences for the IXF1002.

3.4.1 Initialization Sequence

Each IXF1002 port must be initialized according to the following sequence:

1. Disable the port and reset it by writing a value of 07h to the port control register (PORT_CTR) and then writing 00h to clear the reset.
2. Initialize the port by writing to the relevant configuration registers.
3. Enable port operation by writing a value of 18h to the port control register (PORT_CTR).

3.4.2 Mode Change Sequence

In order to change the IXF1002 working mode without impacting packet transfer, the following sequence must be used:

1. Disable the port by writing a value of 00h to the port control register (PORT_CTR).
2. Wait until the port enters the stop state. The stop state entry may generate an interrupt if enabled, and is reported by the stop bit in the interrupt status register (INT_STT<STOP>).
3. Change the configuration register values.
4. Enable port operation by writing a value of 18h to the port control register (PORT_CTR).

Note: The port mode register (PORT_MODE) can be updated only by using the initialization sequence.

3.4.3 Interrupt Handling Sequence

Following interrupt, the subsequent sequence must be used to reset the interrupt:

1. If both ports are sharing the same interrupt line, perform steps 2 to 4 for each port that generates an interrupt.
2. Read the port interrupt status register (INT_STT) and act according to the interrupt cause.
3. If the packet event bit is set (INT_STT<PKEVE>), read the transmit and receive status register (TX_RX_STT) and act according to the interrupt cause. If the counter overflow bit is set (INT_STT<OVFC>), read the counter overflow status registers (TX_OV_STT and RX_OV_STT) to find out which counter has reached its highest possible value.
4. If the port was programmed to stop or underflowed while TX_RX_ERR<UNFS>=1, resume transmission by writing a value.

4.0 IX Bus Interface Operation

This section describes the IXF1002 IX Bus interface operation, including the transmission and reception flows.

4.1 IX Bus Interface

The IXF1002 uses a generic bus interface for data transfer to and from its FIFOs. The data bus is 64 bits wide and has three modes of operation. Big and little endian byte ordering are both supported on 32-bit boundaries (PORT_MODE<BEND>). The different FIFOs are accessed according to port selection signal (fps) as well as transmit or receive enabling signals (txsel_l, rxsel_l). Data transfer is synchronized to the main clock (clk), and new data may be sent or received on each clock cycle. Each FIFO has a dedicated signal for each direction (txrdy, rxrdy), reporting if it is ready for data transfer according to predetermined thresholds. (FFO_TSHD<TTH,RTH>). The burst size should be shorter than or equal to the effective threshold. The amount of data transferred during a FIFO access may be dynamically changed from one access to the other. On receive, if the PORT_MODE<HRYD> bit is reset, each first burst of a packet should be shorter than or equal to the header size.

4.1.1 IX Bus Operating Modes

The IXF1002 provides three IX Bus modes:

- Full-64 mode–64 bits for transmit or receive
- Split mode–32 low bits for receive, and 32 high bits for transmit
- Narrow mode–32 bits for transmit or receive

The selection of the IX Bus mode is done through the FIFMD field in the PORT_MODE register, as detailed in Section 3.2.3.3.

4.1.1.1 Signal Naming in Full-64 and Narrow Mode

When the IX Bus is in full-64 or narrow mode, signals fps, sop and eop are input during assertion of the txsel_l signal, and are output during assertion of the rxsel_l signal. In full-64 and narrow mode, fps_txf, sop_txf and eop_txf are not used and should be connected to pull-up resistors.

4.1.1.2 Signal Naming in Split Mode

When the IX Bus is in split mode, the three signals fps, sop and eop which are output signals, refer to the packets being received on the 32 low bits of the IX Bus. These three signals are then named fps_rxf, sop_rxf and eop_rxf. Three other input signals fps_txf, sop_txf and eop_txf refer to the packets being transmitted on the 32 high bits of the IX Bus. Figure 2, Figure 3 and Figure 4 show the signals of the parallel interface, depending on the different FIFO modes.

Note: When working in split-bus mode in port 1 only, there is a need to write both port's PORT_MODE registers.

Figure 2. Full-64 IX Bus Mode

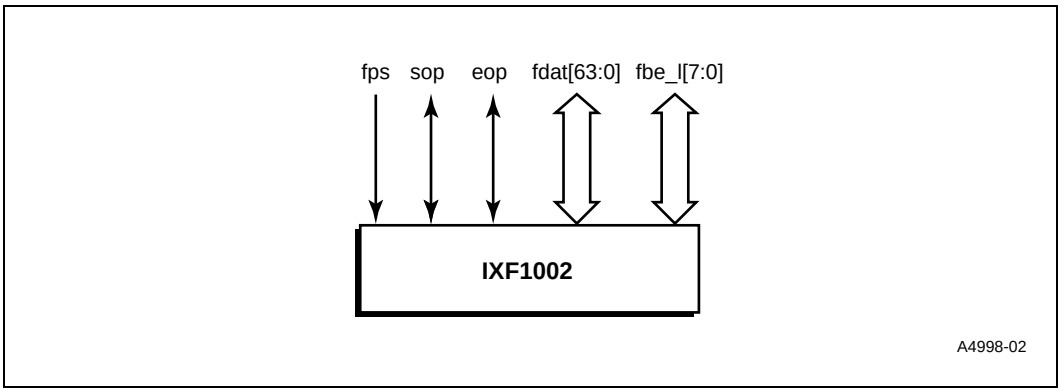


Figure 3. Narrow IX Bus Mode

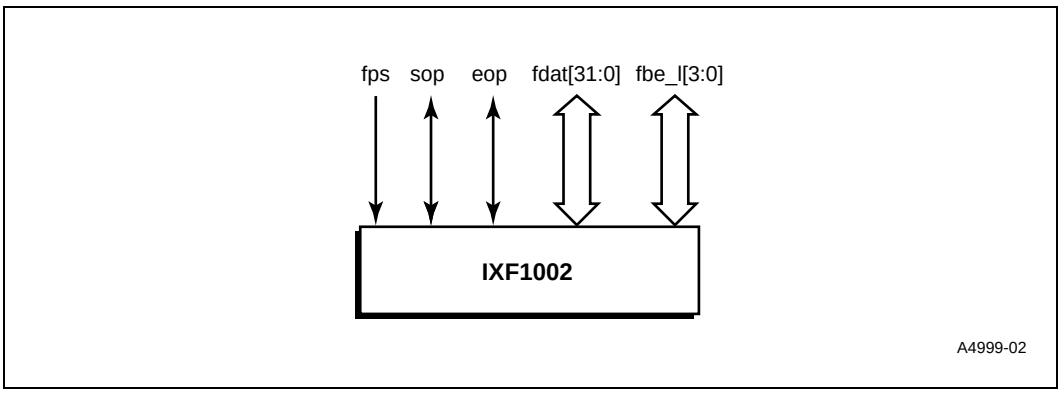
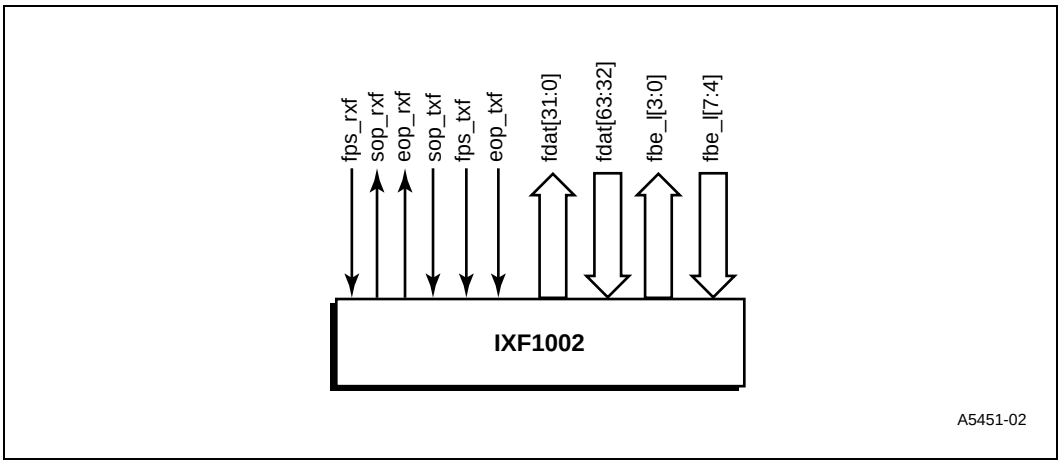


Figure 4. Split IX Bus Mode



4.1.2 Byte Ordering on IX Bus

On the IX Bus, bytes are ordered according to the endian mode (PORT_MODE<BEND>) and the bus mode (PORT_MODE). Figure 5, Figure 6 and Figure 7 show the different options for the little endian mode. Figure 8, Figure 9 and Figure 10 show the different options for the big endian mode.

Figure 5. Little Endian, Full-64 Bus Mode (BEND=0, FIFMD=01)

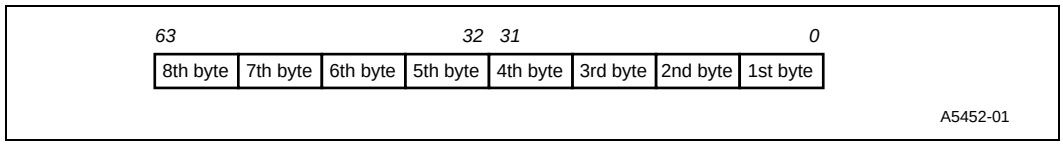


Figure 6. Little Endian, Split Bus Mode (BEND=0, FIFMD=10)

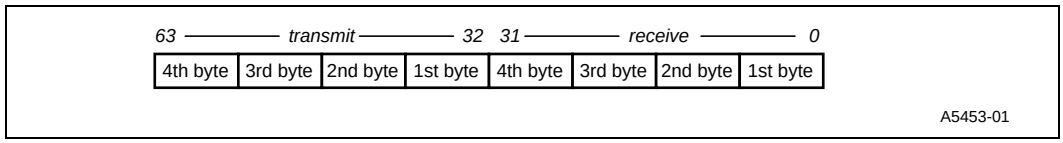


Figure 7. Little Endian, Narrow Bus Mode (BEND=0, FIFMD=00)

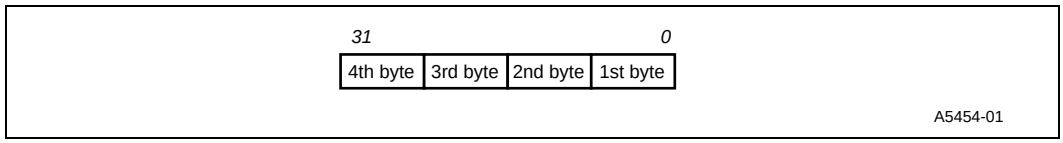


Figure 8. Big Endian, Full-64 Bus Mode (BEND=1, FIFMD=01)

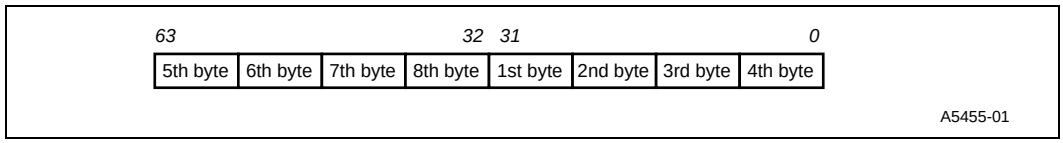


Figure 9. Big Endian, Split Bus Mode (BEND=0, FIFMD=10)

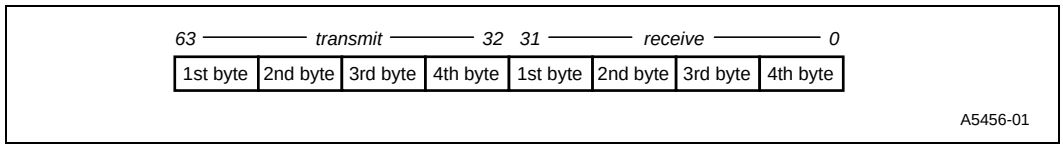
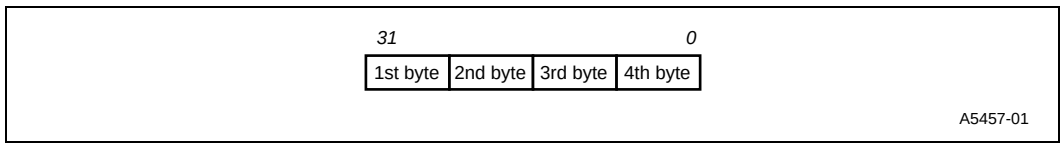


Figure 10. Big Endian, Narrow Bus Mode (BEND=1, FIFMD=00)



4.1.3 FIFO Status Signaling

The IXF1002 reports the status of each FIFO through dedicated signals. Each transmit FIFO has a txrdy signal indicating that there is enough free space to load new data. Each receive FIFO has a rxrdy signal indicating that there is enough data to be transferred onto the IX Bus. The txrdy signals are driven by the IXF1002 only when the txctl_l signal is asserted. The rxrdy signals are enabled by the rxclt_l signal.The txrdy signal of a specific port is deasserted when the txsel_l signal is asserted and the specific port is selected (fps). The same applies for the rxrdy signal of a specific port, which is deasserted with rxsel_l assertion and the specific port selection (fps).

4.2 Packet Transmission

The following sections describe the packet transmission policy.

Note: The signal naming below refers to the Full-64 IX Bus mode. Signal names should be changed in accordance to the bus mode as described in Section 4.1.1.1 and Section 4.1.1.2.

4.2.1 Packet Loading

The IXF1002 loads packets from the IX Bus into the transmit FIFO during burst accesses. In order to guarantee a minimal amount of data transfer, the transmit FIFO txrdy signal reports minimal space availability according to a programmable threshold (FFO_TSHD<TTH>).

When a new packet is loaded on the FIFO, the first cycle of the first burst must be signalled with sop signal assertion. If TX_RX_PARAM<CRCD> is set or if the txasis signal is asserted together with the sop signal, the packet will be sent onto the network without padding or CRC addition. In this case, it is assumed by the IXF1002 that the CRC is valid and it will not be checked.

At the end of a packet load, the last data must be signalled with the assertion of the eop signal in the last cycle of the last burst. If the txerr signal is asserted together with eop, the GMII error signal terr will be asserted or a symbol error will be generated (GPCS mode) in the last data byte of the packet sent onto the network. The CRC will be damaged if it was requested to be appended by the IXF1002.

Note: In case of VLAN tag append, strip or replace, the frame check sequence (FCS) field will be calculated by the IXF1002 (see Section 4.2.2.1).

The IXF1002 may be programmed to handle only a single packet at a time (TX_RX_PARAM<SPM>).

Byte masking signals (fbe_l[7:0]) may be used to load selective bytes. They can be used during packet transfer to load packet segments on byte boundaries and for loading the exact number of bytes at the end of a packet. Valid bytes may start at any byte boundary, while all valid bytes, in a given cycle, need to be contiguous.

For example, a packet may be built up from the following buffers, with each one being transferred in a different burst:

Buffer 1:

B3	B2	B1	X	X	X	X	X
B11	B10	B9	B8	B7	B6	B5	B4
X	X	X	X	X	X	X	B12

A5458-01

Buffer 2:

X	X	X	B14	B13	X	X	X

A5459-01

Buffer 3:

X	B19	B18	B17	B16	B15	X	X
X	X	B21	B20	X	X	X	X

A5460-01

4.2.2 VLAN Tagging

The IXF1002 supports IEEE P802.1Q Virtual Bridged Local Area Networks (VLAN) standard.

Figure 11 shows the format of a tagged MAC frame. This format is an extension of the basic MAC frame, as specified in IEEE 802.3 standard (see Section 6.3).

Figure 11. VLAN Tagged MAC Frame Format

Preamble	SFD	Destination Address	Source Address	QTag Prefix		Length/ Type	Data+ Padding	FCS
				Length/ Type	Control Information			
(7)	(1)	(6)	(6)	(4)		(2)	(46..1500)	(4)

A5461-01

Note: Numbers in parentheses indicate field length in bytes.

The QTag Prefix field is 4 octets long. The first two octets transferred on to the network are called the Tagged MAC Frame Length/Type field and contain a constant value of 8100H. The following two octets are called the Tag Control Information field and are subdivided as follows:

- A three-bit user priority field
- A one-bit Canonical Format Indicator (CFI)
- A 12-bit VLAN identifier.

Note: The minimal frame length supported by VLAN mode is 18 bytes. If the txasis signal is asserted together with the sop signal or TX_RX_PARAM<CRCD=1>, the minimal frame length supported is 22 bytes.

4.2.2.1 VLAN Tag Functions in IXF1002

The IXF1002 is able to append, strip, or replace a VLAN tag during packet transmission.

In case of VLAN tag append, strip, or replace, the Frame Check Sequence (FCS) field will be calculated by the IXF1002.

If the txasis signal is asserted together with the sop signal or if TX_RX_PARAM<CRCD=1>, the IXF1002 will replace the four last bytes of the MAC frame with the recalculated FCS.

If the txasis signal is not asserted together with the sop signal and TX_RX_PARAM<CRCD=0>, the IXF1002 will append the recalculated FCS field to the end of the MAC frame.

4.2.2.2 VLAN Tag Append

When appending a VLAN tag, the IXF1002 takes two bytes from the VLAN_TAG register and two bytes from the IX Bus, and builds a four byte VLAN tag. The VLAN tag is inserted into the basic MAC frame at an offset of 12 bytes from the beginning of the frame.

The value entered by the IXF1002 into the tagged MAC frame length/type field is 8100H. This value can be changed through the VLAN_TAG register.

The value of the tag control information field should be transferred to the IXF1002 through the IX Bus before each MAC frame.

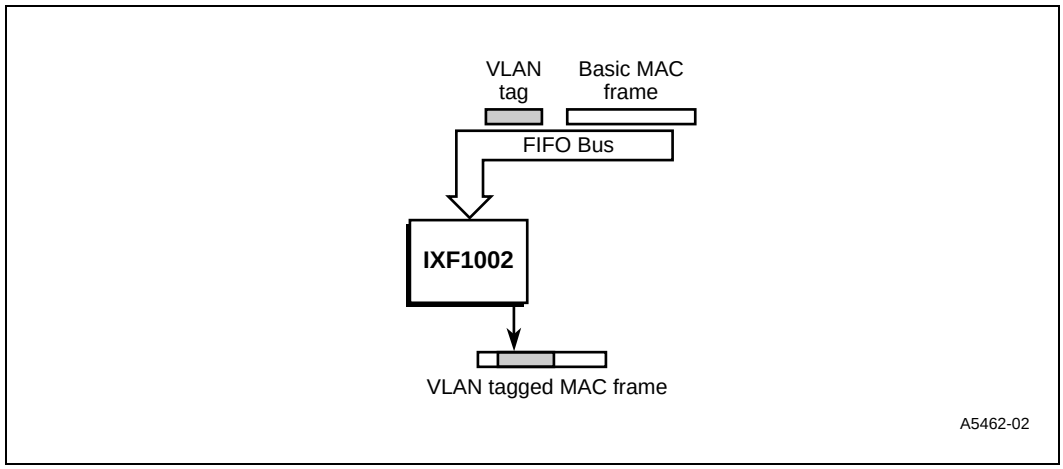
For appending a VLAN tag to a basic MAC frame, the following procedure should be performed:

Before transferring the basic MAC frame onto the IX Bus, assert the vtg signal for one cycle together with the transfer of the tag control information field (16 bits) on the IX Bus. This data should be transferred on the 16 low bit of the IX Bus (fdat[15:0] in Full-64 and Narrow mode, and fdat[47:32] in split mode). During this cycle, the value of the fbe_l[7:0] signals have no meaning.

When asserting the vtg signal, the txsel_l signal should be asserted and the specific port should be selected (fps). The basic MAC frame could be transferred any time after the transfer of the tag control information field in the same or different txsel_l burst (see Section 7.1.4).

Figure 12 shows VLAN tag append.

Figure 12. VLAN Tag Append



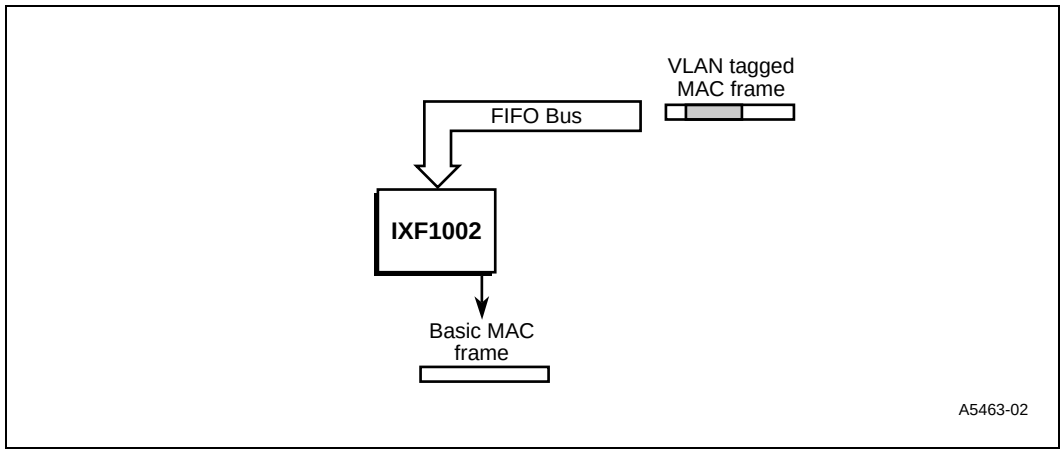
4.2.2.3 VLAN Tag Strip

For stripping a VLAN tag from a VLAN tagged MAC frame, the following procedure should be performed:

Packet Transmission	For every VLAN tagged MAC frame transferred onto the IX Bus, assert the vtg signal for one cycle at the beginning of the MAC frame together with the assertion of the sop signal (see Section 7.1.5).

Figure 13 shows the VLAN tag strip.

Figure 13. VLAN Tag Strip

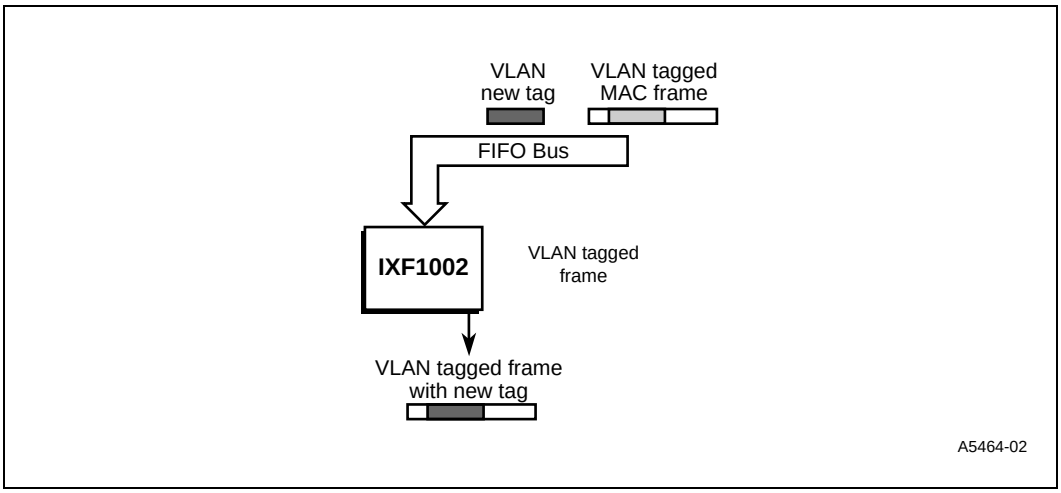


4.2.2.4 VLAN Tag Replace

For replacing a VLAN tag that exists in a VLAN tagged MAC frame with a new VLAN tag, execute the VLAN tag append and the VLAN tag strip procedures on the same MAC frame (see Section 7.1.6).

Figure 14 shows VLAN tag replacement

Figure 14. VLAN Tag Replace



4.2.3 Network Transmission

The IXF1002 will start to transmit the packet if there is enough data on the transmit FIFO according to the programmable transmission threshold (TX_TSHD<TSD>), or if the full packet is loaded onto the transmit FIFO.

If the packet is transmitted successfully, the next packet loaded onto the FIFO is transmitted onto the network, using the programmable IPG_VAL<IPG> gap between them.

4.2.4 FIFO Underflow

In case of an underflow error, the IXF1002 can be programmed to stop or continue working. By default (error continue mode) the IXF1002 will continue with the next packet loaded after an underflow. In this mode the IX Bus will behave the same way with or without an underflow. In both modes the appropriate statistics counters will be updated.

Following an underflow, packet transmission is truncated. The GMII error signal terr will be asserted or a symbol error will be generated (GPCS mode) in the last data byte. A bad CRC will be appended to the packet, if the IXF1002 is programmed to append the CRC. If the underflow occurs before the transmission of 60 bytes, padding is added.

4.2.4.1 Stopping Mode on Transmission Underflow Error

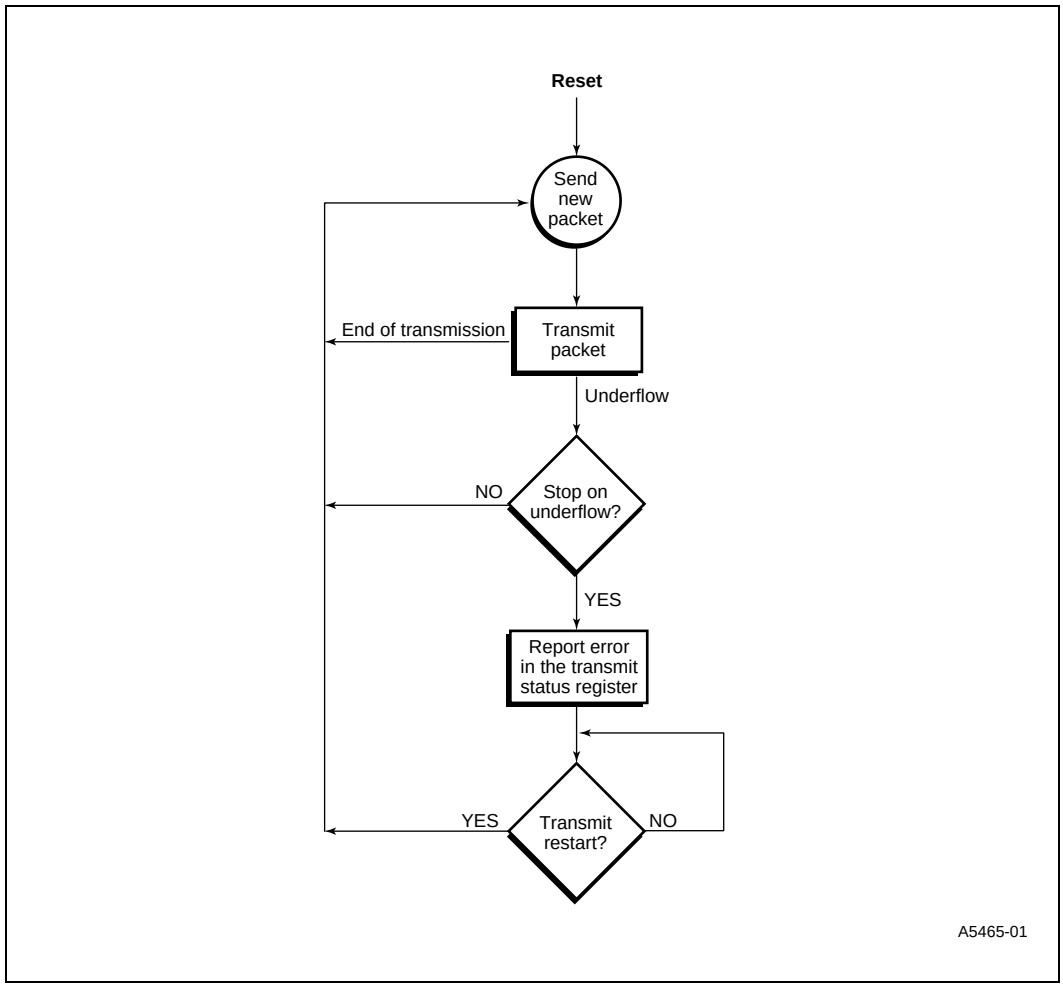
If the IXF1002 is programmed to stop after an underflow (TX_RX_ERR<UNFS>), the transmit FIFO will be flushed and no more packets will be transmitted. The number of packets flushed from the transmit FIFO and the underflow event are reported in the transmit and receive status register (TX_RX_STT). Subsequent packets will be loaded only after the FIFO is restarted (PORT_CTR<TXSTT>).

The transmission underflow error may also generate an interrupt, if programmed to do so (INT_EN<PKEVE>).

4.2.5 Transmit Flow Diagram

Figure 15 shows the transmit flow diagram.

Figure 15. Transmit Flow Diagram



4.3 Packet Reception

The following sections describe the packet reception policy.

Note: The signal naming below refers to the Full-64 IX Bus mode. Signal names should be changed in accordance to the bus mode as described in Section 4.1.1.1 and Section 4.1.1.2.

4.3.1 Packet Storing

Packets received from the network are loaded into the receive FIFO. Received packets are transferred from the receive FIFO onto the IX Bus during burst accesses. To indicate the minimal amount of data available in the receive FIFO, the rxrdy signal is asserted according to a programmable threshold. (FFO_TSHD<RTH>). If the end of a packet is loaded onto the FIFO, the rxrdy signal is asserted even if the amount of data available is below the threshold value.

The fbe_l[7:0] signals are used to report which bytes driven onto the bus are valid. For example, they indicate which bytes are valid in the last bus transfer of a packet.

At a given time, multiple packets may be loaded in the receive FIFO, up to the FIFO limit.

The first packet data is signalled with the sop signal, while the last data is signalled with the eop signal. Following the last data transfer of a received packet, a field describing the packet status can be programmed to be driven on the data bus, reporting the status of the packet and its length. Further reads from the receive FIFO during the same access will be ignored, and the byte enable for these additional read transactions will report that all bytes contain invalid data (fbe_l<7:0>=FFh). This is done to prevent transfer of the next packet in the same burst. If the IXF1002 is programmed to remove CRC (TX_RX_PARAM<CRCR>), the last four bytes of the packet will not be transferred on the IX Bus, and the eop signal will be asserted on the packet's last data byte. In the CRC remove mode, packets that are four bytes long or less will be discarded, even if the IXF1002 is programmed to pass short packets (TX_RX_ERR<PSRT>).

4.3.1.1 Packet Status

When packet status mode is enabled (PORT_MODE<PS_D=0>, the packet status is appended to any received packet completely transferred onto the IX Bus, and is driven onto the IX Bus in the access following the last byte transfer. The packet status is driven on the IX Bus according to the description in Table 7. In full 64-bit FIFO mode, the status will be driven on fdat<63:32> and fdat<31:0>. In narrow and split IX Bus modes, the status will be driven on fdat<31:0>. The status will always be driven as little endian data as described in Figure 5, Figure 6, and Figure 7. During status transfer, the value of the fbe_l<7:0> signals have no meaning and should be ignored. The full status word is always valid.

If the eop signal is asserted on the last cycle of the burst, the rxrdy signal will be asserted, and the packet status will pass in the next burst of the rxsel_l signal.

The packet length reports the number of bytes received in this packet on the serial line, independent of the packet transfer on the IX Bus.

Table 7 describes the IX Bus receive packet status.

Table 7. IX Bus Receive Packet Status

Bit Name	Bit Number	Bit Description
LEN	31:16	Packet length
—	15:11	RESERVED
MLT	10	Multicast packet
BRD	9	Broadcast packet
ROK	8	Receive OK
FLW	7	Flow-control packet
—	6	RESERVED
GMER	5	GMII error
RTL	4	Too long packet
SHRT	3	Short packet
—	2	RESERVED
CRC	1	CRC error
OVF	0	Receive FIFO overflow (if set, LEN field is not valid)

4.3.2 Header Preprocessing

The IXF1002 supports the ability to process the packet header in several ways. The header size is programmable (TX_RX_PARAM<HDRS>) and may be changed according to the required processing (for example, MAC header, VLAN header, or Layer3 header).

When header-ready mode is enabled (FFO_BUS<HRYD=0>) and a packet header has been fully loaded into the receive FIFO, the IXF1002 will assert the rxrdy signal even if the header size is smaller than the programmed receive threshold (FFO_TSHD<RTH>). In this case, the first burst of a packet must be shorter than or equal to the header size.

The packet header may also be read from the receive FIFO for processing without removing it from the FIFO. If the IXF1002 is programmed to work in the header replay mode (TX_RX_PARAM<HRPL>), the packet header will be transferred twice onto the IX Bus: first time for header processing and second time with the packet transfer.

4.3.3 Packet Segmentation

The IXF1002 supports receive-packet segmentation on any byte boundary. When the rxkep signal is asserted on the last data transfer of a burst, the same data will be transferred as the first data word of the next burst.

The rxkep signal is ignored when it is asserted in one of the following cases: invalid data, last data of the packet, or last data of the header on header replay mode (TX_RX_PARAM<HRPL>).

Packets may be split to multiple buffers, as in the following example.

rxkep is asserted on the last cycle of a three octal word burst from the IXF1002, causing the third octal word to be retained in the receive FIFO. During the next receive burst, this same octal word will be driven as the first data word of the burst. Masking of data bytes to the buffers is performed by the host. In the following example, the host places bytes 1–19 in the first buffer (as result of the first burst, which are bytes 1–24). And bytes 20–28 in the second buffer (as a result of the second burst, which are bytes 17–24).

Buffer 1:

B8	B7	B6	B5	B4	B3	B2	B1
B16	B15	B14	B13	B12	B11	B10	B9
X	X	X	X	X	B19	B18	B17

A5466-01

Buffer 2:

B24	B23	B22	B21	B20	X	X	X
X	X	X	X	B28	B27	B26	B25

A5467-01

4.3.4 Packet Abortion

During the transfer of a received packet onto the IX Bus, the IXF1002 supports the ability to prevent any further transfer of this packet. At any time during packet reception, the packet may be dynamically discarded from the receive FIFO by asserting the rxabt signal during packet reading while rxsel_l signal is asserted. Any subsequent packet loaded onto the receive FIFO is not affected by rxabt assertion. The next FIFO access will access the new packet.

4.3.5 Network Reception

A packet received from the network is loaded to the receive FIFO. If the packet is received without any error, it is transferred to the IX Bus. If an error occurs during reception, the packet is handled according to the programming in the TX_RX_ERR register.

The IXF1002 may be programmed to work in two modes: reject the erroneous packet or accept it. In both modes, the appropriate statistic counters will be updated (even if the packet was rejected due to packet error or FIFO overflow), and any following packets will continue to be accepted and loaded to the receive FIFO.

The following events are considered as reception errors:

- FIFO overflow
- CRC error
- Short packet
- Too long packet
- GMII error

4.3.6 Rejecting Mode on Reception Errors

If a packet with a reception error is programmed to be rejected (zero in the relevant bit of the TX_RX_ERR register). The IXF1002 discards the packet from the receive FIFO without affecting previous packets that may still be in the receive FIFO. If the packet had not yet started to be transferred on the IX Bus, it will be discarded without affecting IX Bus activity. If the packet had already started to be transferred onto the IX Bus, or rxrdy was already asserted, the rxfail signal will be asserted on the next FIFO access, indicating that the currently transferred packet was discarded from the receive FIFO. Packet status will not be driven for such a packet.

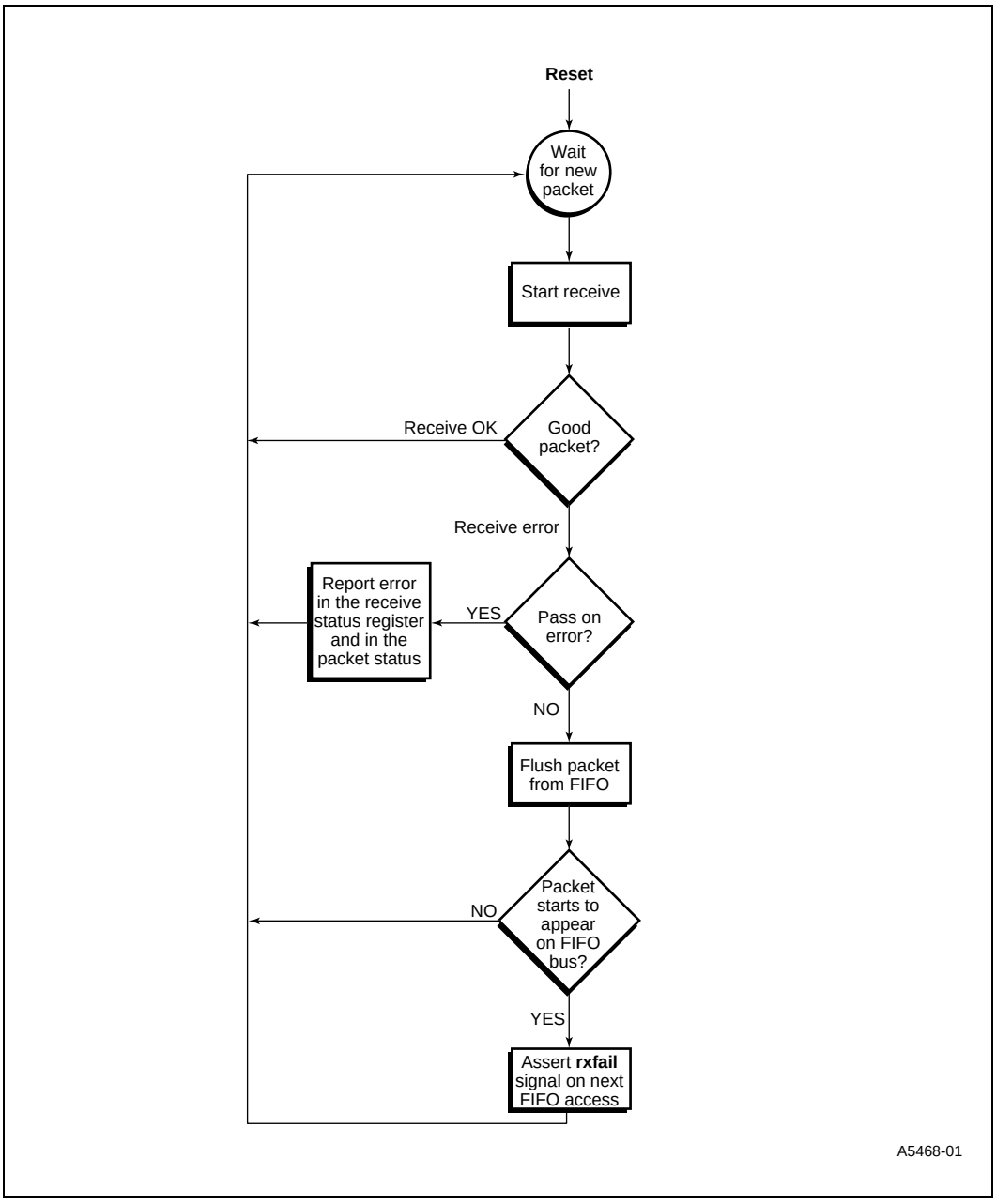
4.3.7 Accepting Mode on Reception Errors

If a packet with a reception error is programmed to be accepted, (a 1 in the relevant bit of the TX_RX_ERR register), it is transferred to the IX Bus as a regular packet. The event type is reported in the packet status appended to the end of the packet, and in the transmit and receive status register (TX_RX_STT).

4.3.8 Receive Flow Diagram

Figure 16 shows the receive flow diagram.

Figure 16. Receive Flow Diagram



5.0 CPU Interface Operation

The following sections describe the CPU interface operation.

5.1 CPU Interface

The IXF1002 has a dedicated port for a CPU interface, enabling access to the different registers without interfering packet transfer through the FIFOs. The CPU interface is generic and supports a wide range of standard controllers. Each of the two IXF1002 ports has its own independent registers. Each of the port registers is accessible through an 8/16-bit-wide data bus and a 10-bit-wide address bus. A specific port is addressed by using the port select signal (cps), which may be considered a part of the address bus. Each port has a dedicated interrupt signal (cint_l_{i}) to report special events to the CPU.

The IXF1002 supports two CPU data bus widths: 8 (default) and 16 bit (controlled by the PORT_MODE<CPUBW> bit). In 16 bit mode, registers are accessible only through an even numbered address. In 8 bit mode, each byte is accessed independently through its individual address.

Each control and status register is 2 bytes wide. Network statistic counters are 4 bytes or 6 bytes wide and require multiple CPU accesses to be fully read.

5.2 Network Management

The IXF1002 includes statistic counters defined by Ethernet SNMP MIB and RMON MIB standards. Each event counter is 4 byte wide and each byte counter is 6 byte wide.

To assemble each counter value, its bytes must be read from the lower to the upper addresses.

Each counter is accessible through two different addresses. One address will cause the read bytes to reset, while the other will not. When a counter overflows, it resets automatically, causes the corresponding bit in the counter overflow status registers (TX_OV_STT and RX_OV_STT) to assert, and can generate an interrupt if programmed accordingly (see Section 3.2.2.2 and Section 3.2.3.12).

Partial byte reading is also possible. If the exact counter value is not required, the lower counter bytes may not be read. If the counter is read often through an address that reset its count (with a 100H offset), the upper byte will always remain null and may not be read.

Receive statistic counters are updated according to analysis of the received packet, while ignoring the IXF1002 filtering mode or the receive FIFO status. When the port is in the disable mode, the counters are not updated.

5.2.1 SNMP MIB Support

The IXF1002 supports Ethernet MIB according to Table 8.

Table 8. SNMP MIB to IXF1002 Counters Mapping

SNMP MAC Counters	IXF1002 Statistic Counters
FramesTransmittedOK	TX_UNI_OK_CNT + TX_MLT_OK_CNT + TX_BRD_OK_CNT
FramesReceivedOK	RX_UNI_OK_CNT + RX_MLT_OK_CNT + RX_BRD_OK_CNT
FramesCheckSequenceErrors	RX_NORM_CRC_CNT
OctetsTransmittedOK	TX_OCT_OK_CNT
OctetsReceivedOK	RX_OCT_OK_CNT
FrameTooLongErrors	RX_LONG_OK_CNT + RX_LONG_CRC_CNT
MulticastFramesXmittedOK	X_MLT_OK_CNT
BroadcastFramesReceivedOK	RX_BRD_OK_CNT
MulticastFramesReceivedOK	RX_MLT_OK_CNT
BroadcastFramesXmittedOK	TX_BRD_OK_CNT
PauseFramesTransmitted	TX_PAUSE_CNT
PauseFramesReceived	RX_PAUSE_CNT

5.2.2 RMON Statistic Group Support

Table 9 describes the IXF1002 support of the RMON statistic group. If packets are loaded into the IXF1002 to be transmitted as bad packets, they must be counted in the error counters, too.

Table 9. RMON Statistics to IXF1002 Counters Mapping (Sheet 1 of 2)

RMON Statistic Counters	IXF1002 Statistic Counters
etherStatsDropEvents	RX_OVF_CNT
etherStatsOctets	TX_OCT_OK_CNT + TX_OCT_BAD_CNT + RX_OCT_OK_CNT + RX_OCT_BAD_CNT
etherStatsPkts	TX_UNI_OK_CNT + RX_UNI_OK_CNT + ether-StatsBroadcastPkts + etherStatsMulticastPkts + etherStatsCRCAlignErrors + etherStatsUndersizeP-kts + etherStatsFragments + etherStatsOversizePkts + etherStatsJabber
etherStatsBroadcastPkts	TX_BRD_OK_CNT + RX_BRD_OK_CNT
etherStatsMulticastPkts	TX_MLT_OK_CNT + RX_MLT_OK_CNT
etherStatsCRCAlignErrors	RX_NORM_CRC_CNT + TX_ERR_CNT
etherStatsUndersizePkts	RX_SHORT_OK_CNT
etherStatsOversizePkts	RX_LONG_OK_CNT
etherStatsFragments	RX_SHORT_CRC_CNT
etherStatsJabber	RX_LONG_CRC_CNT
etherStatsPkts64Octets	TX_PKT_64_CNT + RX_PKT_64_CNT
etherStatsPkts65to127Octets	TX_PKT_65_CNT + RX_PKT_65_CNT
etherStatsPkts128to255Octets	TX_PKT_128_CNT + RX_PKT_128_CNT

Table 9. RMON Statistics to IXF1002 Counters Mapping (Sheet 2 of 2)

RMON Statistic Counters	IXF1002 Statistic Counters
etherStatsPkts256to511Octets	TX_PKT_256_CNT + RX_PKT_256_CNT
etherStatsPkts512to1023Octets	TX_PKT_512_CNT + RX_PKT_512_CNT
etherStatsPkts1024to1518Octets	TX_PKT_1024_CNT + RX_PKT_1024_CNT
etherStatsDropEvents	RX_OVF_CNT
etherStatsOctets	TX_OCT_OK_CNT + TX_OCT_BAD_CNT + RX_OCT_OK_CNT + RX_OCT_BAD_CNT

5.2.3 RMON Host Group Support

Table 10 describes the IXF1002 support of the RMON host group when a single node is connected to a port. If packets are loaded into the IXF1002 to be transmitted as bad packets, they must be counted in the error counters too.

Table 10. RMON Host to IXF1002 Counters Mapping

RMON Host Counters	IXF1002 Statistics Counters
hostInPkts	TX_UNI_OK_CNT + TX_MLT_OK_CNT + TX_BRD_OK_CNT
hostOutPkts	RX_UNI_OK_CNT + RX_MLT_OK_CNT + RX_BRD_OK_CNT + RX_NORM_CRC_CNT + RX_SHORT_OK_CNT + RX_SHORT_CRC_CNT + RX_LONG_OK_CNT + RX_LONG_CRC_CNT
hostInOctets	TX_OCT_OK_CNT
hostOutOctets	RX_OCT_OK_CNT + RX_OCT_BAD_CNT
hostOutErrors	RX_NORM_CRC_CNT + RX_SHORT_OK_CNT + RX_SHORT_CRC_CNT + RX_LONG_OK_CNT + RX_LONG_CRC_CNT
hostOutBroadcastPkts	RX_BRD_OK_CNT
hostOutMulticastPkts	RX_MLT_OK_CNT

6.0 Network Interface Operation

This section describes the GMII/GPCS port operation. It also describes media access control (MAC), full-duplex, and loopback operations. The IXF1002 supports implementation of the MAC sublayer according to the IEEE 802.3z standard, in full-duplex mode.

6.1 Operating Modes

Each of the IXF1002 two ports supports GMII or GPCS interfaces.

In the GMII mode, the GMII port provides a standard and simple interconnection between the MAC sublayer and the PHY layer. In this mode, the IXF1002 can be used with any device with an GMII interface that implements the 1000BASE-SX, 1000BASE-LX, 1000BASE-CX, or 1000BASE-T standards.

The GMII interface comprises the following characteristics:

- Supports 1000 Mb/s data rate
- Includes data and delimiters that are synchronous to clock references
- Provides independent, 8-bit-wide transmit and receive data paths
- Utilizes TTL signal levels
- Provides a simple management interface through mdc and mdio signals

In the GPCS mode, the 8B/10B encoding/decoding is done by the IXF1002, which enables connection of serializer/deserializer (SERDES) devices implementing de/serialization and clock recovery for the 1000BASE-SX, 1000BASE-LX or 1000BASE-CX standards.

The GPCS port is multiplexed together with the GMII port.

6.2 GMII Port Interface

In the GMII mode (PORT_MODE<GPCS=0>), the IXF1002 implements the IEEE 802.3 Standard GMII interface. Table 11 describes the GMII port signal names as they refer to the appropriate IEEE 802.3 signal names.

The GMII management signals (mdc and mdio) are common to both ports.

Table 11 describes the GMII port signals versus standard signals.

Table 11. GMII Port Signals versus Standard Signals

GMII Signals	IEEE 802.3 Signals	I/O	Purpose
tclk	—	I	This signal operates at 125 MHz, and is used as a reference clock for the gtxclk_{i} output signals.
gtxclk_{i}	gtx_clk	O	125MHz clock which provides the timing reference for the transfer of the ten{i}, terr{i}, and txd_{i} signals.
rclk_{i}	rx_clk	I	Receive clock, synchronizes all receive signals (dv{i}, rxd_{i}<7:0>, rerr{i}).
ten{i}	tx_en	O	Transmit enable, asserted by the MAC sublayer when the first transmit preamble byte is driven over the GMII. It remains asserted for the remainder of the frame, up to the last CRC byte.
txd_{i}<7:0>	txd<7:0>	O	These lines provide transmit data, driving a byte on each tclk cycle when ten{i} is asserted.
terr{i}	tx_err	O	Transmit error, asserted by the MAC layer to generate a coding error on the byte currently being transferred over txd_{i}<7:0>.
dv{i}	rx_dv	I	Receive data valid, asserted by the PHY layer when the first received preamble byte is driven over the GMII. It remains asserted for the remainder of the frame, up to the last CRC byte.
rxd_{i}<7:0>	rxd<7:0>	I	These lines provide receive data, driving a byte on each rclk_{i} cycle when dv{i} is asserted.
rerr{i}	rx_err	I	Receive error, asserted by the PHY layer to indicate an error the MAC cannot detect. If asserted during packet reception, indicates a coding error on the frame currently being transferred on rxd_{i}<7:0>.
mdc	mdc	O	Management data clock, the mdio signal clock reference.
mdio	mdio	I/O	Management data input/output, used to transfer control signals between the PHY layer and the manager entity. The IXF1002 is capable of initiating control signal transfer between the IXF1002 and the PHY devices.

6.3 MAC Frame Format

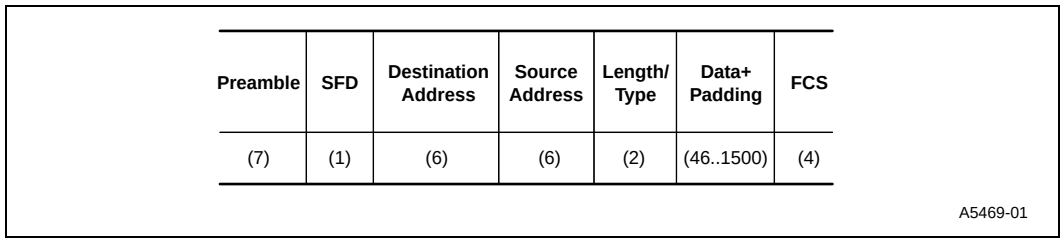
Ethernet is the generic name for the network type implementing the IEEE 802.3 Standard. An Ethernet frame has a minimum length of 64 bytes and a maximum length of 1518 bytes, excluding the preamble and the SFD bytes.

An Ethernet frame format consists of the following fields:

- Preamble
- Start frame delimiter (SFD)
- Two address fields
- Length or type field
- Data field
- Frame check sequence (CRC value)

Figure 17 shows the MAC frame format.

Figure 17. MAC Frame Format



Note: Numbers in parentheses indicate field length in bytes.

VLAN tagged MAC frames contain an additional 4 byte Qtag prefix field, as described in Section 4.2.2. Table 12 describes the Ethernet frame fields.

Table 12. Ethernet Frame Description

Field	Description
Preamble	A 7-byte field of alternating 1s and 0s: 10101010.
Start Frame Delimiter (SFD)	A single-byte field containing the value 10101011.
Destination address	A 6-byte field containing either a specific station address, or the broadcast address, or a multicast (logical) address, all of which indicate the frame's destination.
Source address	A 6-byte field containing the specific station address of frame origin.
Length/type	A 2-byte field indicating whether the frame is in the IEEE 802.3 format or the Ethernet format. A field greater than 1500 is interpreted as a type field, which defines the protocol type. A field smaller than or equal to 1500 (05-DC) is interpreted as a length field, indicating the number of data bytes in the frame.
Data+Padding	A data field consisting of 0 to 1500 information bytes. This data field is fully transparent because any arbitrary sequence of bits can occur. A data field shorter than 46 bytes, specified by the length field, is allowed. In its default mode, padding is enabled and up to 46 bytes are added to the data field by the IXF1002 when transmitting.
Frame Check Sequence (FCS)	A 32-bit cyclic redundancy check (CRC), computed as a function of the destination address field, source address field, type field, and data field. The FCS is appended to each transmitted frame and is used during reception to determine if the received frame is valid.

The CRC polynomial, as specified in the 802.3 Standard, is as follows:

$$FCS(X) = X^{31} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X^{1} + 1$$

The 32 bits of the CRC value are placed in the FCS field so that the X31 term is the right-most bit of the first octet. The CRC bits are thus transmitted in the following order: X31, X30,..., X1, X0.

A frame octet is transferred on the serial line from the LSB to the MSB.

6.4 MAC Transmit Operation

This section describes the transmit operation in detail, as supported by the IXF1002. Transmit activities are registered into the network management registers, which are accessible through the CPU port.

6.4.1 Transmit Initiation

After the transmit FIFO is adequately filled up to the programmed threshold level (TX_TSHD<TSD>), or after there is a full frame loaded into the transmit FIFO, the IXF1002 starts to encapsulate the frame. The transmit encapsulation is performed by the transmit controller, which delays the actual transmission of the data onto the network until it has been idle for a minimum interpacket gap (IPG) time.

6.4.2 Inter Packet Gap

Actual transmission of the data onto the network occurs 96-bit time period (by default) after the completion of the last transmission. The interpacket gap time can be changed through the IPG_VAL register. In accordance with the standard, the IXF1002 begins to measure the IPG in full-duplex mode from TEN deassertion.

6.4.3 Frame Encapsulation

The transmit data frame encapsulation stream includes the appending of the 56 preamble bits and the 8 bits of SFD to the basic frame beginning, and the FCS to the basic frame end. The basic frame loaded from the bus includes the destination address field, the source address field, the type/length field, and the data field. If the data field length is shorter than 46 bytes and pad appending is not disabled (TX_RX_PARAM<PADD> or TX_RX_PARAM<CRCD>), the IXF1002 pads the basic frame with the pattern 00 for up to 46 bytes. At the end of the frame, the IXF1002 appends the FCS field if CRC appending is not disabled (TX_RX_PARAM<CRCD>). If the txasis signal is asserted at the beginning of the packet load, the IXF1002 ignores the programmed mode and transmits the frame without the padding and the FCS field.

In the GMII mode, the transmit enable signal (ten{i}) is asserted together with the first preamble byte transmission and is deasserted with the last CRC byte transmission.

6.4.4 Terminating Transmission

A specific frame transmission is terminated under any of the following conditions:

- **Normal**

  The frame has been transmitted successfully. After the last byte is serialized, the pad and CRC are optionally appended and transmitted, thus concluding frame transmission.

- **CRC error**

  The txerr signal was asserted during packet loading. The IXF1002 infects the CRC it is building and sends a bad CRC onto the network. A transmit error will be generated as well (terr assertion in GMII mode, or symbol error in GPCS mode).

- **Underflow**

  Transmit data is not ready when needed for transmission. The packet is terminated on the network with a bad CRC and transmit error generation (terr assertion in GMII mode, or symbol error in GPCS mode).

6.4.5 Flow Control

The IXF1002 supports the standard flow control defined in the IEEE 802.3 Standard, enabling the stopping of remote node transmissions. Upon triggering, the IXF1002 sends a flow-control frame in the following format:

	Destination Address	Source Address	Type	Op-Code	Pause Time	Padding	FCS
Byte Count	6	6	2	2	2	42	4
Value (Canonic Form)	01-80-C2-00-00-01	EA1-EA2-..-EA6	88-08	00-01	PT1-PT2		

The source address field (EA1 – EA6) is taken from the MAC_ADD register.

The IXF1002 supports all combinations of symmetric or asymmetric flow-control function. Upon assertion of the flct_{i} signal or setting of the flow-control trigger bit (SER_COM<FCT>), a flow-control frame is sent with the pause time field (PT1 – PT2) equal to the PAUSE_TIME register. Upon deassertion of the flct_{i} signal, another flow-control frame will be sent with the pause time field equal to zero, meaning that the remote node may resume transmission. If the XON mode is disabled (TX_RX_PARAM<XOND>), the flow-control frame will not be transmitted on deassertion. If a flow-control was triggered during transmission of another packet, the flow-control packet will be transmitted immediately after the packet currently being sent. If more than one flow-control packet is triggered during transmission, only the last one is considered.

6.4.5.1 Additional Flow-Control Mode

When the additional flow control is enabled (TX_RX_PARAM<ADFC=1>), the IXF1002 will send an additional flow-control packet if a flow-control packet was sent upon assertion of the flct_{i} signal, and while this signal was asserted, the link partner's pause time period was about to end.

This will cause the link partner to receive the additional flow-control packet before its pause time counting ends.

Note: This feature is operative only if XOND bit is equal to 0.

6.5 MAC Receive Operation

This section describes the detailed receive operation as supported by the IXF1002. Receive activities are registered into network management registers, which are accessible through the CPU port.

6.5.1 Receive Initiation

The IXF1002 continuously monitors the network when reception is enabled. When an activity is recognized, the IXF1002 starts to process the incoming data.

In the GMII mode, the IXF1002 detects activity when the data valid signal (dv{i}) asserts. In GPCS mode, the IXF1002 detects activity when the /S/ symbol appears. After detecting receive activity on the line, the IXF1002 starts to process the preamble bytes.

6.5.2 Preamble Processing

The IEEE 802.3 Standard allows a maximum size of 56 bits (7 bytes) for the preamble, while the IXF1002 allows any arbitrary preamble length. The IXF1002 checks for the start frame delimiter (SFD) byte. If the next byte of the preamble which is different from 1010 1010, is not 1010 1011, the frame will be discarded. In this case the IXF1002 waits until the network activity stops before monitoring the network activity for a new preamble.

The interpacket gap (IPG) between received frames should be at least 80-bit time.

6.5.3 Frame Decapsulation

While the frame is being assembled, the IXF1002 continues to monitor the line condition.

In the GMII mode, the IXF1002 detects the end of frame when the data valid signal (dv{i}) deasserts. In GPCS mode, the IXF1002 detects the end of the frame when the /T/ symbol appears. Reception terminates with a frame error if the frame is not a valid MAC frame (e.g. short, too long, no SFD), or if a receive error was detected during frame reception.

In the GMII mode, receive error is detected when the receive error signal (rerr{i}) asserts during frame reception. In GPCS mode, receive error is detected when a symbol error is detected. The IXF1002 refers to the last 4 bytes received as the CRC. It checks the CRC bytes of all received frames and reports all errors.

6.5.4 Terminating Reception

When reception terminates, the IXF1002 determines the status of the received frame and loads the status into the receive FIFO. The IXF1002 can report the following events at the end of frame reception:

- **Overflow**

  The IXF1002 receive FIFO is not emptied as rapidly as it is filled, and the frame data is lost. If the FIFO is already full when a new frame is received, it will not be loaded in the FIFO and the whole packet is lost.

- **CRC error**
  The 32-bit CRC, received with the frame, did not match the CRC calculated upon reception.
- **Receive error**
  An receive error was detected during frame reception.
- **Frame too short**
  A frame containing less than 64 bytes (including CRC) was received.
- **Frame too long**
  A frame containing more than the programmed maximum size (in PKT_MAX_SIZE register) was received.

6.5.5 Flow Control

The IXF1002 identifies standard flow-control frames during reception. If a flow-control frame is received and flow-control mode is enabled (TX_RX_PARAM<FLCE>), frame transmission will be stopped until expiration of the pause time. If flow-control frames are received during frame transmission, the frame will be completely transmitted on the line, and transmission will then stop. The IXF1002 identifies flow-control frames according to the field matching described in Table 13, and correctness of the CRC.

Table 13. Flow-Control Field Matching

	Byte Number	Value (Canonic Form)
Destination Address	1-6	01-80-C2-00-00-01
Type	13-14	88-08
Op-Code	15-16	00-01

The value of fields 17 – 18 in the frame indicates the transmit pause time, represented in units of slot times.

By default, flow-control frames are not loaded into the receive FIFO and are discarded following identification, unless the IXF1002 is programmed to pass them (TX_RX_ERR<PFLC>).

6.6 MAC Loopback Operations

The IXF1002 supports two loopback modes:

- Internal loopback
- External loopback

6.6.1 Internal Loopback Mode

The internal loopback mode enables verification of correct internal logic operation. In this mode, frames loaded in the transmit FIFO are transferred to the receive FIFO through the transmit logic and receive logic. In the internal loopback mode, the IXF1002 disconnects from the network. Frames are not transmitted onto the line, and frames received from the line are rejected.

In GPCS mode, the transmitted packets pass through the GPCS encoding and decoding logic, and the txd<7:0> signals are unpredictable.

6.6.2 External Loopback Mode

The external loopback mode enables verification that the logic up to the wire operates correctly. In GPSC mode, when setting the external loopback mode (MII_CTL<LPBK>), the ewrap_{i} signal will be asserted in order to cause the external logic to loop back frames from the transmit side to the receive side. In GPCS mode, the loopback will work properly even if the link detection signal (sd) is not asserted.

In GMII mode, external loopback mode could be enabled by programming the external logic PHY to loop back frames from the transmit side to the receive side.

6.7 GPCS Mode

In the GPCS mode (PORT_MODE<GPCS=1>), the 8B/10B PCS encoding and decoding is performed by the IXF1002. The functions implemented in this mode include:

- 8-bit to 10-bit encoding in the transmit path
- 10-bit to 8-bit decoding in the receive path
- Auto-Negotiation
- Start-of-packet delimiter (SOP) and end-of-packet delimiters (EOP) detection and generation
- Symbol error detection
- Link timer

In the GPCS mode, the GMII/GPCS port works as a GPCS port. Table 14 describes the GPCS port signal names and their appropriate functions.

Table 14. GPCS Port Signal Description (Sheet 1 of 2)

GPCS Signals	IEEE 802.3z Signals	I/O	Description
tclk	—	I	Input - 125 MHz clock for reference.
pmatclk_{i}	PMA_TX_CLK	O	125 MHz transmit clock, synchronizing the txd_{i}<9:0> signals.
rclk_{i}	PMA_RX_CLK0	I	The 62.5 MHhz recovered receive byte clock. Used to latch odd numbered bytes of the receive data.
pmarclk_{i}	PMA_RX_CLK1	I	The 62.5 MHz recovered receive byte clock. This clock is 180° out-of-phase with rclk_{i}, and is used to latch even numbered bytes of the receive data.
txd_{i}<9:0>	TX_CODE-GROUP	O	Transmit data lines, driving a symbol on each tclk cycle.
rxd_{i}<9:0>	RX_CODE-GROUP	I	Receive data lines, driving a symbol on each pmarclk_0 and pmarclk_1 positive edge.
lnk_{i}	—	O	Link signal, asserted by the IXF1002 when the GPCS logic detects a link to a remote node.
sd{i}	SIGNAL_DETECT	I	Signal detect, asserted by the PHY layer when it detects link connection to the remote mode.
act_{i}	—	O	Activity signal, asserted by the IXF1002 when it transmits a frame or is receiving a frame.

Table 14. GPCS Port Signal Description (Sheet 2 of 2)

GPCS Signals	IEEE 802.3z Signals	I/O	Description
ewrap_{i}	EWRAP	O	Enable Warp. When asserted to the PHY, it should loop the transmit serialized data to the receive section. This pin is controlled in the GMII management control register (MII_CTL<LPBK>).
lckref_l_{i}	LCK_REF	O	Lock to reference. When asserted, enables the PHY to lock its PLL to the 125 MHz reference clock. This pin is controlled by bit LCKE in the PORT_MODE register.
encdet_{i}	EN_CDET	O	Enable comma detect. When asserted, enables the PHY for comma detect and word resynchronization. When deasserted, the PHY will keep current word alignment and will not try to detect new commas.
comdet_{i}	COM_DET	I	Comma detect. An indication from the PHY layer that the data contains a valid comma character.

When operating in the GPCS mode, the IXF1002 encapsulates and decapsulates the frames according to the IEEE 802.3z 1000BASE-X standard.

During transmit, encapsulation is performed according to the following rules:

- The first byte of the preamble in the MAC frame is replaced with the /S/ symbol.
- All of the MAC frame data is encoded according to 8B/10B standard encoding.
- After the FCS byte of the MAC frame, the /T/R/R/ or /T/R/ symbol is inserted.
- An IDLE symbol /I/, is transmitted between frames.
- Transmit error generation is translated to illegal symbol generation.

During receive, decapsulation is performed according to the following rules:

- An /I/S/ symbol sequence will cause the internal data valid signal to be asserted (start of receive activity).
- The /S/ symbol is replaced by a preamble byte.
- All of the data symbol stream is decoded according to 10B/8B standard decoding.
- The /T/R/R/ or/T/R/ symbol sequence will cause the internal data valid signal to be deasserted (end of receive activity).

During receive, the IXF1002 expects the frame to start with the symbol sequence /I/S/ followed by the preamble. If an /I/S/ symbol sequence is not detected, the reception of the current frame is aborted (not received), and the IXF1002 waits until the network activity stops before monitoring the network activity for a new frame. During reception, the IXF1002 also checks symbol validity. If an invalid symbol is being received, or if the frame does not end with the /T/R/R/ or /T/R/ symbol sequence, the IXF1002 reports a receive error.

6.7.1 Synchronization

The IXF1002 implements the synchronization process as defined in IEEE 802.3z. The synchronization process is responsible for determining whether the underlying receive channel is ready for operation.

Every set of ten bits transferred onto the line are called a Code-group. Ordered set consist of either one, two, or four code-groups where the first code-group is a special code-group. The seven bit comma string is defined as either b'xxx0011111' (comma+) or b'xxx1100000' (comma-).

Code-group synchronization is acquired by the detection of three ordered sets, containing comma strings in their first code group without receiving invalid code-group errors in between these three ordered sets.

6.7.1.1 Comma detect

When the Physical Medium Attachment (PMA) sublayer, which is a part of the PHY, detects a comma within the incoming rx_bit stream, it may realign its current code-group boundary to that of the received comma. During reception of a comma, the comdet_{i} signal is asserted by the PHY. Detection of a comma is done by the PHY only when the encdet_{i} signal is asserted. Assertion of PORT_MODE<FXECD> bit, will cause the encdet_{i} signal to be continuously asserted. Deassertion of this bit will cause assertion of the encdet_{i} signal only during loss-of-synchronization mode.

6.7.2 Auto-Negotiation

The IXF1002 implements the Auto-Negotiation process as defined in IEEE 802.3z, including full support of next page exchange.

The Auto-Negotiation process provides the means to exchange configuration information between the local device and the link partner device, and to automatically configure both devices to maximum advantage of their abilities. The receive and transmit flow-control working mode, which is resolved by the priority resolution function of the Auto-Negotiation, will be reflected in the GPCS_STT register. (see Section 3.2.5.9).

The Auto-Negotiation process starts with no need of management interference. For restarting Auto-Negotiation with ability advertised values other than the default, updating should be done in AN_ADV register and then the MII_CTL<RESAN> bit, should be asserted. Disable Auto-Negotiation by deasserting MII_CTL<ANENBL> bit. This will immediately start data transmission and reception in the default mode.

7.0 Timing Diagrams

This section contains the IX Bus port and GMII/GPCS port timing diagrams.

Note: The signal naming below refers to the Full-64 IX Bus mode. Signal names should be changed in accordance to the bus mode as described in Section 4.1.1.1.

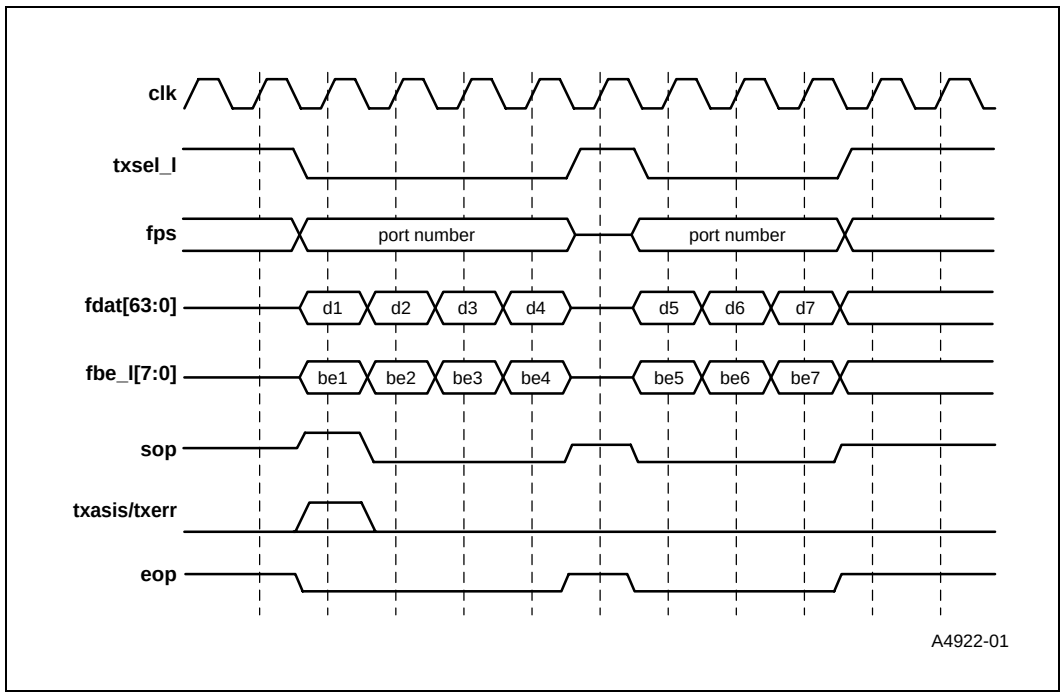
7.1 IX Bus Port Timing Diagrams

This section describes the IX Bus port timing diagrams.

7.1.1 Transmit Start-of-Packet Timing

Figure 18 shows the transmit start-of-packet timing.

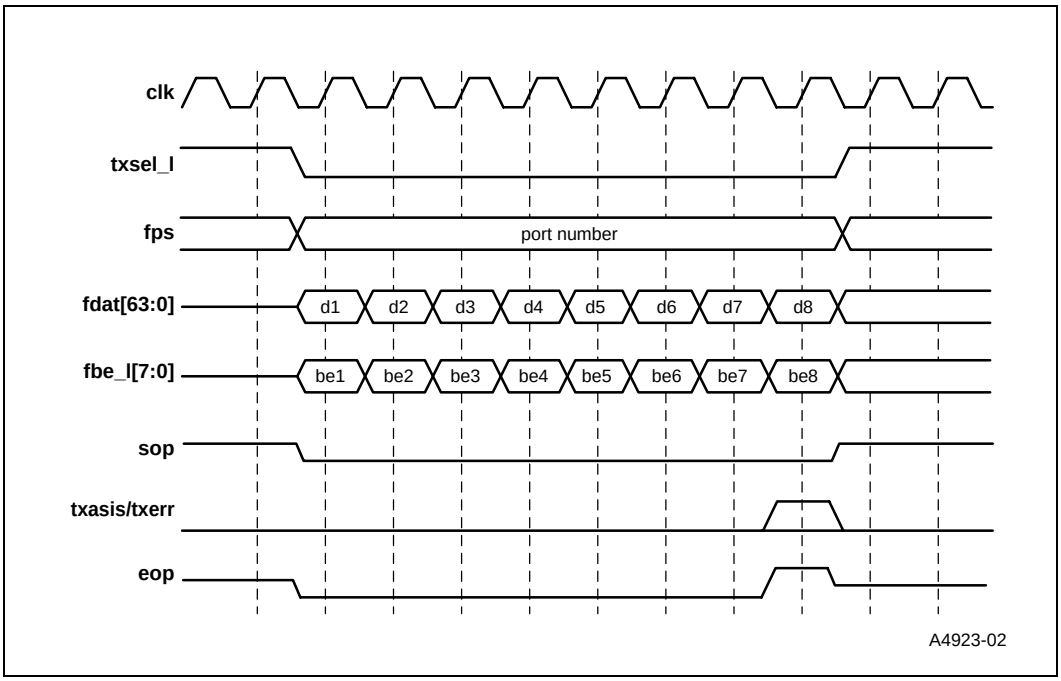
Figure 18. Transmit Start-of-Packet Timing



7.1.2 Transmit End-of-Packet Timing

Figure 19 shows the transmit end-of-packet timing.

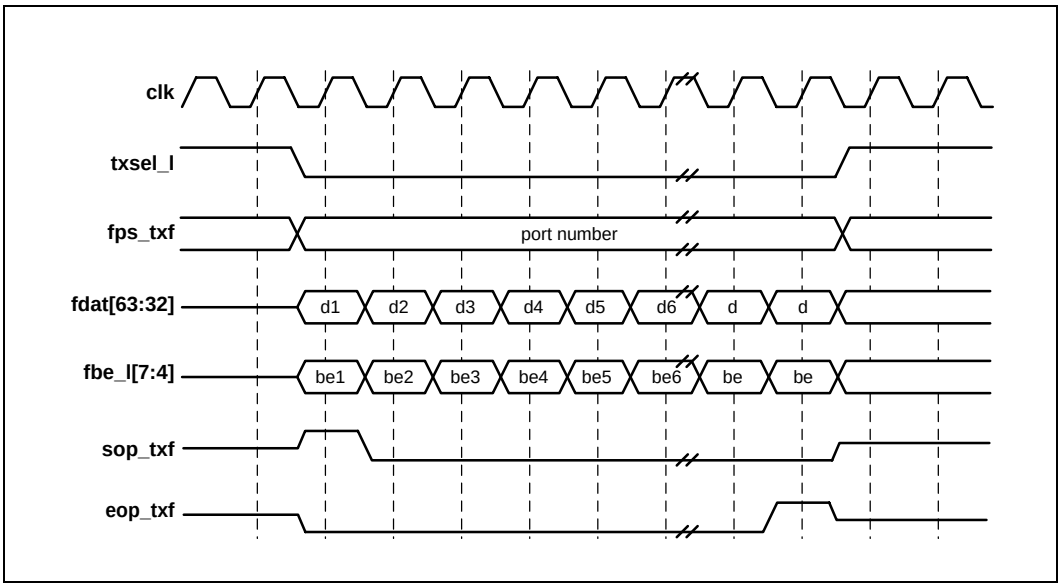
Figure 19. Transmit End-of-Packet Timing



7.1.3 Transmit Packet Timing in Split Mode

Figure 20 shows the transmit packet timing in the split mode.

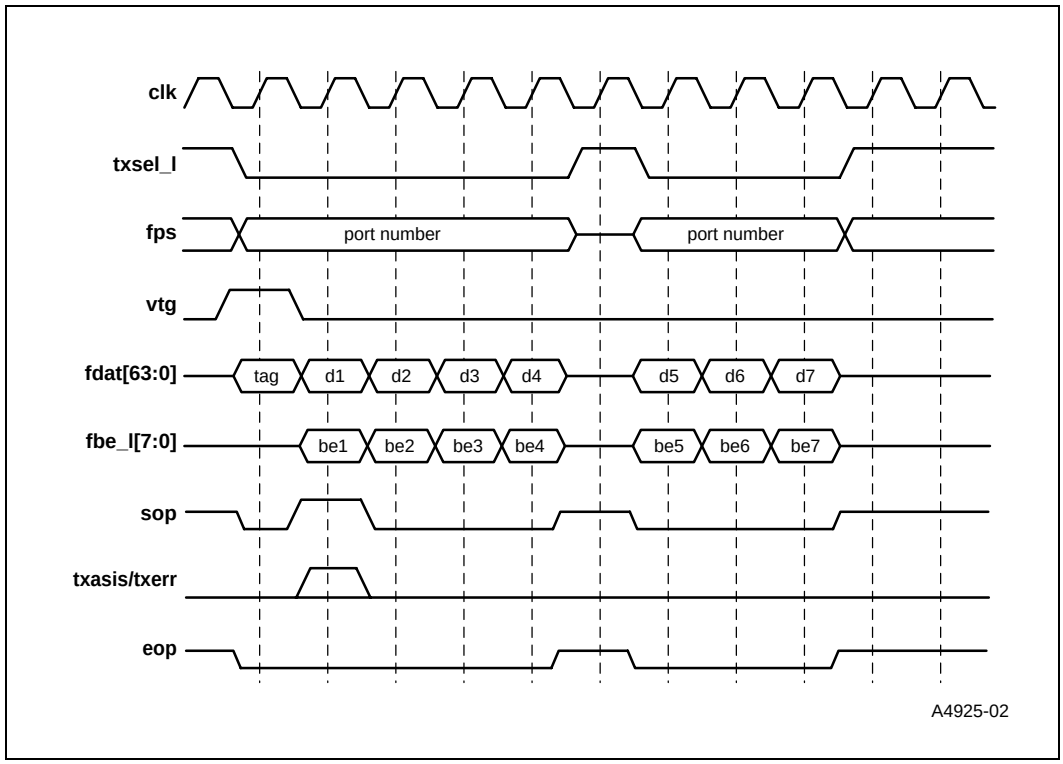
Figure 20. Transmit Packet Timing in Split Mode



7.1.4 Transmit Packet with VLAN Tag Append Timing

Figure 21 shows the transmit packet with VLAN tag append timing

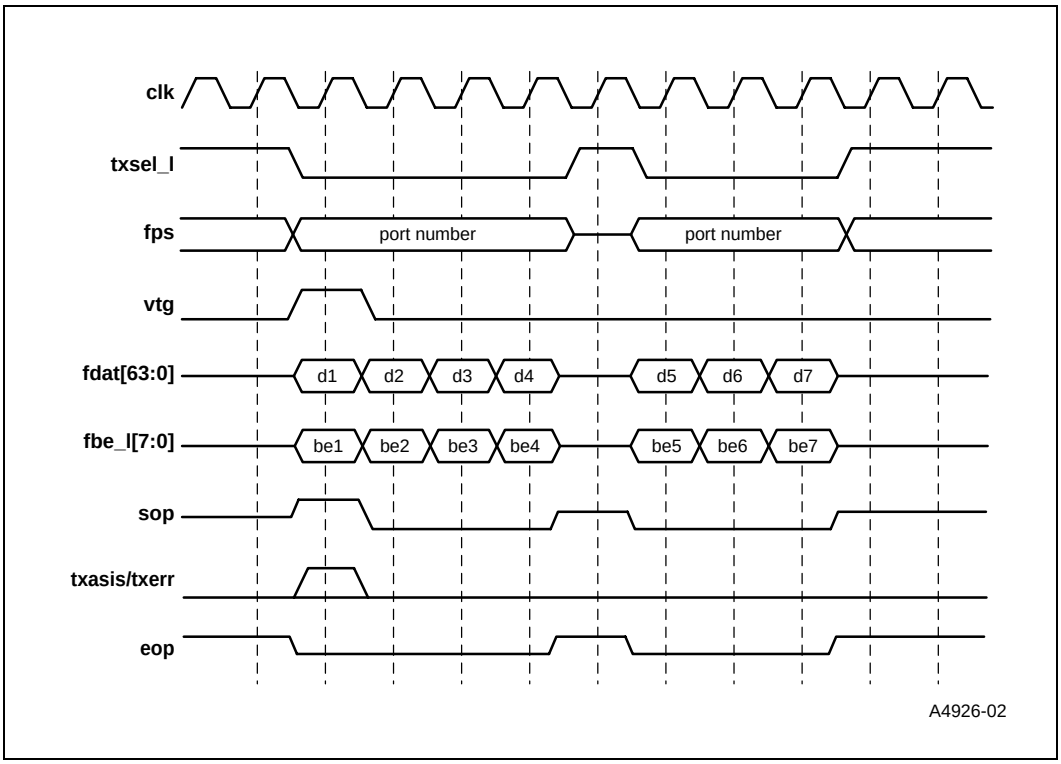
Figure 21. Transmit packet with VLAN Tag Append Timing



7.1.5 VLAN Strip Mode Timing

Figure 22 shows the transmit packet with VLAN tag strip timing

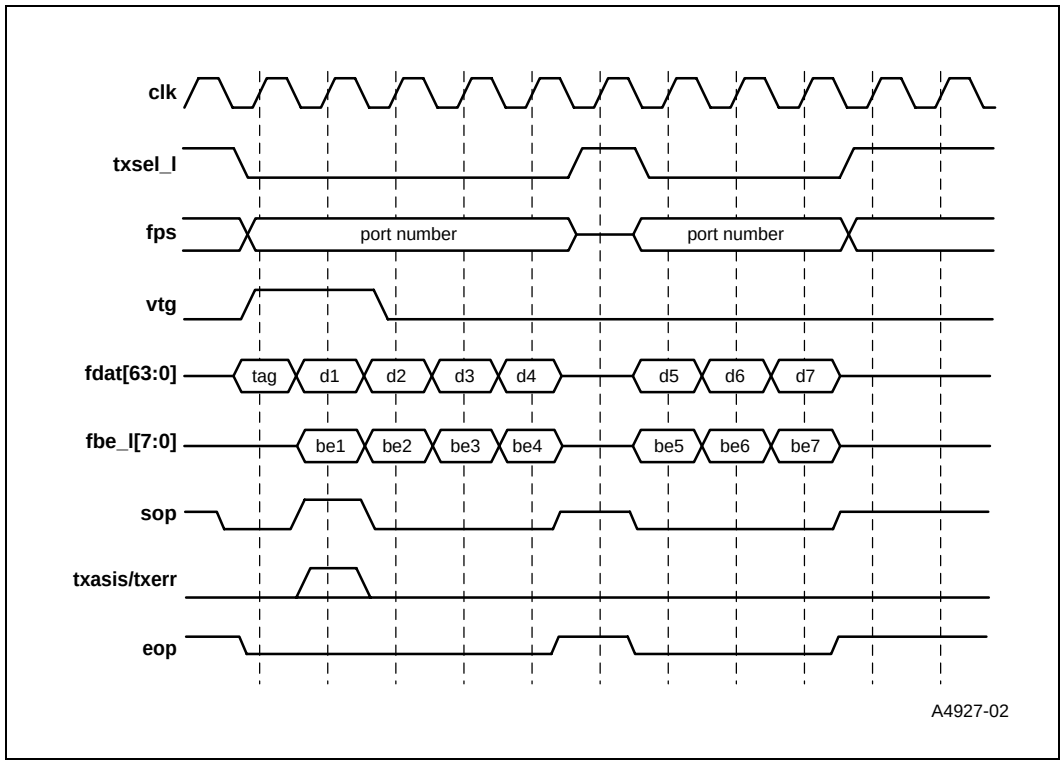
Figure 22. Transmit packet with VLAN Tag Strip Timing



7.1.6 Transmit Packet with VLAN Tag Replace Timing

Figure 23 shows the transmit packet with VLAN tag Replace timing

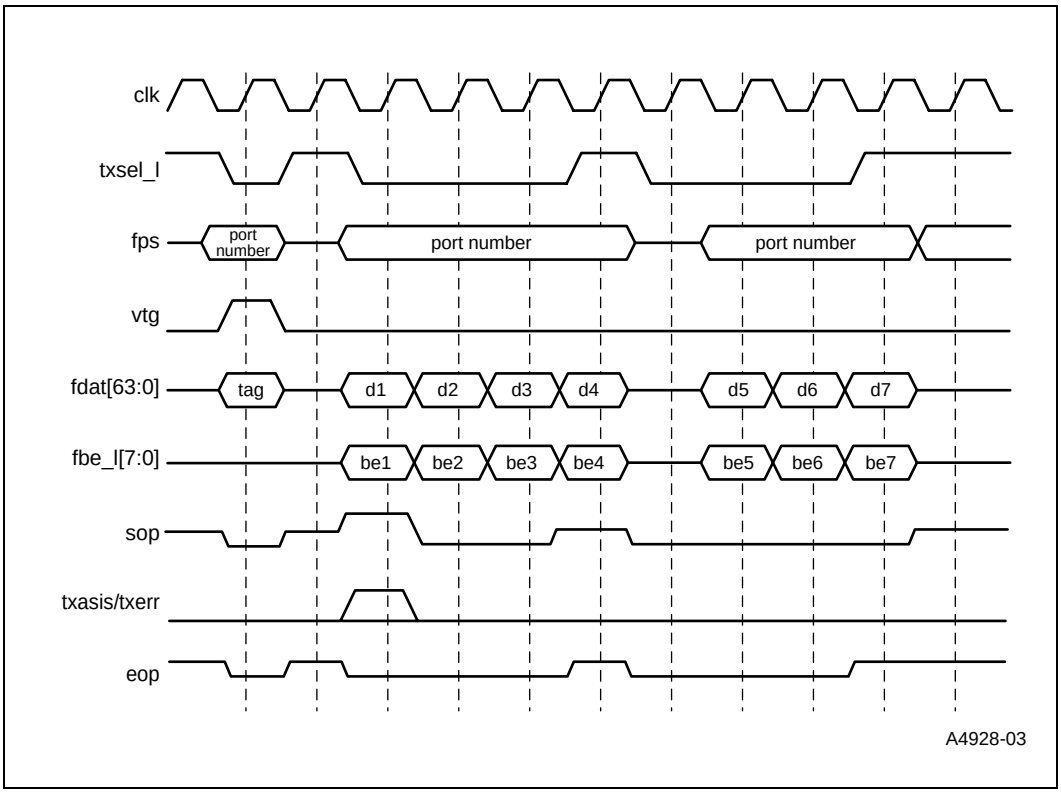
Figure 23. Transmit packet with VLAN Tag Replace Timing



7.1.7 VLAN Tag Append in Two txsel_l Bursts

Figure 24 shows the VLAN tag append in two txsel_l bursts timing.

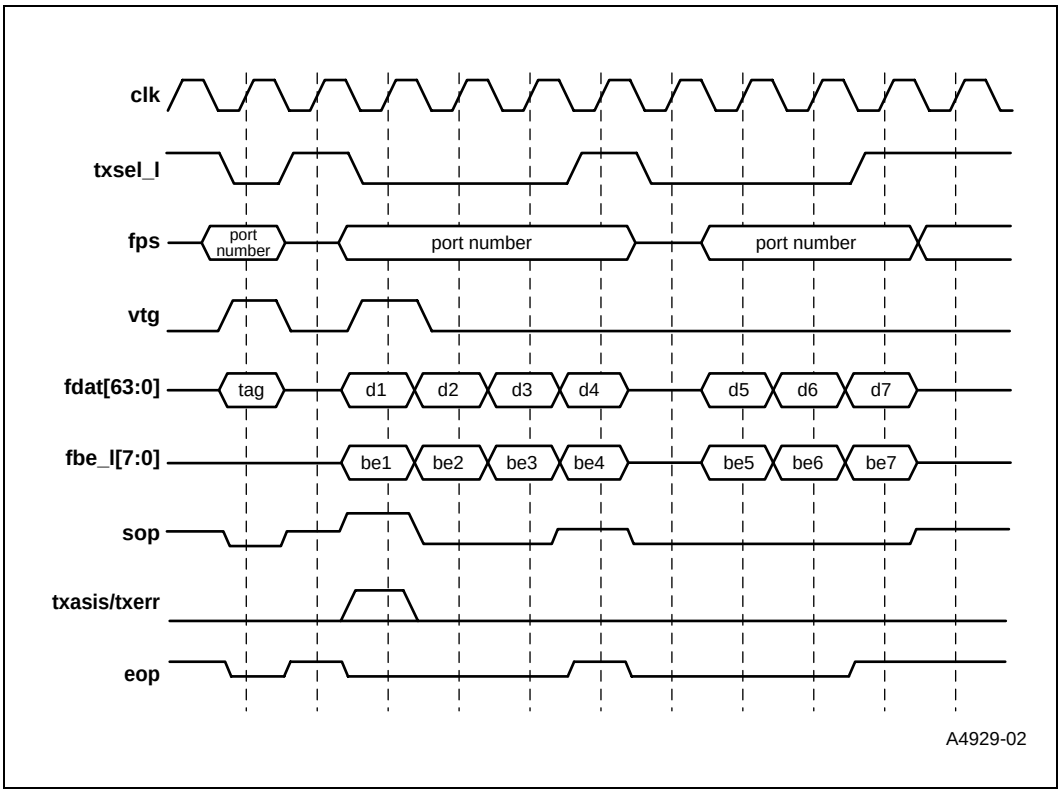
Figure 24. VLAN Tag Append in Two txsel_l Bursts Timing



7.1.8 VLAN Tag Replace in Two txsel_l Bursts

Figure 25 shows the VLAN tag replace in two txsel_l bursts timing.

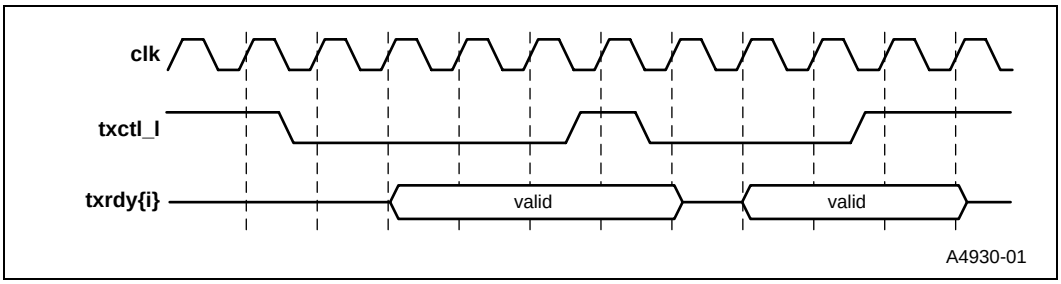
Figure 25. VLAN Tag Replace in Two txsel_l Bursts Timing



7.1.9 Transmit FIFO Control Timing

Figure 26 shows the transmit FIFO control timing.

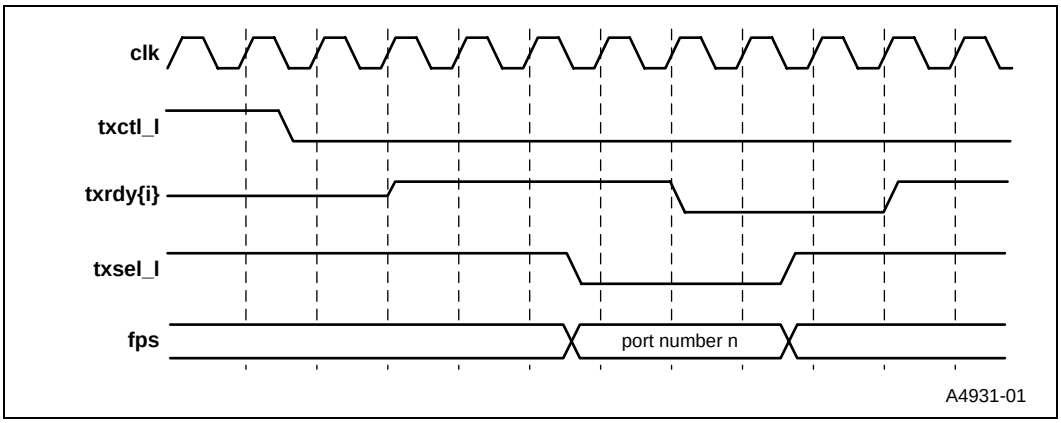
Figure 26. Transmit FIFO Control Timing



7.1.10 Transmit txrdy Timing

Figure 27 shows the transmit txrdy timing.

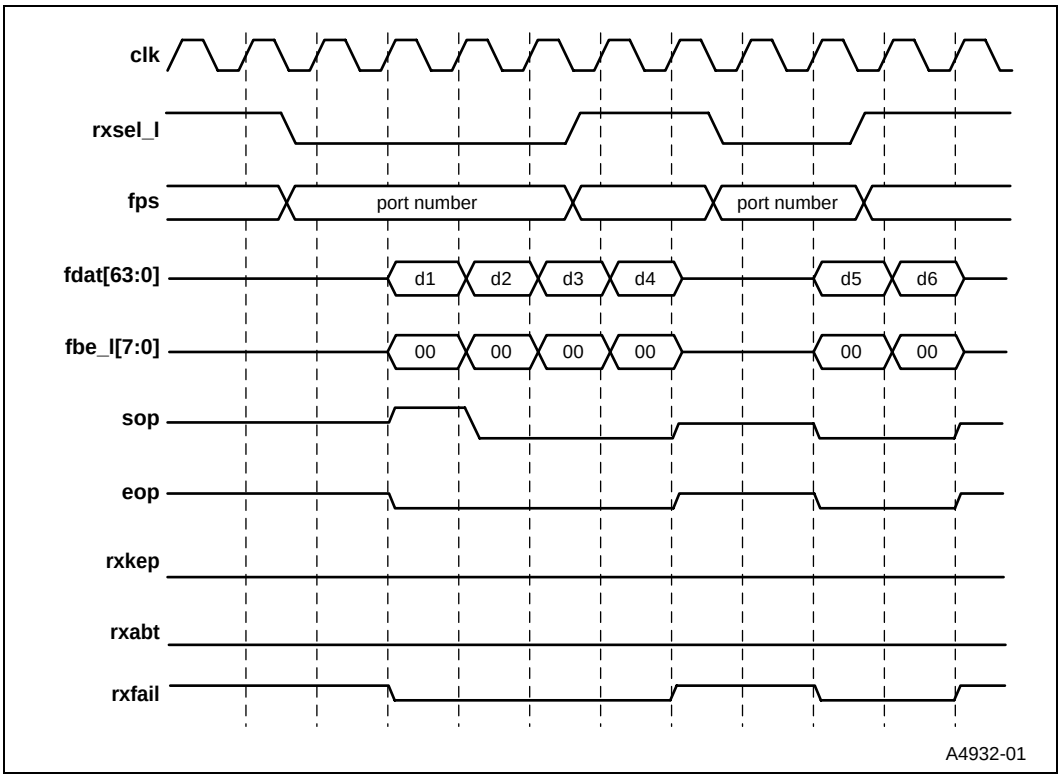
Figure 27. Transmit txrdy Timing



7.1.11 Receive Start-of-Packet Timing

Figure 28 shows receive start-of-packet timing.

Figure 28. Receive Start-of-Packet Timing

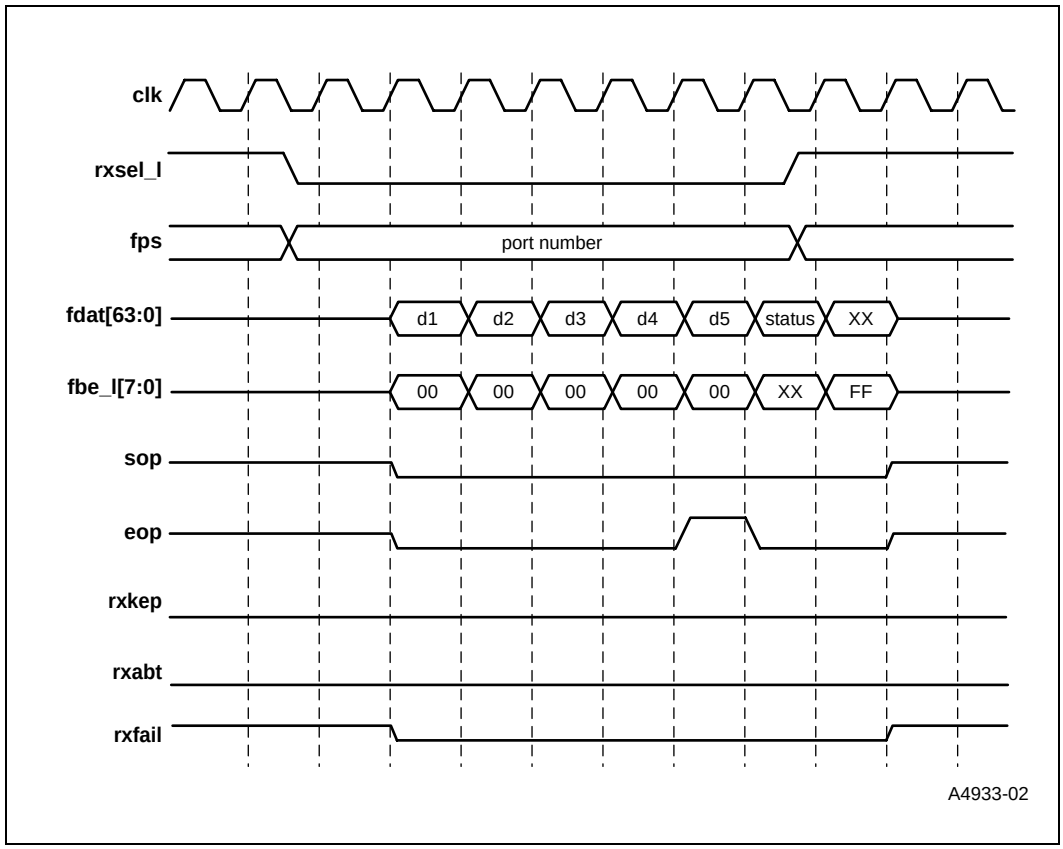


Note: rxsel_l must be deasserted for at least two cycles between two accesses to the same port.

7.1.12 Receive End-of-Packet Timing

Figure 29 shows the receive end-of-packet timing.

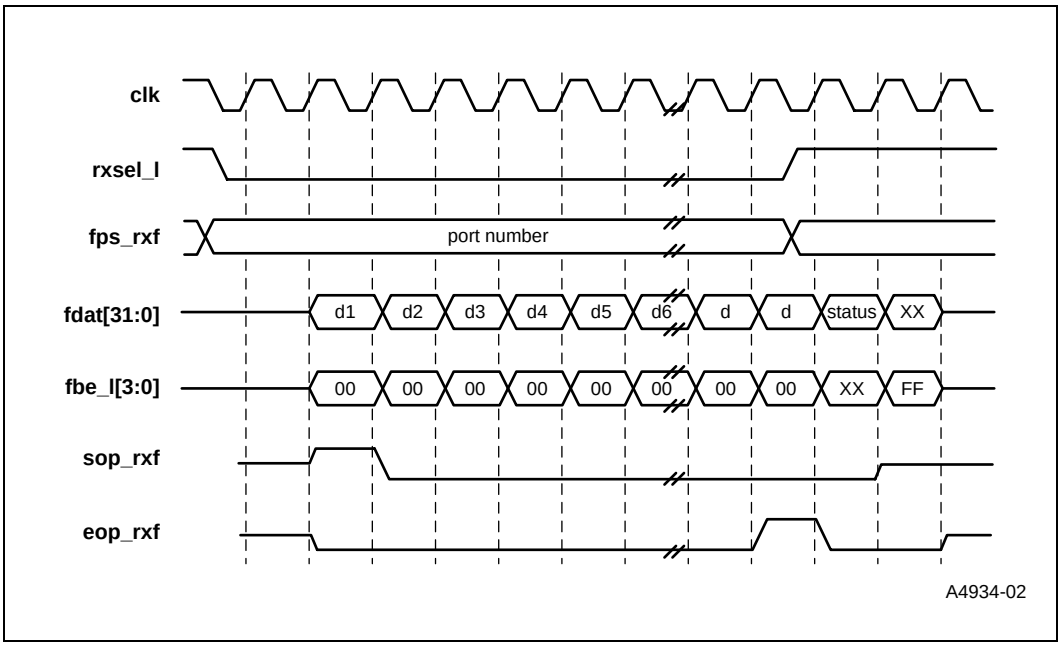
Figure 29. Receive End-of-Packet Timing



7.1.13 Receive Packet Timing in Split Mode

Figure 30 shows the receive packet timing in the split mode.

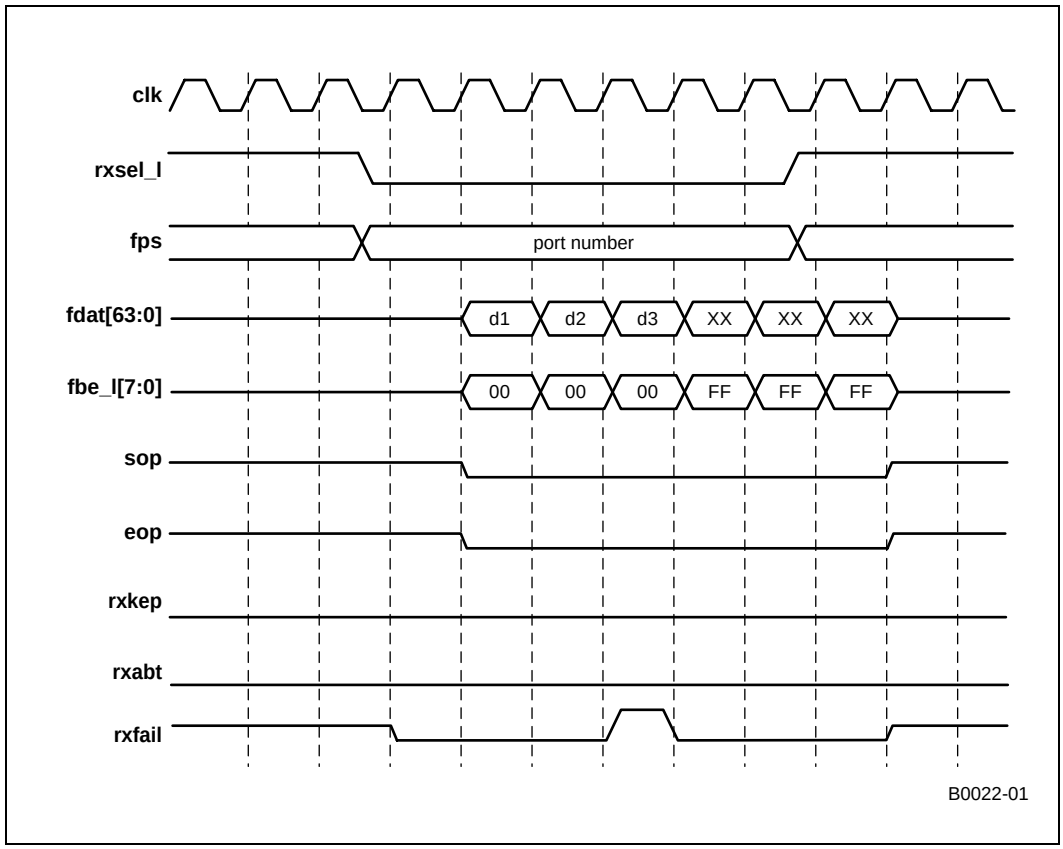
Figure 30. Receive Packet Timing in Split Mode



7.1.14 Receive rxfail Timing

Figure 31 shows the receive rxfail timing.

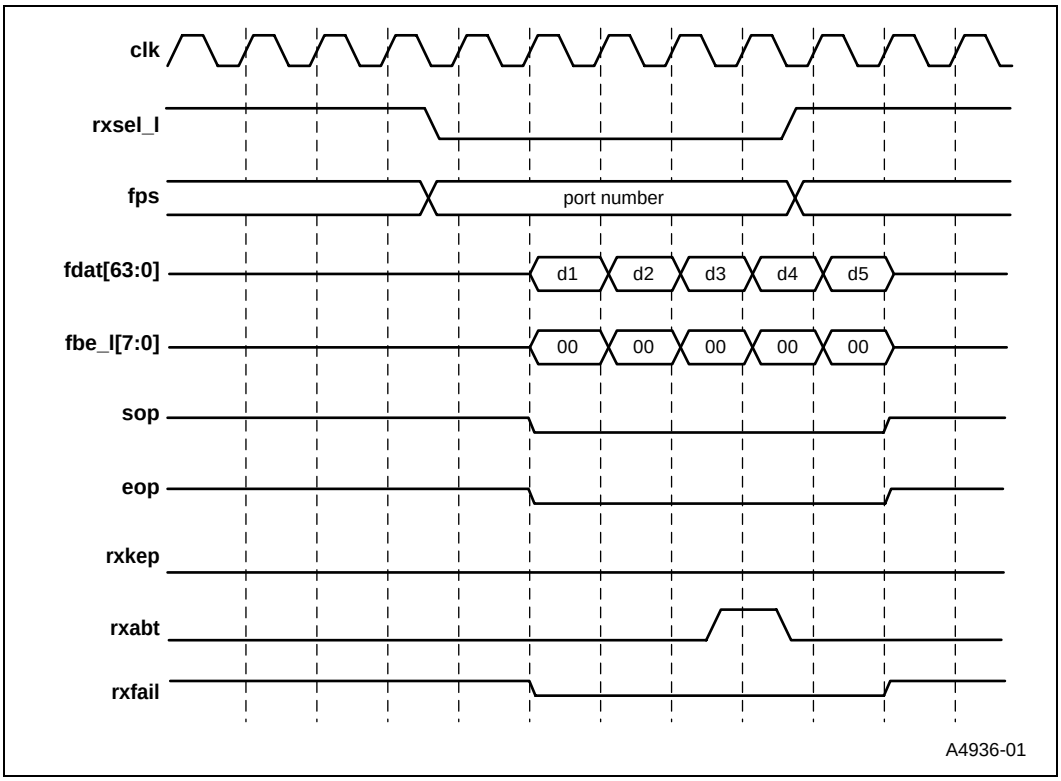
Figure 31. Receive rxfail Timing



7.1.15 Receive rxabt Timing

Figure 32 shows the receive rxabt timing.

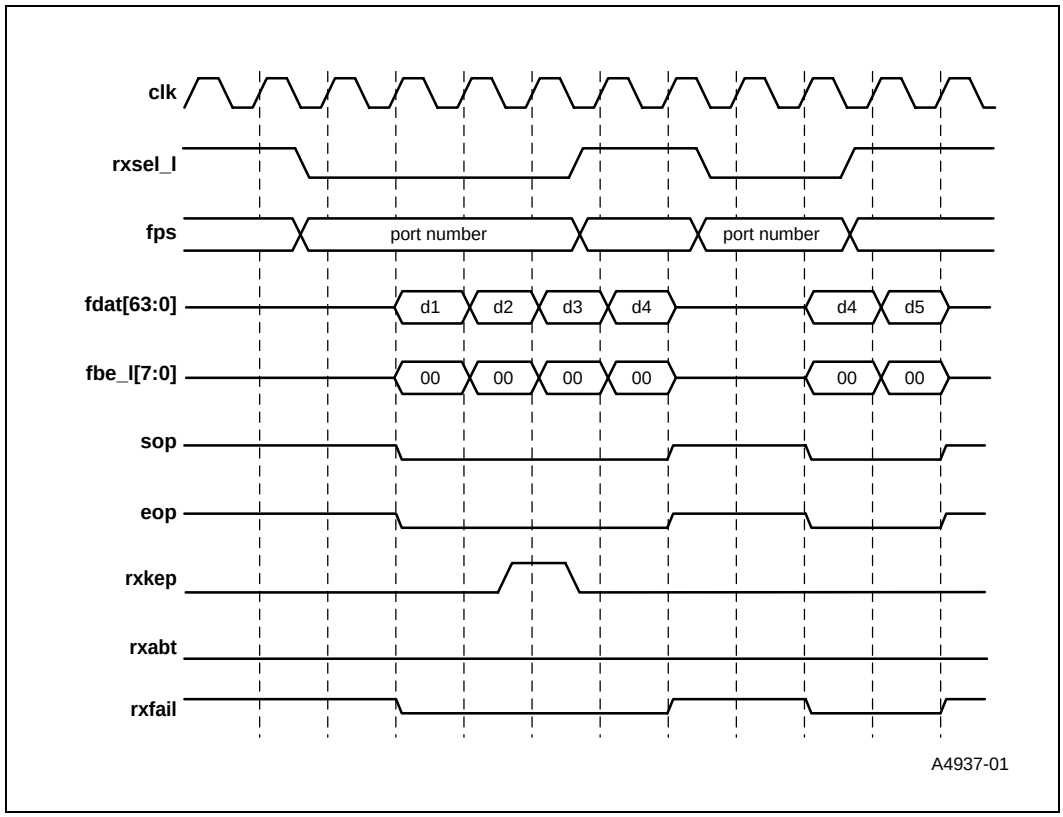
Figure 32. Receive rxabt Timing



7.1.16 Receive rxkep Timing

Figure 33 shows the receive rxkep timing.

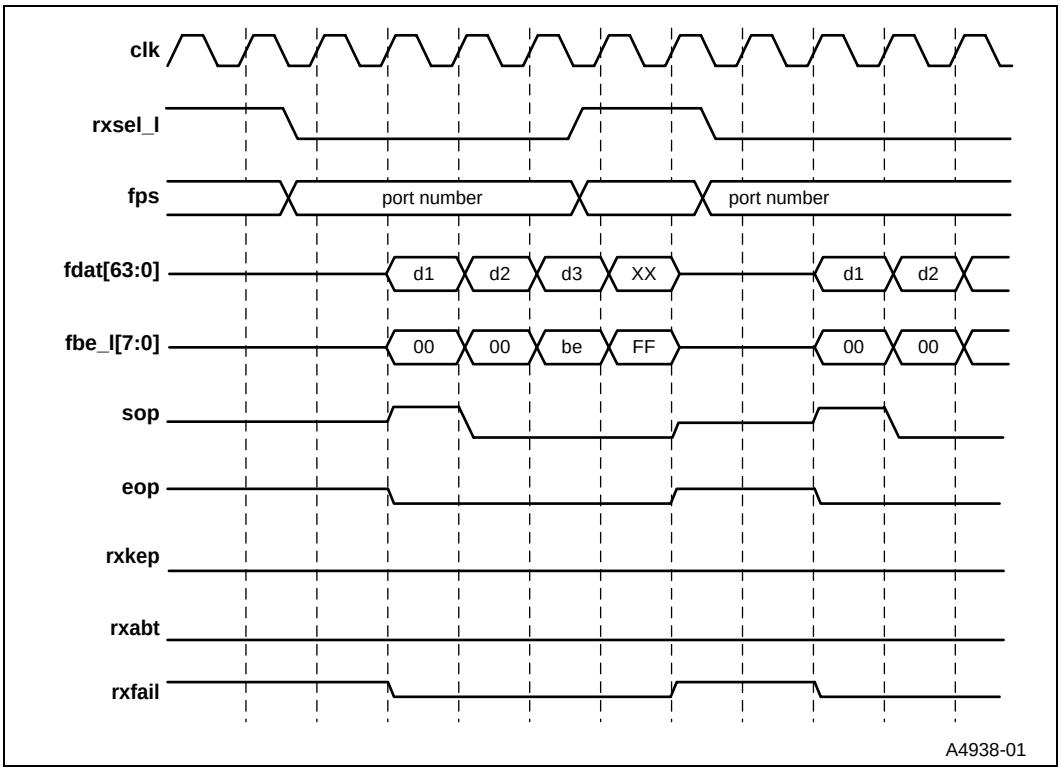
Figure 33. Receive rxkep Timing



7.1.17 Receive Header Replay Timing

Figure 34 shows the receive header replay timing (for 20 byte header, be=F0h).

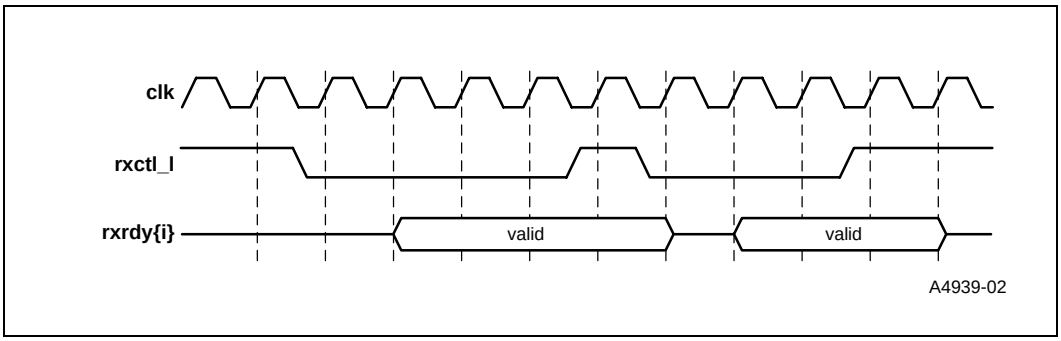
Figure 34. Receive Header Replay Timing



7.1.18 Receive FIFO Control Timing

Figure 35 shows the receive FIFO control timing.

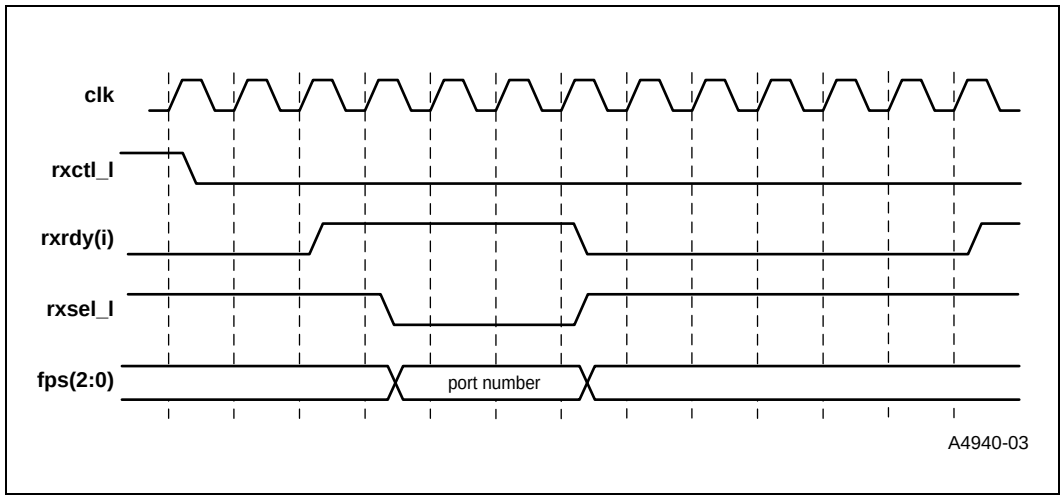
Figure 35. Receive FIFO Control Timing



7.1.19 Receive rxrdy Control Timing

Figure 36 shows the receive rxrdy control timing.

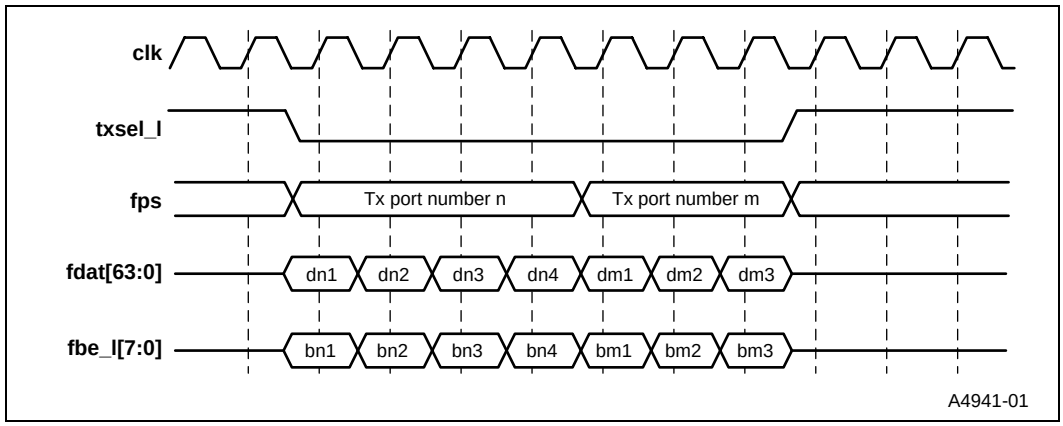
Figure 36. Receive rxrdy Timing



7.1.20 Consecutive Transmit-Transmit Timing

Figure 37 shows the consecutive transmit-transmit timing.

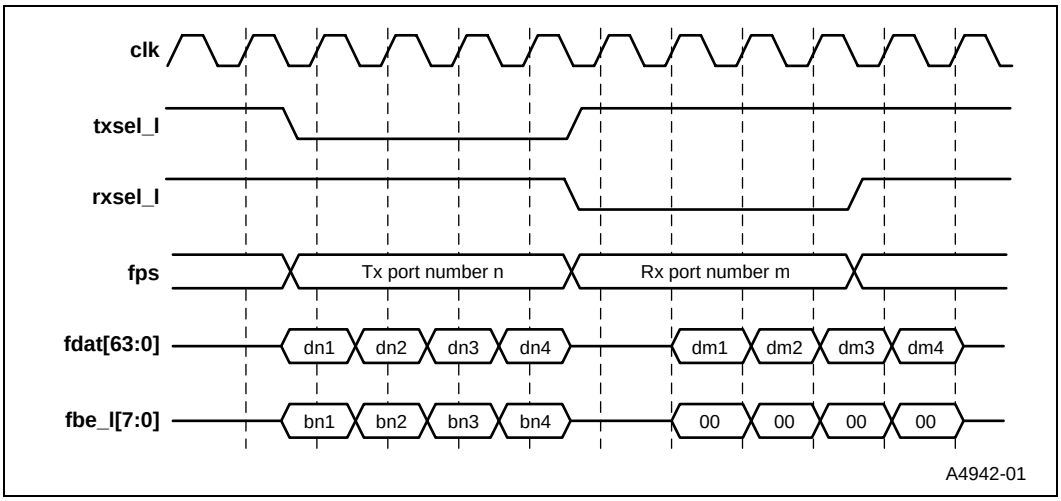
Figure 37. Consecutive Transmit-Transmit Timing



7.1.21 Consecutive Transmit-Receive Timing

Figure 38 shows the consecutive transmit-receive timing.

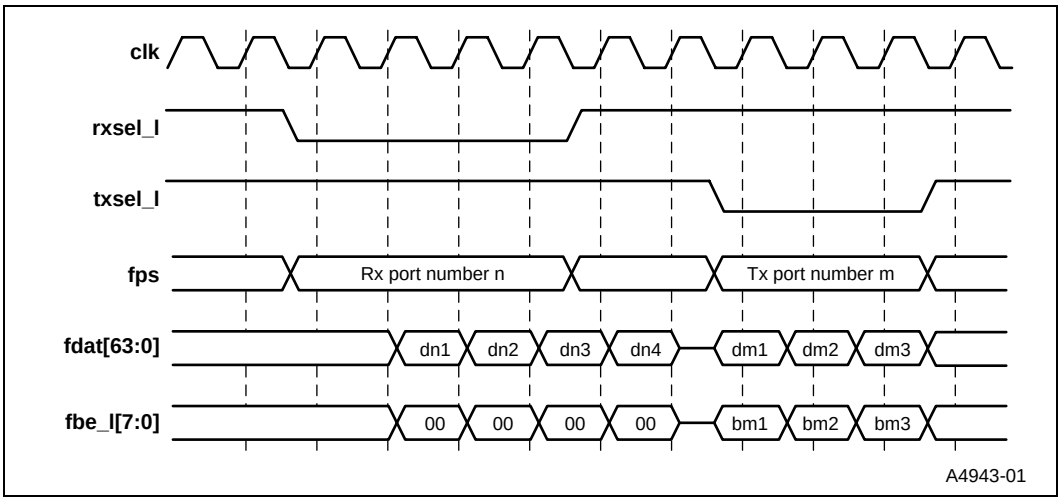
Figure 38. Consecutive Transmit-Receive Timing



7.1.22 Consecutive Receive-Transmit Timing

Figure 39 shows the consecutive receive-transmit timing.

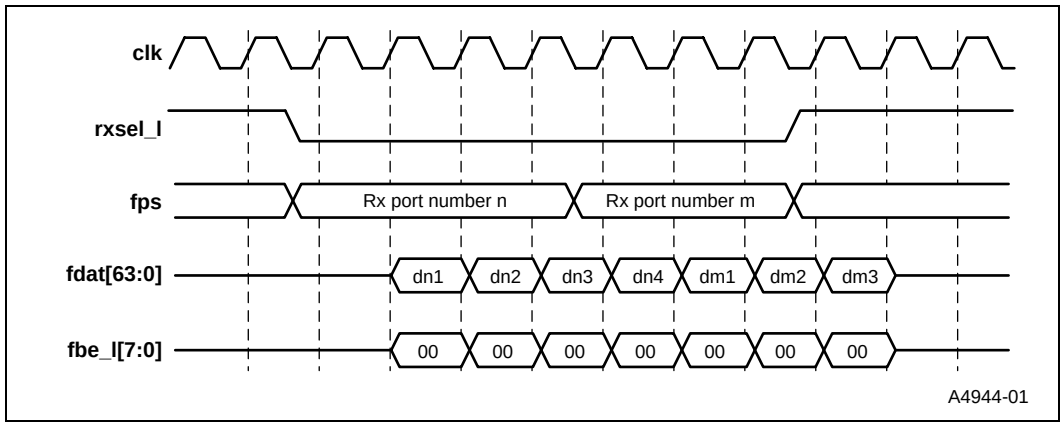
Figure 39. Consecutive Receive-Transmit Timing



7.1.23 Consecutive Receive-Receive Timing

Figure 40 shows the consecutive receive-receive timing.

Figure 40. Consecutive Receive-Receive Timing



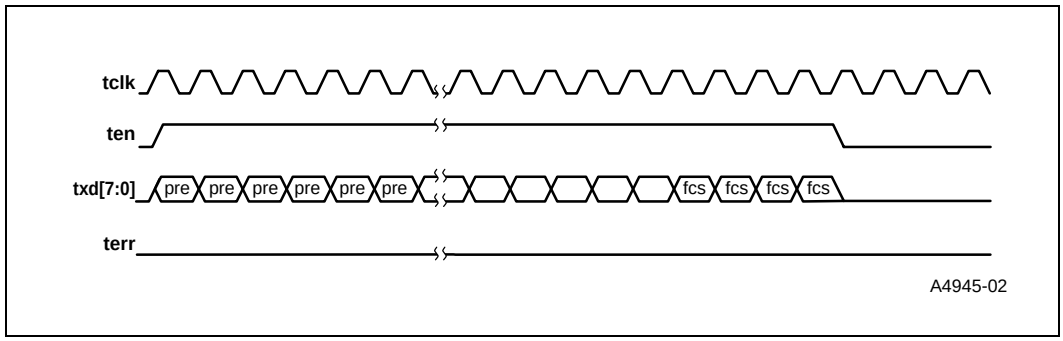
7.2 GMII/GPCS Port Timing Diagrams

This section shows the GMII/GPCS port timing diagrams. The GMII/GPCS port timing specification is compliant with the IEEE 802.3 Standard.

7.2.1 Packet Transmission Timing

Figure 41 shows the packet transmission timing.

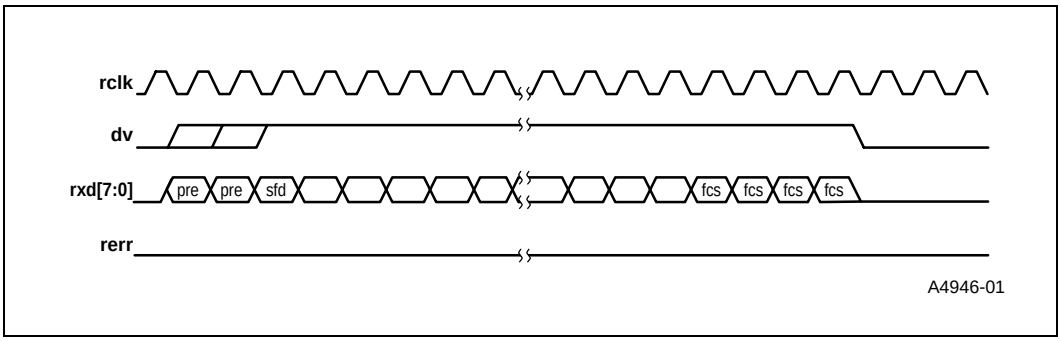
Figure 41. Packet Transmission Timing



7.2.2 Packet Reception Timing

Figure 42 shows the packet reception timing.

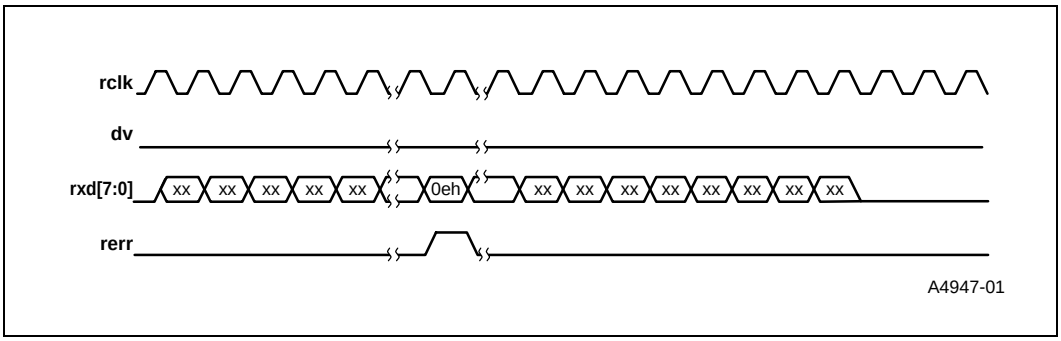
Figure 42. Packet Reception Timing



7.2.3 False Carrier Timing

Figure 43 shows the false carrier timing.

Figure 43. False Carrier Timing



8.0 Electrical and Environmental Specifications

This section contains the electrical and environmental specifications for the IXF1002. The IXF1002 supports both 5 V and 3.3 V signaling environments.

8.1 Functional Operating Range

Table 15 lists the functional operating range. Refer to Section 8.2 for details about the absolute maximum ratings.

Table 15. Functional Operating Range

Parameter	Minimum	Maximum
Power supply (Vdd)	3 V	3.6 V
Vdd_clmp (5.0 V signaling)	—	5 V
Vdd_clmp (3.3 V signaling)	3 V	Min. [3.6 V, (Vdd + 0.3 V)]
ESD protection voltage	—	2000 V Human Body Model (HBM)

8.2 Absolute Maximum Rating

Applying stresses beyond the absolute maximum may cause unrecoverable damage to the device. Operation of this product is not implied for any condition beyond the ranges specified in the functional operation range described in Section 8.1. Operating this product at the absolute maximum rating for a prolonged period can negatively impact device reliability. Table 16 lists the absolute maximum ratings for the IXF1002.

Table 16. Absolute Maximum Rating

Parameter	Maximum Rating
Supply voltage (Vdd)	3.9 V
Signal pins (Vsig)	5.5 V
Junction temperature, commercial (Tj)	125° C
Junction temperature, extended (Tj)	110° C

8.3 Supply Current and Power Dissipation

The values listed in Table 17 are based on a 80-MHz IX Bus clock frequency.

Table 17. Supply Current and Power Dissipation

Power Supply	Maximum Power
3.6 V	3.6 W

8.4 Temperature Limit Ratings

Table 18 lists the temperature limit ratings.

Table 18. Temperature Limit Ratings

Parameter	Minimum	Maximum
Storage temperature	–55°C	125°C
Operating temperature, commercial	0°C	70°C
Operating temperature, extended	–40°C	85°C

8.5 Reset Specification

The IXF1002 reset signal (reset_l) is an asynchronous signal that must be active for at least 10 IX Bus clock (clk) cycles with stable power.

8.6 FIFO Port Specifications

This section describes the FIFO port specifications.

8.6.1 Clock Specification

Figure 44 shows the IX Bus clock timing diagram.

Figure 44. IX Bus Clock Timing Diagram

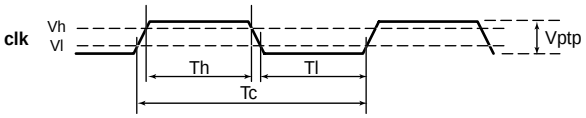


Figure 19 lists the specifications of the IX Bus clock.

Table 19. IX Bus Clock Timing Specifications

Symbol	Parameter	Condition	Minimum	Maximum
Freq	Clock frequency	—	33 MHz	85 MHz
Tc	Cycle time	—	11.75 ns	30.3 ns
Th	Clock high time	—	5 ns	—
Tl	Clock low time	—	5 ns	—
Vptp	Clock peak to peak (0.2 × Vdd to 0.6 × Vdd)	3.3 V clock	0.4 × Vdd	—
Vh	Clock high threshold	IX Bus @ 3.3 V	2.0 V	—
Vl	Clock low threshold	IX Bus @ 3.3 V	—	0.9 V
Vptp	Clock peak to peak (0.4 V to 2.4 V)	IX Bus @ 5 V	2 V	—
Vh	Clock high threshold	IX Bus @ 5 V	2 V	—
Vl	Clock low threshold	IX Bus @ 5 V	—	0.8 V

8.6.2 3 Volt DC Specifications

Table 20 lists the DC parameters for the IX Bus 3.3 V signaling levels.

Table 20. IX Bus 3.3 V Signaling Specifications

Symbol	Parameter	Condition	Minimum	Maximum
Vih	Input high voltage	—	2.0 V	Vdd_clmp + 0.5 V [1]
Vil	Input low voltage	—	–0.5 V [2]	0.9 V
Ii	Input leakage current	0 < Vin < Vdd	–15 µA	15 µA
Voh	Output high voltage	Iout = –4 mA	2.7 V	—
Vol	Output low voltage	Iout = +4 mA	—	0.36 V
Cin	Pin capacitance	—	5 pF	10 pF

1. Overvoltage protection maximum is +7.1 V for 11 ns, through a 29 Ω resistor.
2. Undervoltage protection maximum is -3.5 V for 11 ns, through a 28 Ω resistor.

8.6.3 5 Volt DC Specifications

Table 21 lists the dc parameters for the IX Bus 5 V signaling levels.

Table 21. IX Bus 5 V Signaling Specifications

Symbol	Parameter	Condition	Minimum	Maximum
Vih	Input high voltage	—	2.0 V	Vdd_clmp + 0.5 V[1]
Vil	Input low voltage	—	–0.5 V [2]	0.9 V
Ii	Input leakage current	0.5 V < Vin < 2.7 V	–15 µA[3]	15 µA
Voh	Output high voltage	Iout = –4 mA	2.4 V	—
Vol	Output low voltage	Iout = +4 mA	—	0.55 V
Cin	Pin capacitance	—	5 pF	10 pF

1. Overvoltage protection maximum is +11 V for 11 ns, through a 55 Ω resistor.
2. Undervoltage protection maximum is -5.5 V for 11 ns, through a 25 Ω resistor.
3. The minimum input leakage current for CDAT is -500 µA.

8.6.4 IX Bus Signals Timing

Figure 45 shows the IX Bus signals timing diagram.

Figure 45. IX Bus Signals Timing Diagram

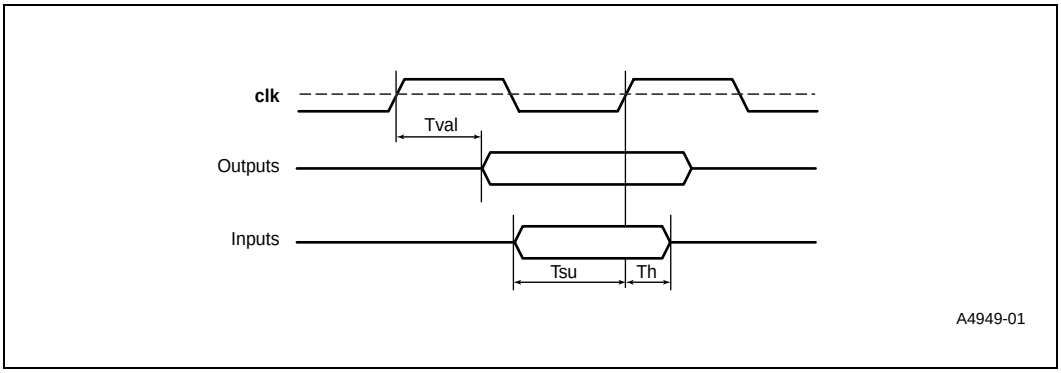


Table 22 lists the timing specifications of the IX Bus signals.

Table 22. IX Bus Signals Timing Specifications

Symbol	Parameter	Minimum (ns)	Maximum (ns)
Tval	Clock-to-signal valid delay Max Tval is measured with load of 10 pF	1	6
Tsu	Input signal valid setup time before clock	4	—
Th	Input signal hold time before clock, excluding Flow Control flct{i}	0	—
Th_flct	Flow Control input signal hold time before clock	1	—

8.7 CPU Port Specifications

This section describes the CPU port electrical specifications.

8.7.1 DC Specifications

Table 23 lists the CPU port DC specifications.

Table 23. CPU Port DC Specifications

Symbol	Parameter	Condition	Minimum	Maximum
Vih	Input high voltage	—	2 V	—
Vil	Input low voltage	—	—	0.8 V
Voh	Output high voltage	Ioh = –10 mA	2.4 V	—
Vol	Output low voltage	Iol = 10 mA	—	0.4 V
Ii	Input leakage current	—	–15 µA[1]	15 µA
Cin	Pin capacitance	—	5 pF	10 pF

1. The minimum input leakage current for CDAT is -500 µA.

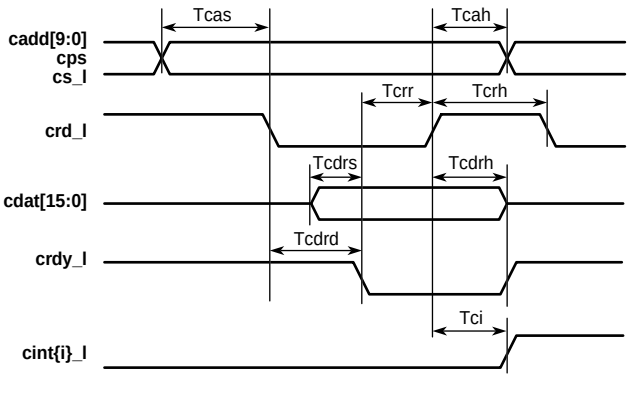
8.7.2 Signals Timing

This section describes the timing diagram of the CPU port.

8.7.2.1 Read Timing

Figure 46 shows the CPU port read timing diagram.

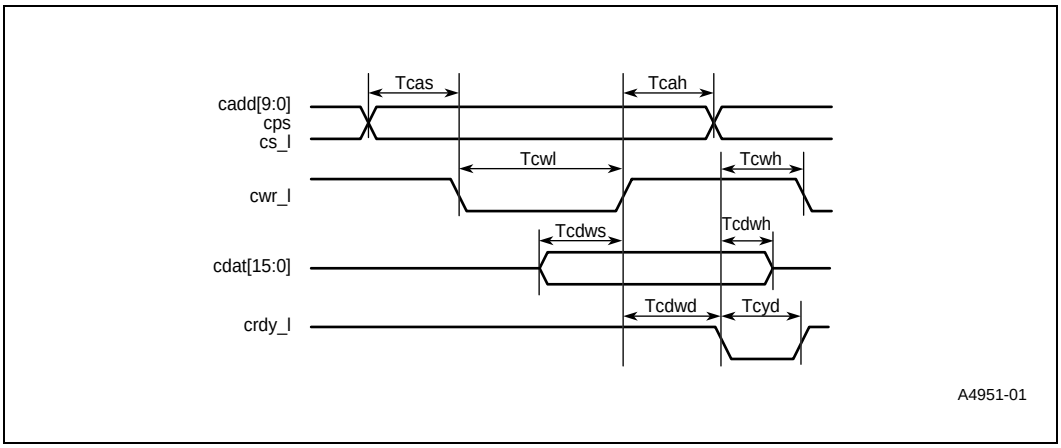
Figure 46. CPU Port Read Timing Diagram



8.7.2.2 Write Timing

Figure 47 shows the CPU port write timing diagram.

Figure 47. CPU Port Write Timing Diagram



8.7.2.3 Timing Parameters

Table 24 lists the CPU bus clock timing parameters.

Table 24. Timing Parameters

Symbol	Parameter	Minimum	Maximum
Tcas	cadd<9:0>, cps, cs_l setup time	10 ns	—
Tcah	cadd<9:0>, cps, cs_l hold time	10 ns	—
Tcrr	crdy_l assertion to crd_l deassertion	10 ns	—
Tcrh	crd_l high width	3 × TC [1]	—
Tcdrs	cdat<15:0> to crdy_l setup time	10 ns	—
Tcdrh	crd_l to cdat<15:0> hold time	TC	4 × TC
Tcdrd	Read cdat<15:0> driving delay	3 × TC	15 × TC
Tci	crd_l to cint_l clear delay	—	6 × TC
Tcwl	cwr_l width	5 × TC	—
Tcwh	crdy_l to cwr_l hold time	2 × TC	—
Tcdws	cdat<15:0> to cwr_l setup time	10 ns	—
Tcdwh	crdy_l to cdat<15:0> hold time	10 ns	—
Tcdwd	Write cdat<15:0> latching delay	1 × TC	4 × TC
Tcyd	crdy_l width in write cycle	3 × TC	5 × TC
Trtw	Read crdy_l deassertion to cwr_l assertion	4 × TC	—
Twtr	Write crdy_l deassertion to crd_l assertion	4 × TC	—

1. TC is the IX Bus clock cycle time.

8.8 GMII/GPCS Port Specifications

The GMII/GPCS port electrical specifications are compliant with the IEEE 802.3z standard.

8.8.1 DC Specifications

Table 25 lists the GMII/GPCS port dc specifications.

Table 25. GMII/GPCS Port DC Specifications

Symbol	Parameter	Condition	Minimum	Maximum
Vih	Input high voltage	—	2 V	—
Vil	Input low voltage	—	-0.5 V	0.8 V
Voh	Output high voltage	Ioh = –10 mA	2.1 V	3.6 V
Vol	Output low voltage	Iol = 10 mA	0 V	0.5 V
Ii	Input leakage current	—	–15 µA	15 µA
Cin	Pin capacitance	—	5 pF	10 pF

8.8.2 Signals Timing

This section describes the timing diagram of the GMII/GPCS port.

8.8.2.1 Clocks Specifications

Figure 48 shows the GMII port clocks timing diagram.

Figure 48. GMII Clock Timing Diagram

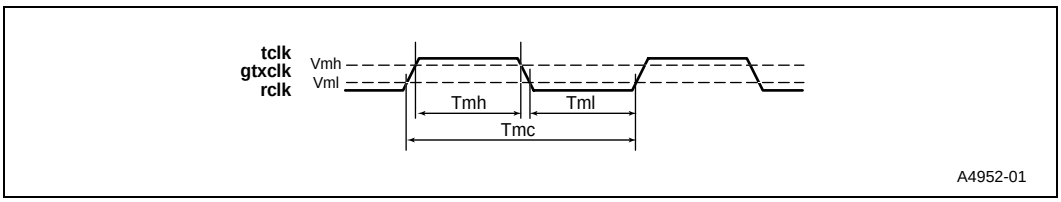


Figure 49 shows the GPCS port clocks timing diagram.

Figure 49. GPCS Transmit Clock Timing Diagram

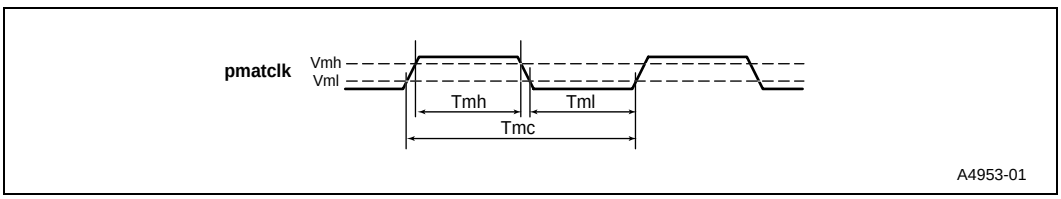


Figure 50 shows the GPCS receive clock timing diagram.

Figure 50. GPCS Receive Clock Timing Diagram

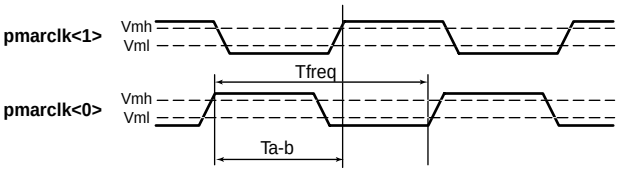


Table 26 lists the GMII/GPCS port signals timing specifications.

Table 26. GMII/GPCS Port Signals Timing Specifications

Symbol	Parameter	Minimum	Maximum
Tmc	tclk, gtxclk, rclk cycle time	8ns -100ppm	8ns +100ppm
Tmh	tclk, gtxclk, rclk high time	0.4 × Tmc	0.6 × Tmc
Tml	tclk, gtxclk, rclk low time	0.4 × Tmc	0.6 × Tmc
Vmh	tclk, gtxclk, rclk high threshold	2 V	—
Vml	tclk, gtxclk, rclk low threshold	—	0.8 V
Tfreq	pmarclk frequency	16 ns -100ppm	16 ns +100ppm
Tdrift	pmarclk drift rate	0.2 µs/MHz	—
Tduty	pmarclk duty cycle	0.4xTfreq	0.6xTfreq
Ta-b	pmarclk skew	7.5 ns	8.5 ns

8.8.2.2 GMII Signals Timing Diagrams

Figure 51 shows the GMII port transmit timing characteristics.

Figure 51. GMII Port Transmit Timing Diagram

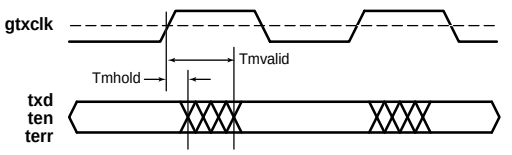
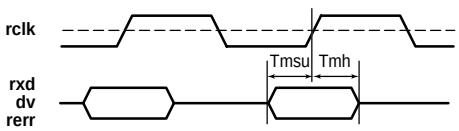


Figure 52 shows the GPCS interface receive timing diagram.

Figure 52. GMII Port Receive Timing Diagram



8.8.2.3 GMII Signals Timing Parameters

Table 27 describes the GMII signals timing parameters.

Table 27. Signals Timing Parameters

Symbol	Parameter	Minimum	Maximum
Tmhold	txd, terr, ten, output valid hold after rise of gtxclk	1.5 ns	—
Tmvalid	gtxclk to output valid delay	—	5 ns
Tmsu	Input setup time before rise of rclk	2 ns	—
Tmh	Input hold time after rise of rclk	0 ns	—

8.8.2.4 GPCS Signals Timing Diagrams

Figure 53 shows the GPCS port transmit timing characteristics.

Figure 53. GPCS Port Transmit Timing Diagram

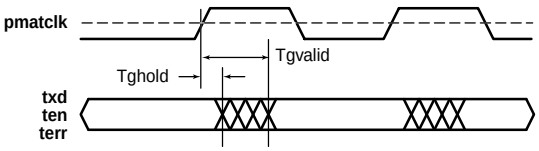
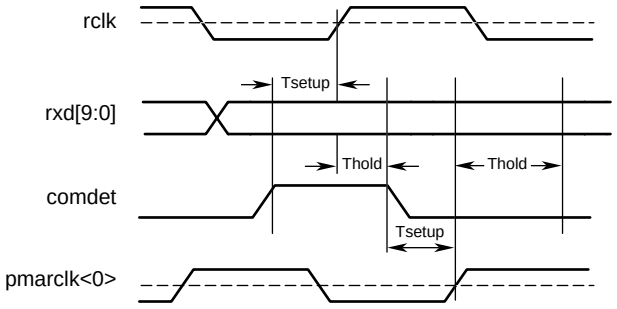


Figure 54 shows the GPCS interface receive timing diagram.

Figure 54. GPCS Receive Timing Diagram



8.8.2.5 GPCS Signals Timing Parameters

Table 28 describes the GPCS signals timing parameters.

Table 28. GPCS Signals Timing Parameters

Symbol	Parameter	Minimum	Maximum
Tghold	txd output valid hold after rise of pmatclk	1.5 ns	—
Tgvalid	Rise of pmatclk to output valid delay	—	5 ns
Tsetup	Data setup before rise of pmarclk	2 ns	—
Thold	Data hold after rise of pmarclk	0 ns	—

8.9 JTAG Port Specifications

This section describes the JTAG port electrical specifications.

8.9.1 DC Specifications

Table 29 lists the JTAG port dc specifications.

Table 29. JTAG Port DC specifications

Symbol	Parameter	Condition	Minimum	Maximum
Vih	Input high voltage	—	2 V	—
Vil	Input low voltage	—	—	0.8 V
Voh	Output high voltage	Ioh = –4 mA	2.4 V	—
Vol	Output low voltage	Iol = 4 mA	—	0.4 V
Ii	Input leakage current (tck)	—	–20 µA	20 µA
Iip	Input leakage current with internal pull-up (tdi, tms)	—	–1500 µA	20 µA
Io	Tristate output leakage current (tdo)	—	–20 µA	20 µA
Cin	Pin capacitance	—	5 pF	10 pF

8.9.2 Signals Timing

Figure 55 shows the JTAG port timing characteristics.

Figure 55. JTAG Port Timing Diagram

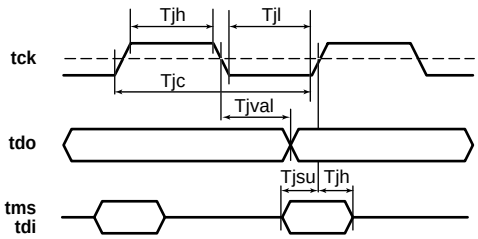


Table 30 lists the JTAG port timing specifications.

Table 30. JTAG Port Timing Specifications

Symbol	Parameter	Minimum	Maximum
Tjc	tck cycle time	90 ns	—
Tjh	tck high time	0.4 × Tjc	0.6 × Tjc
Tjl	tck low time	0.4 × Tjc	0.6 × Tjc
Tjval	tck fall to tdo valid delay	—	25 ns
Tjsu	tms and tdi setup time before tck	20 ns	—
Tjh	tms and tdi hold time from tck	5 ns	—

9.0 Mechanical Specifications

The IXF1002 is contained in a 304-ESBGA package. Figure 56 shows the part marking.

Product Name	Stepping	Marketing Part Number	Notes
GCIXF1002ED	C0	832414	Multi-Packet Mode.
GCIXF1002EDT	C0	838953	Extended temperature version.

Figure 56. Part Marking

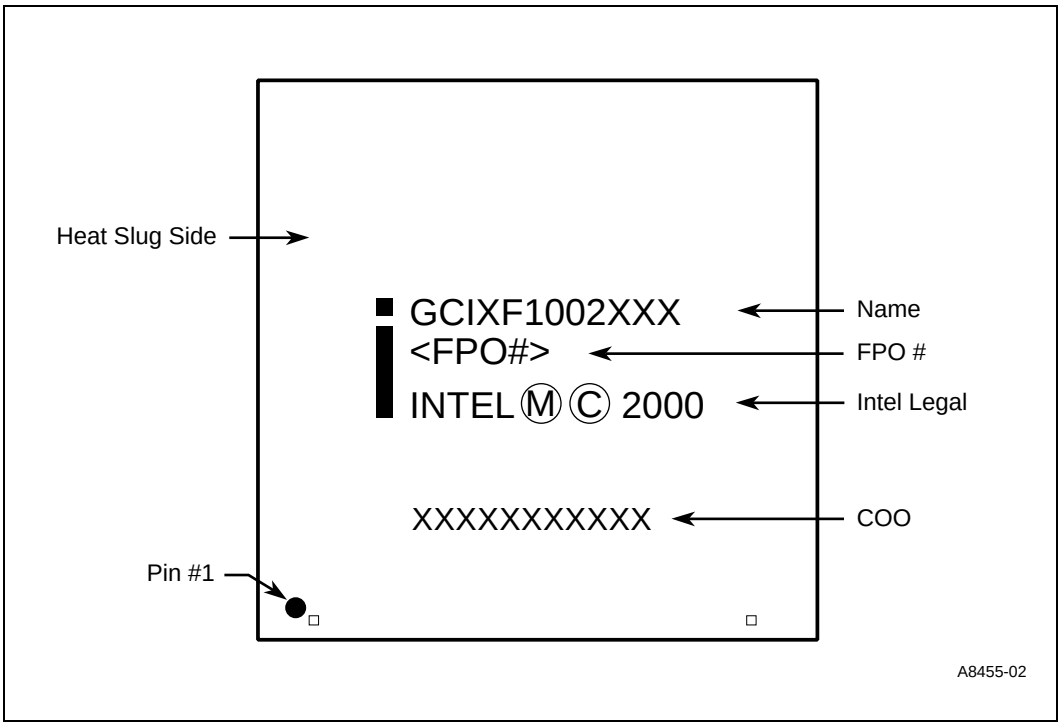


Figure 57 shows the 304-ESBGA package and Table 31 lists the dimensions in millimeters.

Figure 57. 304-ESBGA Package

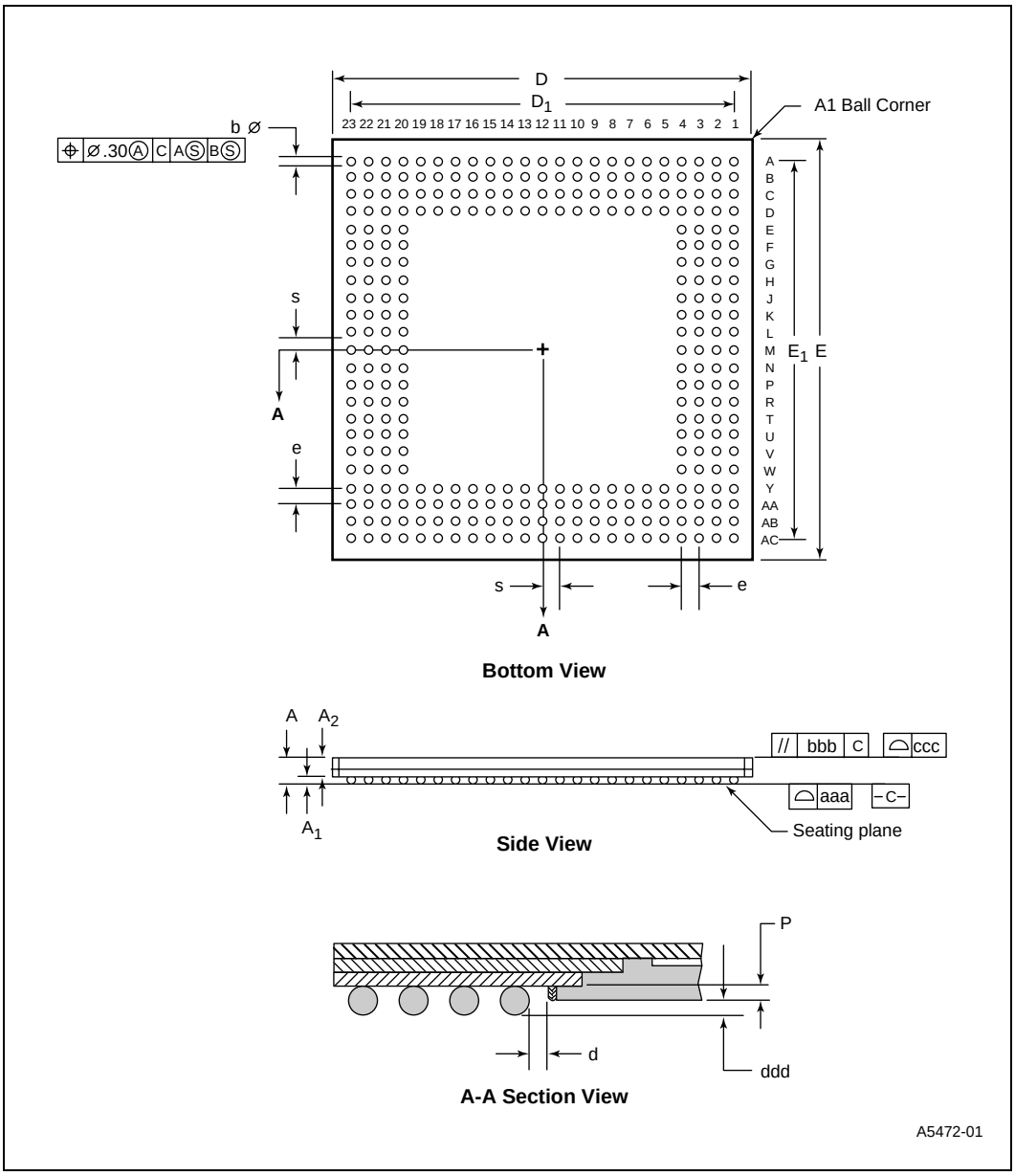


Table 31. 304-ESBGA Dimensional Attributes

Dimension	Symbol	Minimum	Nominal	Maximum
Package overall thickness	A	1.41	1.54	1.67
Ball height	A1	0.56	0.63	0.70
Body thickness	A2	0.85	0.91	0.97
Body size	E	30.90	31.00	31.10
Ball footprint	E1	27.84	27.94	28.04
Ball matrix	—	—	23 × 23	—
Number of rows deep	—	—	4	—
Ball diameter	b	0.60	0.75	0.90
Minimum distance encapsulation to balls	d	—	0.6	—
Ball pitch	e	—	1.27	—
Coplanarity	aaa	—	—	0.20
Parallel	bbb	—	—	0.15
Top flatness	ccc	—	—	0.20
Seating plane clearance	ddd	0.15	0.33	0.50
Encapsulation height	P	0.20	0.30	0.35
Solder ball placement	S	—	—	0.635

Joint Test Action Group – Test Logic A

This appendix describes the joint test action group (JTAG) test logic and the associated registers.

A.1 General Description

JTAG test logic supports testing, observation, and modification of circuit activity during normal operation of the components. The IXF1002 supports the IEEE Standard 1149.1 Test Access Port and Boundary Scan Architecture. The IXF1002 JTAG test logic allows boundary scan to be used to test both the device and the board it is installed in. The JTAG test logic consists of the following four signals to serially interface within the IXF1002:

- tck – JTAG clock
- tdi – Test data and instructions in
- tdo – Test data and instructions out
- tms – Test mode select

Note: If JTAG test logic is not used, the tck pin should be connected to “0”, and both the tms and tdi pins should be connected to “1”. The tdo signal should remain unconnected.

Note: If JTAG logic is used, a 1149.1 ring is created by connecting one device’s tdo pin to another device’s tdi pin and so on, to create a serial chain of devices. In this application, the IXF1002 receives the same tck and tms signals as the other devices. The entire 1149.1 ring is connected to either a motherboard test connector for test purposes or to a resident 1149.1 controller.

A.1.1 Test Access Port Controller

The test access port (TAP) controller interprets IEEE P1149.1 protocols received on the tms pin. The TAP controller generates clocks and control signals to control the operation of the test logic. The TAP controller consists of a state machine and a control dispatch logic. The IXF1002 fully implements the TAP state machine as described in the IEEE P1149.1 Standard.

A.2 Registers

In JTAG test logic, three registers are implemented in the IXF1002:

- Instruction register
- Bypass register
- Boundary-scan register

A.2.1 Instruction Register

The IXF1002 JTAG test logic instruction register is a 3-bit scan-type register that is used to program the JTAG machine to the appropriate operating mode. Its contents are interpreted as test instructions. Table A-1 lists the instructions register.

Table A-1. Instructions Register

IR<2>	IR<1>	IR<0>	Description
0	0	0	**EXTEST mode (mandatory instruction)**. Test data is shifted into the IXF1002 boundary-scan register and then transferred in parallel to the output pins.
0	0	1	**Sample-preload mode (mandatory instruction)**. Test data is loaded in parallel from the input pins into the IXF1002 boundary-scan register and then shifted out for examination.
0	1	0	RESERVED
0	1	1	RESERVED
1	0	0	RESERVED
1	0	1	**Tristate mode (optional instruction)**. Allows the IXF1002 to enter the power-saving mode. In this mode, all the port pads are tristated.
1	1	0	**Continuity mode (optional instruction)**. Allows the IXF1002 continuity test. In this mode, all the port pads get a “0” value.
1	1	1	**Bypass mode (mandatory instruction)**. Allows the test features on the IXF1002 test logic to be bypassed. Bypass mode is selected automatically when power is applied.

A.2.2 Bypass Register

The bypass register is a 1-bit shift register that provides a single-bit serial connection between the tdi and tdo signals. This register is used when the instruction register is set to bypass mode or after powerup.

A.2.3 Boundary-Scan Register

The boundary-scan register consists of cells located on all the pads. This register provides the ability to perform board-level interconnection tests by shifting data inside through tdi and outside through tdo. It also provides additional control and observation of the IXF1002 pins. For example, the IXF1002 boundary-scan register can observe the output enable control signals of the I/O pads.

Glossary B

B.1 List of Abbreviations

1000BASE-X	802.3z PHY specification for 100Mb/s 2 optical fibers or 2 pairs of specialized balanced cabling.
802.3	IEEE CSMA/CD LAN standard (Ethernet)
ESBGA	Ball Grid Array package
Mb/s	Mega bits per second
MHz	Mega Hertz
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check appended to Ethernet packets
FIFO	First In First Out memory
IEEE	Institute of Electrical and Electronics Engineers, Inc.
IP	Internet protocol
IPG	Interpacket Gap
JTAG	Join Test Action group
LAN	Local area Network
MAC	Media Access control
OD	Open Drain
SFD	Start Frame Delimiter
GMII	Gigabit Media Independent interface
GPCS	Gigabit Physical Coding Sublayer
PHY	Physical Layer Entity
RMON	Remote Network Monitoring Management
SNMP	Simple Network Management Protocol
VLAN	Virtual bridged LAN
WAN	Wide Area Network

Multi-Packet Mode C

C.1 Overview

This addendum contains the description of a new Multi-Packet Mode of operation introduced for the IXF1002 Dual Port Gigabit Ethernet Controller (GCIXF1002ED only).

C.2 Introduction - txrdy Assertion/Deassertion Rules

The IXF1002 uses a generic bus interface (IX Bus) for data transfer to and from its FIFOs. The Transmit FIFO (TFIFO) is accessed according to a port selection signal (fps) as well as a transmit enabling signal (txsel_l). When a data transfer occurs, it is synchronized to the main clock (clk), and new data may be sent on each clock cycle. The IXF1002 provides a dedicated signal (txrdy), which indicates that it is ready for data transfer into the TFIFO. The IXF1002 asserts the txrdy signal when both of the following criteria are met:

- The amount of free space in the TFIFO is greater than the predetermined FIFO transmit threshold (FFO_TSHD<TTH>).
- The number of full packets stored in the TFIFO is less than two.

When the txrdy signal is asserted, the transfer burst size should be shorter than or equal to the FIFO transmit threshold to ensure that there is adequate space in the TFIFO to store the data. The IXF1002 allows transferring of up to one packet in a single data transfer burst.

Packet transmission across the IX Bus should continue until the amount of data sent is equal to the FIFO transmit threshold or until the entire packet is transmitted into the TFIFO (i.e. EOP is reached).

The IXF1002 deasserts txrdy to indicate at least one of the following:

- The amount of free space in the TFIFO is below the FIFO transmit threshold (FFO_TSHD<TTH>)
- The number of full packets stored in the TFIFO is two
- A data burst across the IX Bus is in progress

The FIFO transmit threshold value should be carefully selected based on latency, IX Bus data transfer bandwidth, and frame sizes in order to avoid transmit underflow scenarios.

When a high serial transmit threshold value is programmed (TX_TSHD<TSD>), there may be scenarios and systems when the IXF1002 limits the system performance from reaching full wire speed bandwidth.This scenario mainly occurs when a small packet is transmitted between streams of large packets. The cause of this performance degradation is related to the two packet maximum in the TFIFO.

In order to overcome this problem, Multi-Packet Mode is introduced. In Multi-Packet Mode, the maximum number of complete packets that can be stored in the TFIFO is sixteen instead of two.

Note that when the IXF1002 is not in Multi-Packet Mode, the device retains all of the features as described in the IXF1002 Data Sheet.

C.3 Multi-Packet Mode

In order to enable systems that require a high serial transmit threshold to reach full wire speed operation, Multi-Packet Mode was introduced. When this mode is enabled (PORT_MODE<14:13> = 1), up to 16 full packets may be stored in the IXF1002's TFIFO.

In Multi-Packet Mode, txrdy signal deassertion rules are changed to indicate at least one of the following:

- The amount of free space in the TFIFO is below the FIFO transmit threshold (FFO_TSHD<TTH>).
- The number of full packets stored in the TFIFO is sixteen.
- A data burst across the IX Bus is in progress.

While working in Multi-Packet Mode, the following IXF1002 features are not supported:

- The ability to add, strip or change VLAN tags during packet transmission
- TFIFO packet count status information (TX_RX_STT<PKC>). Reading this register will give an incorrect value.
- Minimum packet sizes of less than 32 bytes on the IX Bus. Packets that have less than 32 bytes between SOP and EOP may corrupt previous and/or following packets.
- Single packet mode for the TFIFO (TX_RX_PARAM<SPM>).
- The functionality of txasis when asserted together with SOP (no padding and/or CRC appended to the packet even if the port was programmed to do so) at IX Bus frequencies below 50 MHz. Note
- that txasis functionality works as specified in the IXF1002 Data Sheet for frequencies of 50 MHz or higher.

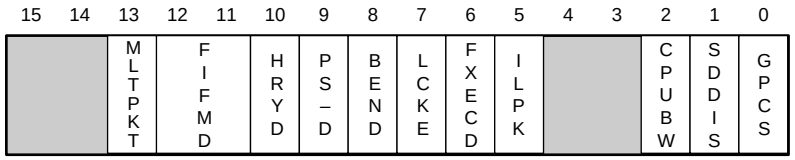
C.4 Port Working Mode Register

Mnemonic: PORT_MODE

Address: 24H – 25H

The port mode register controls the CPU bus, IX Bus, and serial interface modes of work.

Note: Bits 14, 13, 12, 11, 2, and 0 must have the same value in both ports.



Bit Name	Bit #	Bit Description
—	15	RESERVED
—	14	RESERVED Should be written to 0 for future compability.
MLTPKT	13	Multi-Packet Mode. When set, the device operates in Multi-Packet mode. While working in Multi-Packet mode, the txrdy signal is deasserted when at least one of the following is true: • The amount of free space in its TFIFO is below the FIFO transmit threshold. • The number of full packets stored in the TFIFO is sixteen. • A data burst on the IX Bus is in progress. Note that the Single Packet Mode control bit (TX_RX_PARAM<SPM>) should be reset to 0 when this bit is set. When cleared, the device retains all the features as described in the *IXF1002Dual Port Gigabit Ethernet Datasheet*.
FIFMD	12:11	**IX Bus mode:** This field sets the IX Bus mode. Both ports of the IXF1002 must be operating in the same IX Bus mode. The table below shows the IX Bus mode according to bits 12 and 11. **Bit 12** **Bit 11** **Mode** 0 0 Narrow-32 bit mode 0 1 Full-64 bit mode 1 0 Split mode 1 1 Reserved In the full-64 bit mode, the 64 bits fdat<63:0> are used for either transmitting or receiving data. In the split mode, the 32 lower bits fdat<31:0> are used for receiving packets from the receive FIFO and the 32 higher bits fdat<63:32> are used for transmitting packets to the transmit FIFO. In the narrow mode, the lower 32 bits fdat<31:1> are used for either transmitting or receiving packets.
HRYD	10	**Header ready disable.** When set, the **rxrdy** signal will not be asserted when a packet header is in FIFO, but only according to FIFO threshold values.
PS_D	9	**Packet status disable.** When set, the packet status will not be appended to received packets that are transferred onto the IX Bus. When reset, The packet status is appended to any packet completely transferred onto the IX Bus, and is driven onto the IX Bus in the access following the last byte transfer (see 4.3.1.1) of data.
BEND	8	**Big or little endian mode.** Defines the byte ordering mode on the IX Bus. When set, the port uses the big endian mode. When reset, the little endian mode is used.

Bit Name	Bit #	Bit Description
LCKE	7	**Enable activation of lock to reference signal.** When set, the lckref_{i} signal will be asserted to the PHY when there is no activity (no signal detected) on the line. Used only in GPCS mode.
FXECD	6	**Fix enable comma detect signal.** When set, the encdet_{i} signal to the PHY will be continuously asserted. When cleared, the encdet_{i} signal will be asserted only during loss of synchronization. Used only in GPCS mode.
ILPK	5	**Internal loopback mode.** When set, the port is disconnected from the line and all the transmitted packets are sent back to the receive side. Packets are not transmitted onto the line and packets received from the line are rejected.
—	4:3	RESERVED
CPUBW	2	**CPU data bus width.** When asserted, bus width is 16, all **cdat<15:0>** bits are in use. When deasserted, bus width is 8, indicating that the 8 low bits **cdat<7:0>** are in use.
SDDIS	1	**Signal detect disable.** Setting this bit will cause IXF1002 to consider the value of the sd{i} input signal as high, regardless to the actual value on the pin. Used only in GPCS mode.
GPCS	0	**GPCS port mode.** This bit defines the GMII/GPCS port mode. If a GPCS PHY device is connected, this bit must be set. If a GMII PHY device is connected, this bit must be reset.
Access Rules		
Register access		R/W
Value after reset		0000H