M2114A

1024 x 4 Bit Static RAM

The Intel M2114A is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using HMOS, a high performance MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding, therefore it requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The M2114A is designed for memory applications where the high performance and high reliability of HMOS, low cost, large bit storage, and simple interfacing are important design objectives. The M2114A is placed in an 18-pin package for the highest possible density.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

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PCN# 2002_002

PRODUCT CHANGE NOTIFICATION

Rochester Part No.(s):	MD2114AL-3/B, -4/B, -5/B	Data Sheet:	Intel Data Sheet
Generic Device:	2114	Die Mfgr:	Intel
Issued By:	Robert S. Everette RSE	Date:	2/20/2002

Item #

THIS PRODUCT CHANGE NOTIFICATION DOCUMENTS DIFFERENCES FROM THE ORIGINAL MANUFACTURER'S DATA SHEET REFERENCED. THIS PCN WILL AFFECT CURRENT ORDERS AND FUTURE ORDERS UNLESS A FURTHER NOTIFICATION IS ISSUED OR UNLESS OTHERWISE STATED BELOW.

1. C_S (capacitance from any pin to V_{SS}) is changed from: 5 picofarads maximum.
to: 6 picofarads maximum.

The following authorized representative hereby acknowledges the above Product Change Notification:

Printed	**Signed**	**Date Signed:**
Name:	**Name:**	
Title:	**Company:**	

M2114A
1024 x 4 BIT STATIC RAM

Military

	M2114AL-3	M2114AL-4	M2114A-4	M2114AL-5
Max. Access Time (ns)	150	200	200	250
Max. Current (mA)	50	50	70	70

- **HMOS Technology**
- **Low Power, High Speed**
- **Identical Cycle and Access Times**
- **Single +5V Supply ±10%**
- **High Density 18-Pin Package**
- **Completely Static Memory—No Clock or Timing Strobe Required**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **M2114 Upgrade**
- **Military Temperature Range −55°C to +125°C (T_C)**
- **Not Recommended for New Designs**

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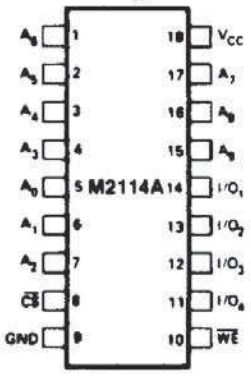
The M2114A is designed for memory applications where the high performance and high reliability of HMOS, low cost, large bit storage, and simple interfacing are important design objectives. The M2114A is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a signal +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual packge when outputs are or-tied.

Pin Configuration



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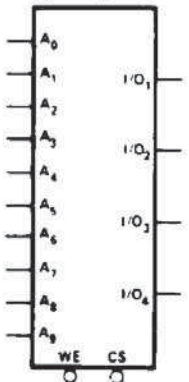
Logic Symbol



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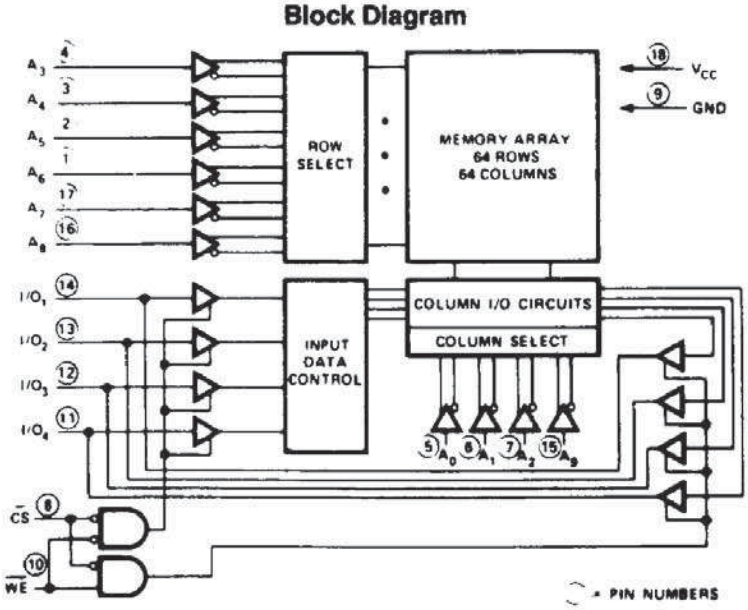
Pin Names

A_0–A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1–I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

Block Diagram



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December 1989
Order Number: 271001-003

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin
With Respect to Ground ..... −3.5V to +7V
Power Dissipation 1.0W
D.C. Output Current ..... 5 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions

Symbol	Parameter	Min	Max	Units
T_C	Case Temperature (Instant On)	−55	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V

D.C. AND OPERATING CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	M2114AL-3/L-4			M2114A-4/-5			Units	Comments
		Min	Typ(2)	Max	Min	Typ(2)	Max		
I_{LI}	Input Load Current (All Input Pins)			10			10	μA	V_{IN} = 0 to 5.5V
$\|I_{LO}\|$	I/O Leakage Current		10				10	μA	$\overline{CS} = V_{IN}$ $V_{I/O}$ = GND to V_{CC}
I_{CC}	Power Supply Current		25	50		50	70	mA	V_{CC} = max, $I_{I/O}$ = 0 mA, T_C = −55°C
V_{IL}	Input Low Voltage	−3.0		0.8	−3.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
I_{OL}	Output Low Current	2.1	9.0		2.1	9.0		mA	V_{OL} = 0.4V
I_{OH}	Output High Current	−1.0	−2.5		−1.0	−2.5		mA	V_{OH} = 2.4V
I_{OS}(2)	Output Short Circuit			40			40	mA	V_{OUT} = GND

NOTES:
1. Typical values are for T_C = 25°C and V_{CC} = 5.0V.
2. Duration not to exceed 30 seconds.

CAPACITANCE T_C = 25°C, f = 1.0 MHz

Symbol	Test	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance	6	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels ..... 0.8V to 2.0V
Input Rise and Fall Times ..... 10 ns
Input and Output Timing Levels 1.5V
Output Load ..... 1 TTL Gate and C_L = 100 pF

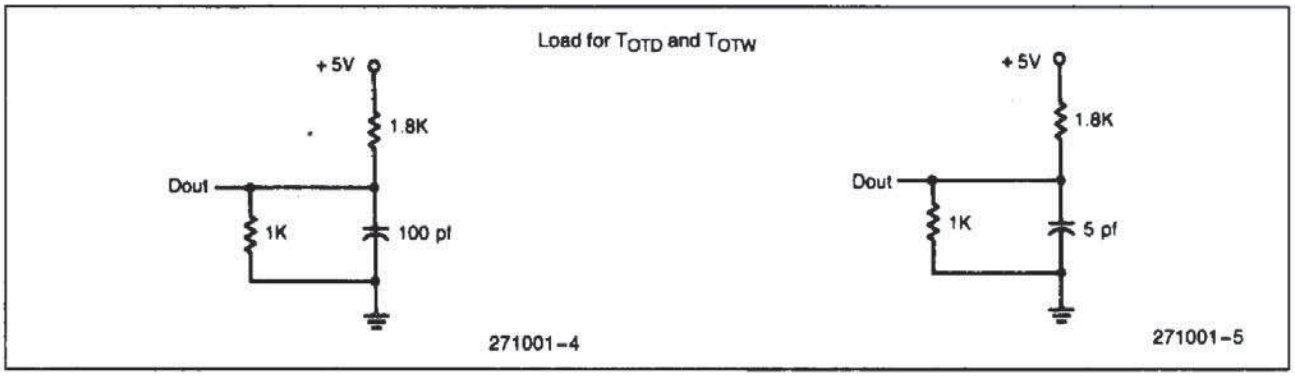

Figure 1

Figure 2

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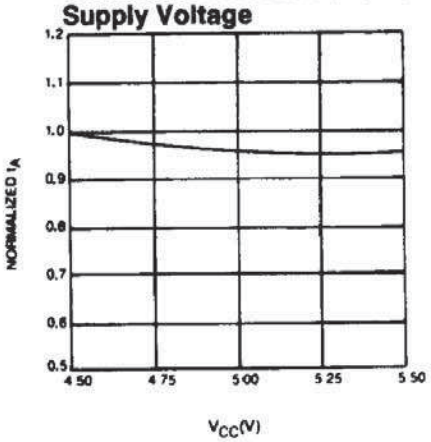
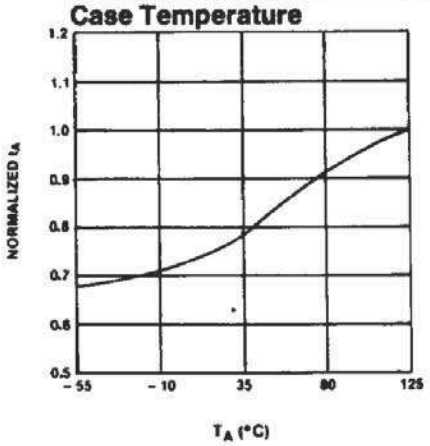
TYPICAL D.C. AND A.C. CHARACTERISTICS

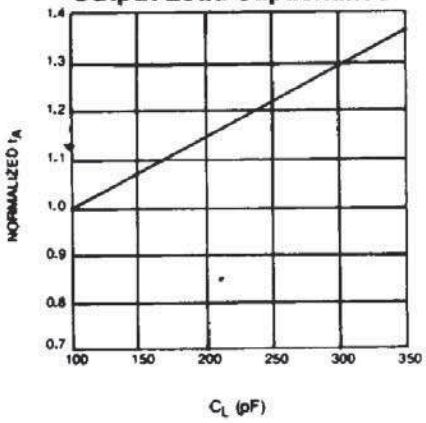
Normalized Access Time Vs. Supply Voltage



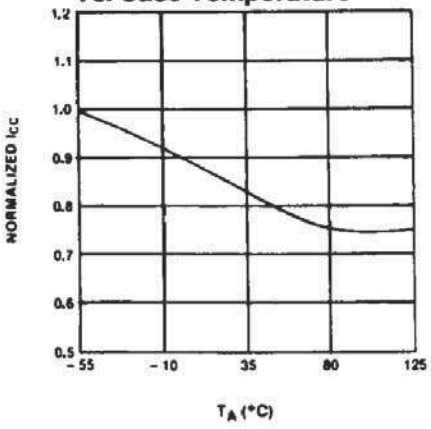
Normalized Access Time Vs. Case Temperature



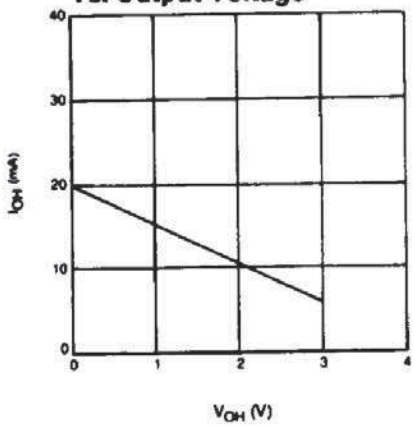
Normalized Access Time Vs. Output Load Capacitance



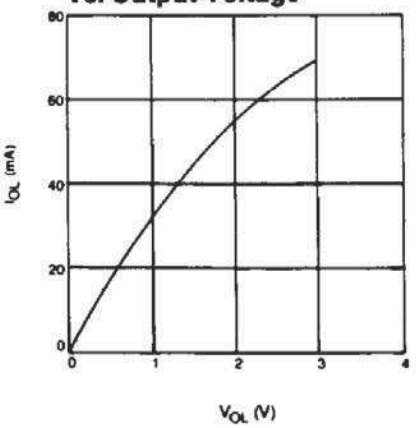
Normalized Power Supply Current Vs. Case Temperature



Output Source Current Vs. Output Voltage



Output Sink Current Vs. Output Voltage



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A.C. CHARACTERISTICS (Over Specified Operating Conditions)

READ CYCLE[1]

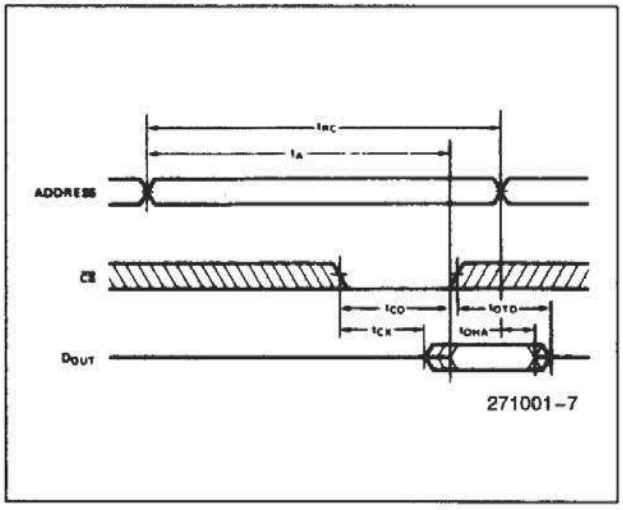
Symbol	Parameter	M2114AL-3		M2114A-4/L-4		M2114A-5		Units
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	150		200		250		ns
t_A	Access Time		150		200		250	ns
t_{CO}	Chip Selection to Output Valid		70		70		85	ns
t_{CX}[2]	Chip Selection to Output Active	10		10		10		ns
t_{OTD}[2]	Output 3-State from Deselection		40		50		60	ns
t_{OHA}	Output Hold from Address Change	15		15		15		ns

WRITE CYCLE[3]

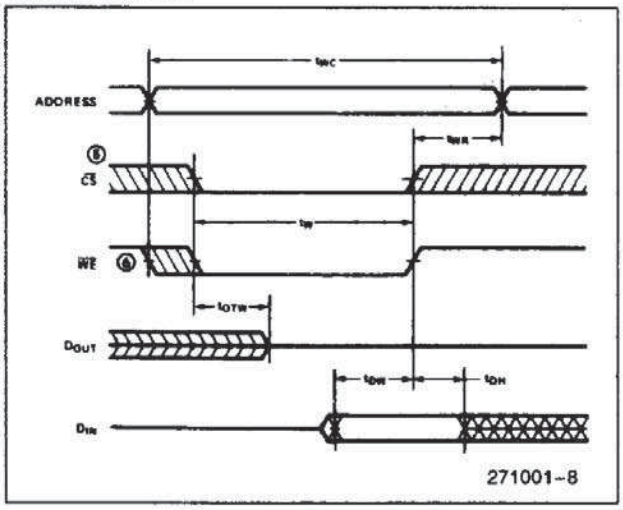
Symbol	Parameter	M2114AL-3		M2114A-4/L-4		M2114A-5		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	150		200		250		ns
t_W[3]	Write Time	90		120		135		ns
t_{WR}	Write Release Time	0		0		0		ns
t_{OTW}[2]	Output 3-State from Write		40		50		60	ns
t_{DW}	Data to Write Time Overlap	90		120		135		ns
t_{DH}	Data Hold from Write Time	0		0		0		ns

WAVEFORMS

READ CYCLE[4]



WRITE CYCLE



NOTES:
1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. Measured at ±500 mV with 1 TTL Gate and C_L = 5 pf. Using Figure 2.
3. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.
4. $\overline{WE}$ is high for a Read Cycle.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
6. $\overline{WE}$ must be high during all address transitions.