

M2732A

32K (4K x 8) UV Erasable PROM

The Intel M2732A is a 5V only, 32,768 bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The standard M2732A's access time is 450 ns with speed selection (M2732A-25) available at 250 ns. The access time is compatible to high performance microprocessors, such as the 5 MHz MiAPX 86/10. In these systems, the M2732A allows the microprocessor to operate without the addition of WAIT states.

An important M2732A feature is the separate output control, Output Enable (\overline{OE}), from the Chip Enable control (\overline{CE}). The \overline{OE} control eliminates bus contention in multiple bus microprocessor systems.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.



M2732A

32K (4K x 8) UV ERASABLE PROM

Military

- 250 ns (M2732A-25) Maximum Access Time ... HMOS* -E Technology
- Compatible to High Speed 5 MHz MIAPX 86/10 MPU ... Zero Wait State
- Military Temperature Range: -55°C to +125°C (T_C)
- Industry Standard Pinout ... JEDEC Approved
- Two Line Control
- Low Standby Current ... 35 mA Max.

The Intel M2732A is a 5V only, 32,768 bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The standard M2732A's access time is 450 ns with speed selection (M2732A-25) available at 250 ns. The access time is compatible to high performance microprocessors, such as the 5 MHz MIAPX 86/10. In these systems, the M2732A allows the microprocessor to operate without the addition of WAIT states.

An important M2732A feature is the separate output control, Output Enable (\overline{OE}), from the Chip Enable control (\overline{CE}). The \overline{OE} control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the \overline{OE} and \overline{CE} controls on Intel's EPROMs. AP-72 is available from Intel's Literature Department.

The M2732A has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 115 mA, while the maximum standby current is only 35 mA, a 66% saving. The standby mode is achieved by applying a TTL-high signal to the \overline{CE} input.

The M2732A is fabricated with HMOS-E technology, Intel's high speed N-channel MOS Silicon Gate Technology.

*HMOS is a patented process of Intel Corporation.

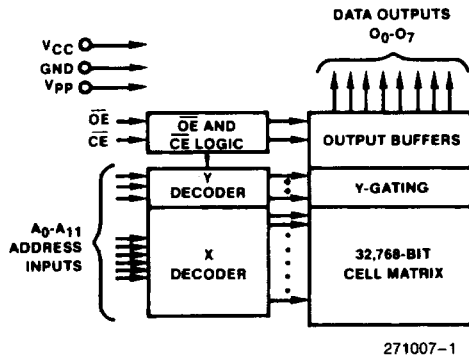


Figure 1. Block Diagram

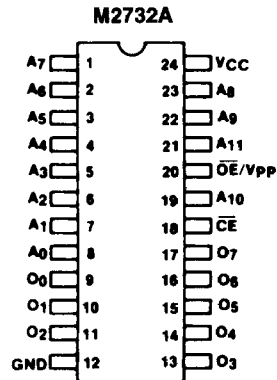


Figure 2. Configuration

| Mode Selection | | | | | |
|-----------------|------|-----------------|-------------------------|----------------------|-----------------------|
| Mode | Pins | CE (18) | OE/V _{PP} (20) | V _{CC} (24) | Outputs (9-11, 13-17) |
| Read | | V _{IL} | V _{IL} | +5 | D _{OUT} |
| Standby | | V _{IH} | Don't Care | +5 | High Z |
| Program | | V _{IL} | V _{PP} | +5 | D _{IN} |
| Program Verify | | V _{IL} | V _{IL} | +5 | D _{OUT} |
| Program Inhibit | | V _{IH} | V _{PP} | +5 | High Z |

| Pin Names | |
|---------------------------------|---------------|
| A ₀ -A ₁₁ | Addresses |
| \overline{CE} | Chip Enable |
| \overline{OE} | Output Enable |
| O ₀ -O ₇ | Outputs |

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias -55°C to $+135^{\circ}\text{C}$
 Storage Temperature -65°C to $+150^{\circ}\text{C}$
 All Input or Output Voltages with
 Respect to Ground $+6\text{V}$ to -0.3V
 V_{PP} Supply Voltage with Respect to
 Ground During Programming $+22\text{V}$ to -0.3V

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. AND A.C. OPERATING CONDITIONS DURING READ

| | M2732A-25 | M2732A-45 |
|---------------------------------------|---|---|
| Operating Temperature Range (T_C) | -55°C to $+125^{\circ}\text{C}$ | -55°C to $+125^{\circ}\text{C}$ |
| V_{CC} Power Supply | $5\text{V} \pm 10\%$ | $5\text{V} \pm 10\%$ |

READ OPERATION
D.C. CHARACTERISTICS

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|------------------|-----------------------------------|--------|--------------------|---------------------|---------------|--|
| | | Min | Typ ⁽¹⁾ | Max | | |
| I_{IL} | Input Load Current | | | 10 | μA | $V_{\text{IN}} = 5.5\text{V}$ |
| I_{LO} | Output Leakage Current | | | 10 | μA | $V_{\text{OUT}} = 5.5\text{V}$ |
| I_{CC1} | V_{CC} Current (Standby) | | | 35 | mA | $\overline{\text{CE}} = V_{\text{IH}}, \overline{\text{OE}} = V_{\text{IL}}$ |
| I_{CC2} | V_{CC} Current (Active) | | | 115 | mA | $\overline{\text{OE}} = \overline{\text{CE}} = V_{\text{IL}}$ |
| V_{IL} | Input Low Voltage | -0.1 | | 0.8 | V | |
| V_{IH} | Input High Voltage | 2.0 | | $V_{\text{CC}} + 1$ | V | |
| V_{OL} | Output Low Voltage | | | 0.45 | V | $I_{\text{OL}} = 2.1\text{mA}$ |
| V_{OH} | Output High Voltage | 2.4 | | | V | $I_{\text{OH}} \pm 400\ \mu\text{A}$ |

NOTE:

1. Typical values are for $T_C = 25^{\circ}\text{C}$ and nominal supply voltages.

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A.C. CHARACTERISTICS

| Symbol | Parameter | M2732A-25 | | | M2732A-45 | | | Unit | Test Conditions |
|-----------------------|---|-----------|--------------------|-----|-----------|--------------------|-----|------|---|
| | | Min | Typ ⁽¹⁾ | Max | Min | Typ ⁽¹⁾ | Max | | |
| t_{ACC} | Address to Output Delay | | | 250 | | | 450 | ns | $\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}$ |
| t_{CE} | $\overline{\text{CE}}$ to Output Delay | | | 250 | | | 450 | ns | $\overline{\text{OE}} = V_{\text{IL}}$ |
| t_{OE} | Output Enable to Output Delay | 10 | | 100 | 10 | | 150 | ns | $\overline{\text{CE}} = V_{\text{IL}}$ |
| $t_{\text{DF}}^{(2)}$ | Output Enable High to Output Float | 0 | | 90 | 0 | | 130 | ns | $\overline{\text{CE}} = V_{\text{IL}}$ |
| $t_{\text{OH}}^{(2)}$ | Output Hold from Addresses, $\overline{\text{CE}}$ or $\overline{\text{OE}}$ Whichever Occurred First | 0 | | | 0 | | | ns | $\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}$ |

CAPACITANCE (1), (2)

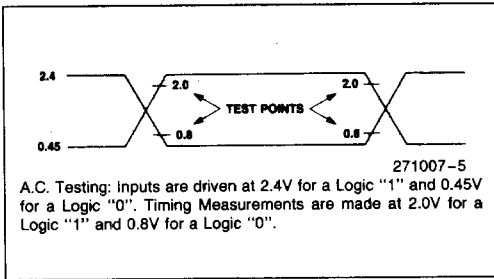
$T_C^{(5)} = 25^\circ\text{C}$, $f = 1 \text{ MHz}$

| Symbol | Parameter | Typ | Max | Unit | Conditions |
|-----------|---|-----|-----|------|----------------|
| C_{IN} | Input Capacitance Except \overline{OE}/V_{PP} | 4 | 6 | pF | $V_{IN} = 0V$ |
| C_{IN} | \overline{OE}/V_{PP} Input Capacitance | | 20 | pF | $V_{IN} = 0V$ |
| C_{OUT} | Output Capacitance | | 12 | pF | $V_{OUT} = 0V$ |

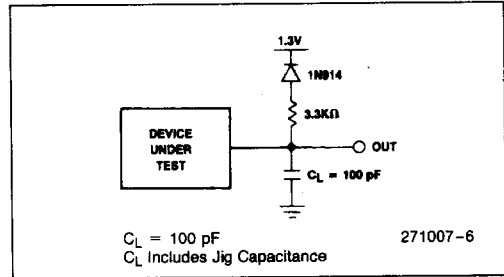
A.C. TEST CONDITIONS

Output Load 1 TTL gate, 100Ω
 Resistor and $C_L = 100 \text{ pF}$
 Input Rise and Fall Times $\leq 20 \text{ ns}$
 Input Pulse Levels 0.45V to 2.4V
 Timing Measurement Reference Level
 Inputs 0.8V and 2V
 Outputs 0.8V and 2V

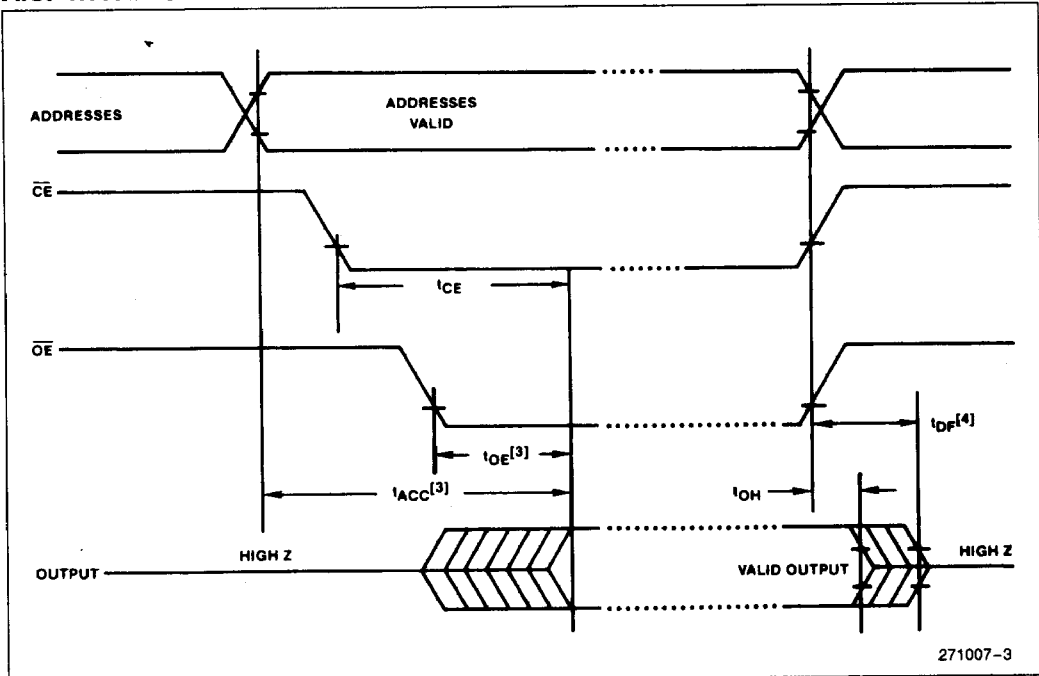
A.C. TESTING, OUTPUT WAVEFORM



A.C. TESTING LOAD CIRCUIT



A.C. WAVEFORMS



NOTES:

1. Typical values are for $T_C = 25^\circ\text{C}$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. \overline{OE} may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{ACC} .
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven.
5. Case temperatures are "instant on".

DEVICE OPERATION

The five modes of operation of the M2732A are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for \overline{OE}/V_{PP} during programming. In the program mode the \overline{OE}/V_{PP} input is pulsed from a TTL level to 21V.

Table 1. Mode Selection

| Mode | Pins | CE (18) | OE/V _{PP} (20) | V _{CC} (24) | Outputs (9-11, 13-17) |
|-----------------|------|-----------------|-------------------------|----------------------|-----------------------|
| Read | | V _{IL} | V _{IL} | +5 | D _{OUT} |
| Standby | | V _{IH} | Don't Care | +5 | High Z |
| Program | | V _{IL} | V _{PP} | +5 | D _{IN} |
| Program Verify | | V _{IL} | V _{IL} | +5 | D _{OUT} |
| Program Inhibit | | V _{IH} | V _{PP} | +5 | High Z |

Read Mode

The M2732A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable (\overline{CE}) is the power control and should be used for device selection. Output Enable (\overline{OE}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from \overline{CE} to output (t_{CE}). Data is available at the outputs after the falling edge of \overline{OE} , assuming that \overline{CE} has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The M2732A has a standby mode which reduces the active power current by 66%, from 115 mA to 35 mA. The M2732A is placed in the standby mode by applying a TTL high signal to the \overline{CE} input. When in standby mode, the outputs are in a high impedance state, independent of the \overline{OE} input.

Output OR-Tieing

Because EPROMs are usually used in larger memory arrays, Intel has provided a 2 line control function that accommodates this use of multiple memory connection. The two line control function allows for:

- a) the lowest possible memory power dissipation, and
- b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, it is recommended that \overline{CE} (pin 18) be decoded and used as the primary device selecting function, while \overline{OE} (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the outputs pins are only active when data is desired from a particular memory device.

Programming

Programming is the same as Intel's M2732 except for the programming voltage. In the program mode the M2732A \overline{OE}/V_{PP} input is pulsed from a TTL low level to 21V (25V for the M2732). **Exceeding 21.5V will damage the M2732A.**

Initially, and after each erasure, all bits of the M2732A are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2732A is in the programming mode when the \overline{OE}/V_{PP} input is at 21V. It is required that a 0.1 μ F capacitor be placed across \overline{OE}/V_{PP} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms, active low, TTL program pulse is applied to the \overline{CE} input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms. The M2732A must not be programmed with a DC signal applied to the \overline{CE} input.

Programming of the multiple M2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled M2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the \overline{CE} input programs the paralleled M2732As.

Program Inhibit

Programming of multiple M2732As in parallel with different data is also easily accomplished. Except for \overline{CE} , all like inputs (including \overline{OE}) of the parallel M2732As may be common. A TTL level program pulse applied to a M2732A's \overline{CE} input with \overline{OE}/V_{PP} at 21V will program that M2732A. A high level \overline{CE} input inhibits the other M2732As from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with \overline{OE}/V_{PP} and \overline{CE} at V_{IL} . Data should be verified t_{DV} after the falling edge of \overline{CE} .

ERASURE CHARACTERISTICS

The erasure characteristics of the M2732A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000

Angstroms (\AA). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 \AA range. Data shows that constant exposure to room level fluorescent lighting could erase the typical M2732A in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M2732A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the M2732A window to prevent unintentional erasure.

The recommended erasure procedure for the M2732A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (\AA). The integrated dose (i.e., UV intensity \times exposure time) for erasure should be a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 $\mu\text{W}/\text{cm}^2$ power rating. The M2732A should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

PROGRAMMING

D.C. PROGRAMMING CHARACTERISTICS(1)

$T_C = 25^\circ\text{C} \pm 5^\circ\text{C}$; $V_{CC} = 5\text{V} \pm 5\%$; $V_{PP} = 21\text{V} \pm 0.5\text{V}$

| Symbol | Parameter | Limits | | | | Test Conditions |
|----------|--|--------|-----|--------------|---------------|---|
| | | Min | Typ | Max | Unit | |
| I_{LI} | Input Current (All Inputs) | | | 10 | μA | $V_{IN} = V_{IL}$ or V_{IH} |
| V_{OL} | Output Low Voltage During Verify | | | 0.45 | V | $I_{OL} = 2.1\text{mA}$ |
| V_{OH} | Output High Voltage During Verify | 2.4 | | | V | $I_{OH} = -400\mu\text{A}$ |
| I_{CC} | V_{CC} Supply Current | | 85 | 125 | mA | |
| V_{IL} | Input Low Level (All Inputs) | -0.1 | | 0.8 | V | |
| V_{IH} | Input High Level (All Inputs Except \overline{OE}/V_{PP}) | 2.0 | | $V_{CC} + 1$ | V | |
| I_{PP} | V_{PP} Supply Current | | | 35 | mA | $\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$ |

NOTE:

1. When programming the M2732A, a 0.1 μF capacitor is required across \overline{OE}/V_{PP} and ground to suppress spurious voltage transients which may damage the device.

A.C. PROGRAMMING CHARACTERISTICS

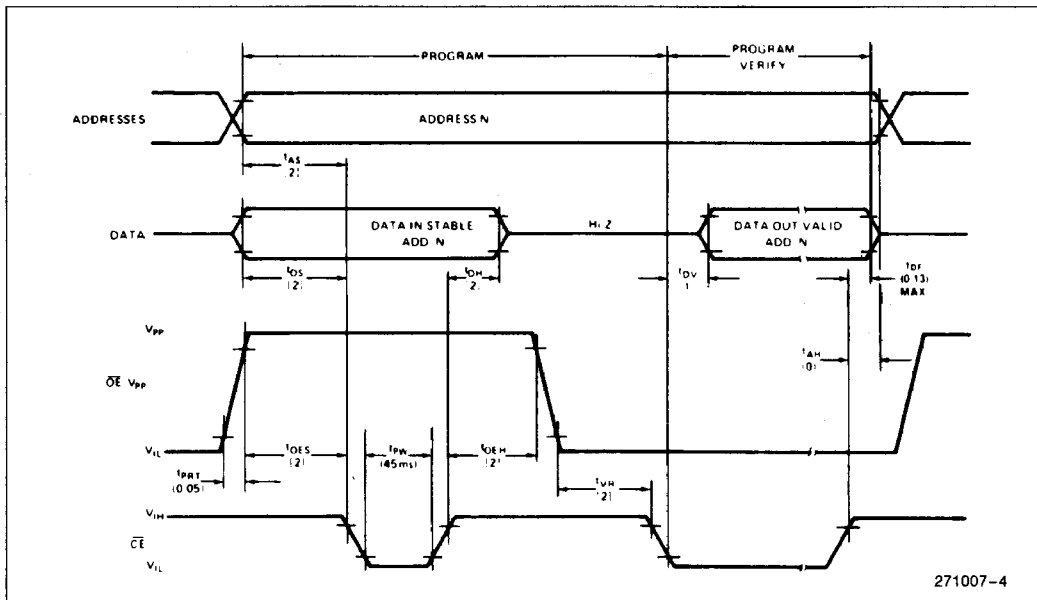
$T_C = 25^\circ\text{C} \pm 5^\circ\text{C}$; $V_{CC} = 5\text{V} \pm 5\%$; $V_{PP} = 21\text{V} \pm 0.5\text{V}$

| Symbol | Parameter | Limits | | | | Test Conditions* |
|------------|---|--------|-----|-----|---------------|---|
| | | Min | Typ | Max | Unit | |
| t_{AS} | Address Setup Time | 2 | | | μS | |
| t_{OES} | $\overline{\text{OE}}$ Setup Time | 2 | | | μS | |
| t_{DS} | Data Setup Time | 2 | | | μS | |
| t_{AH} | Address Hold Time | 0 | | | μS | |
| $t_{OE H}$ | OE Hold Time | 2 | | | μS | |
| t_{DH} | Data Hold Time | 2 | | | μS | |
| t_{DF} | Chip Enable to Output Float Delay | 0 | | 130 | ns | |
| t_{DV} | Data Valid from $\overline{\text{CE}}$ | | | 1 | μS | $\overline{\text{OE}} = V_{IL}, \text{OE} = V_{IL}$ |
| t_{PW} | $\overline{\text{CE}}$ Pulse Width During Programming | 45 | 50 | 55 | ms | |
| t_{PRT} | $\overline{\text{OE}}$ Pulse Rise Time During Programming | 50 | | | ns | |
| t_{VR} | V_{PP} Recovery Time | 2 | | | μS | |

*A.C. TEST CONDITIONS

- Input Rise and Fall Times (10% to 90%) 20 ns
- Input Pulse Levels 0.45V to 2.4V
- Input Timing Reference Level 1.0V and 2.0V
- Output Timing Reference Level 0.8V and 2.0V

PROGRAMMING WAVEFORMS



- NOTES:**
- All times shown in () are minimum and in μS unless otherwise specified.
 - The input timing reference level is 1V for a V_{IL} and 2V for a V_{IH} .