M80C51BH/M80C31BH

CMOS Single-Chips 8-Bit Microcomputer

The MCS®-51 CHMOS products are fabricated on Intel's CHMOS III process and are functionally compatible with the standard MCS-51 HMOS and EPROM products. CHMOS III is a technology which combines the high speed and density characteristics of HMOS with the low power attributes of CHMOS. This combination expands the effectiveness of the powerful MCS-51 architecture and instruction set.

Like the MCS-51 HMOS versions, the MCS-51 CMOS products have the following features: 4K byte of ROM (M80C51BH only); 128 bytes of RAM; 32 I/O lines; two 16-bit timer/counters; a five-source two-level interrupt structure; a full duplex serial port; and on-chip oscillator and clock circuitry.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

© 2013 Rochester Electronics, LLC. All Rights Reserved 07112013

M80C51BH/M80C31BH
CMOS SINGLE-CHIP 8-BIT MICROCOMPUTER

Military

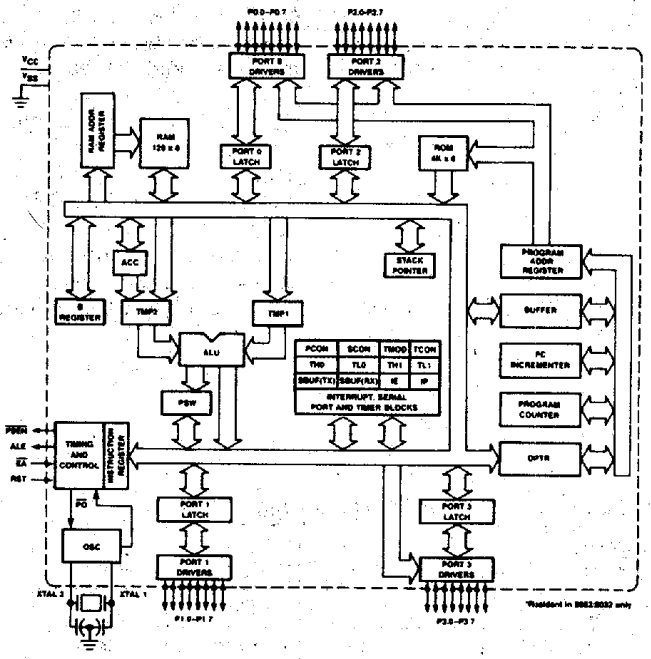
- **M80C31BH—Control Oriented CPU with RAM and I/O**
- **M80C51BH—An M80C31BH with Factory Mask-Programmable ROM**
- **Power Control Modes**
- **128 x 8-Bit RAM**
- **32 Programmable I/O Lines**
- **Two 16-Bit Timer/Counters**
- **Available in 40-Pin CERDIP, 44-Pin Leadless Chip Carrier, 44-Pin Gullwing and 44-Pin J-Lead Packages**
- **64K Program Memory Space**
- **High Performance CHMOS Process**
- **Boolean Processor**
- **5 Interrupt Sources**
- **Programmable Serial Port**
- **64K Data Memory Space**
- **Military Temperature Range: −55°C to +125°C (T_C)**

The MCS®-51 CHMOS products are fabricated on Intel's CHMOS III process and are functionally compatible with the standard MCS-51 HMOS and EPROM products. CHMOS III is a technology which combines the high speed and density characteristics of HMOS with the low power attributes of CHMOS. This combination expands the effectiveness of the powerful MCS-51 architecture and instruction set.

Like the MCS-51 HMOS versions, the MCS-51 CHMOS products have the following features: 4K byte of ROM (M80C51BH only); 128 bytes of RAM; 32 I/O lines; two 16-bit timer/counters; a five-source two-level interrupt structure; a full duplex serial port; and on-chip oscillator and clock circuitry. In addition, the MCS-51 CHMOS products have two software selectable modes of reduced activity for further power reduction—Idle and Power Down.

4

The Idle mode freezes the CPU while allowing the RAM, timer/counters serial port and interrupt system to continue functioning. The Power Down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.



270071-1

Figure 1. Block Diagram

February 1991
Order Number: 270071-005

IDLE MODE

In the Idle mode, the CPU puts itself to sleep while all the on chip peripherals stay active. The instruction that invokes the Idle mode is the last instruction executed in the normal operating mode before Idle mode is activated. The content of CPU, the on chip RAM, and all the Special Function Registers remain intact during this mode. The Idle mode can be terminated either by any enabled interrupt, at which time the process is picked up at the interrupt service routine and continued, or by a hardware reset which starts the processor the same as a power on reset.

POWER DOWN MODE

In the Power Down mode the oscillator is stopped, and the instruction that invokes Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

The only exit from Power Down is a hardware reset. Reset redefines the SFRs, but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

The control bits for the reduced power modes are in the Special Function Register PCON.

NOTE:
For more detailed information on these reduced power modes refer to Application Note AP-255, "Designing with the M80C51BH".

PIN DESCRIPTIONS

V_{CC}

Supply voltage during normal, Idle, and Power Down operations.

V_{SS}

Circuit ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s. Port 0 also outputs the code bytes during program verification in the M80C51BH. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during program verification.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Table 1. Status of the external pins during Idle and Power Down modes

Mode	Program Memory	ALE	PSEN	Port 0	Port 1	Port 2	Port 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

INTEL CORP (UP/PRPHLS)

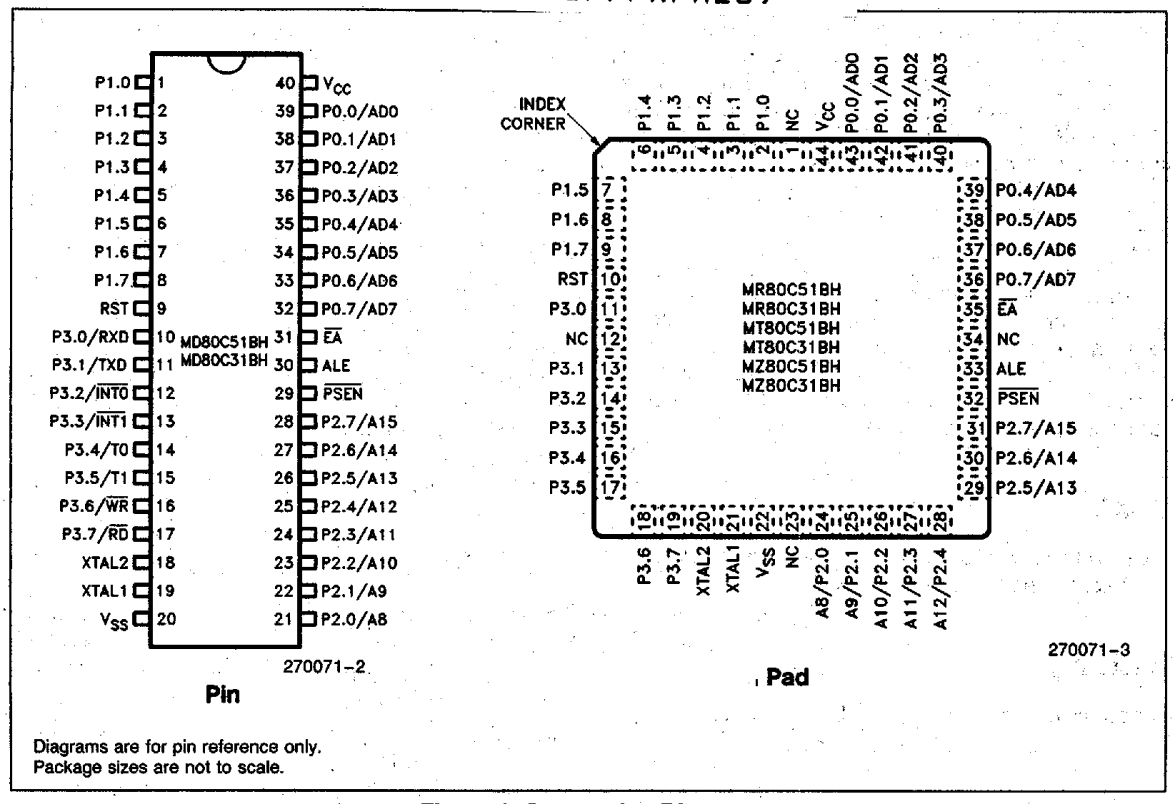


Figure 2. Connection Diagram

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits Power-On reset using only an external capacitor to V_{CC}.

ALE

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{PSEN}$

Program Store Enable is the read strobe to external Program Memory.

When the M80C51BH is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.

$\overline{EA}$

External Access enable. $\overline{EA}$ must be externally held low in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFH. If $\overline{EA}$ is held high the device executes from internal Program Memory unless the program counter contains an address greater than 0FFFH.

XTAL1

Input to the inverting oscillator amplifier and input to the internal block generator circuits.

XTAL2

Output from the inverting oscillator amplifier.

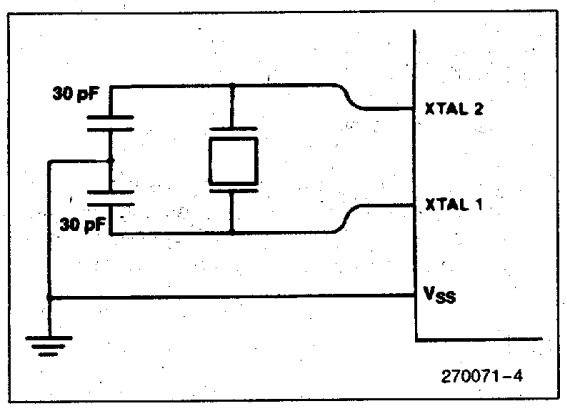


Figure 3. Crystal Oscillator

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers," published in the Embedded Controller Handbook.

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

DESIGN CONSIDERATIONS

- At power on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.
- Before entering the Power Down mode the contents of the Carry Bit and B.7 must be equal.
- When the Idle Mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

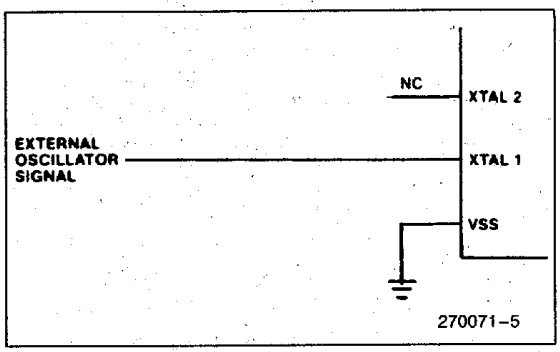


Figure 4. External Drive Configuration

ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin to V_{SS} . . . . −0.5V to V_{CC} +0.5V
Voltage on V_{CC} to V_{SS} . . . . . −0.5V to +6.5V
Power Dissipation . . . . . 200 mW

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Operating Conditions

Symbol	Description	Min	Max	Units
T_C	Case Temperature (Instant On)	−55	+125	°C
V_{CC}	Digital Supply Voltage	4.0	6.0	V
f_{OSC}	Oscillator Frequency	3.5	12	MHz

D.C. CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	Min	Max	Units	Comments
V_{IL}	Input Low Voltage (Except EA)	−0.5	0.2 V_{CC} − 0.25	V	
V_{IL1}	Input Low Voltage (EA)	−0.5	0.2 V_{CC} − 0.45		
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC} +1.1	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC} + 0.2	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)		0.45	V	I_{OL} = 1.6 mA (Note 1)
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN)		0.45	V	I_{OL} = 3.2 mA (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2, 3)	2.4		V	I_{OH} = −60 μA, V_{CC} = 5V ±10%
		0.75 V_{CC}		V	I_{OH} = −25 μA
		0.9 V_{CC}		V	I_{OH} = −10 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode, ALE, PSEN)	2.4		V	I_{OH} = − 400 μA, V_{CC} = 5V ±10%
		0.75 V_{CC}		V	I_{OH} = −150 μA
		0.9 V_{CC}		V	I_{OH} = −40 μA (Note 2)
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)		−75	μA	V_{in} = 0.45V
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3)		−750	μA	V_{in} = 2V
I_{LI}	Input Leakage Current (Port 0, EA)		±10	μA	0.45 < V_{in} < V_{CC}
RRST	Reset Pulldown Resistor	50	150	KΩ	
CIO	Pin Capacitance		10	pF	Test Freq = 1 MHz, T_C = 25°C
IPD	Power Down Current		75	μA	V_{CC} = 2V to 6V (Note 5)

*See "Notes" on next page.

4

INTEL CORP (UP/PRPHLS)

MAXIMUM I_{CC} (mA)

	Operating (Note 3)			Idle (Note 4)		
Freq. V_{CC}	**4V**	**5V**	**6V**	**4V**	**5V**	**6V**
3.5 MHz	4.3	5.7	7.5	1.1	1.6	2.2
8.0 MHz	8.3	11	14	1.8	2.7	3.7
12 MHz	12	16	20	2.5	3.7	5

NOTES:

1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OLS} of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall before the 0.9 V_{CC} specification when the address bits are stabilizing.
3. I_{CC} is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5 ns, V_{IL} = V_{SS} + 0.5V, V_{IH} = V_{CC} − 0.5V; XTAL2 N.C.; $\overline{EA}$ = RST = Port 0 = V_{CC}. I_{CC} would be slightly higher if a crystal oscillator is used (see Figure 5).
4. Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5 ns, V_{IL} = V_{SS} + 0.5V, V_{IH} = V_{CC} − 0.5V; XTAL2 N.C.; Port 0 = V_{CC}; $\overline{EA}$ = RST = V_{SS} (see Figure 6).
5. Power Down I_{CC} is measured with all output pins disconnected; XTAL1 = V_{SS}; XTAL2 N.C.; Port 0 = V_{CC}; $\overline{EA}$ = RST = V_{SS} (see Figure 8).

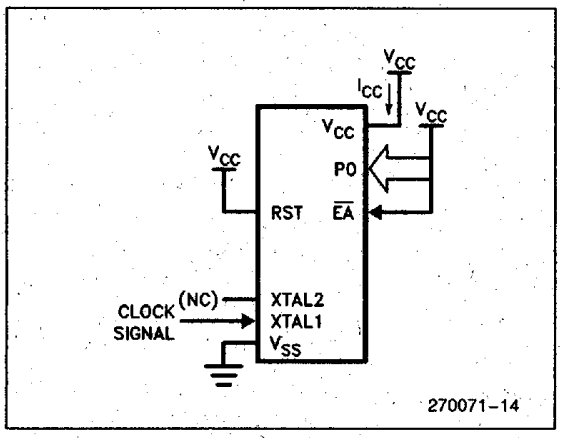


Figure 5. I_{CC} Test Condition, Active Mode. All other pins are disconnected.

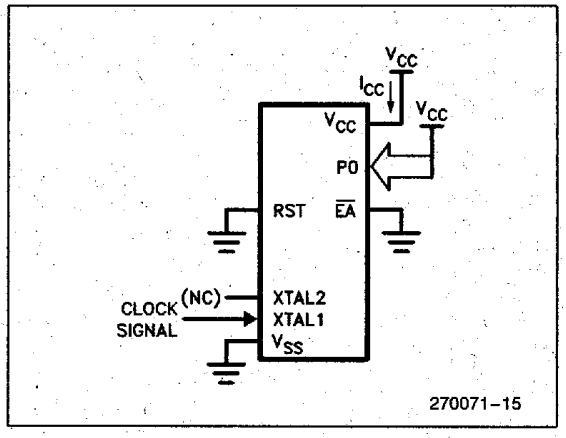


Figure 6. I_{CC} Test Condition, Idle Mode. All other pins are disconnected.

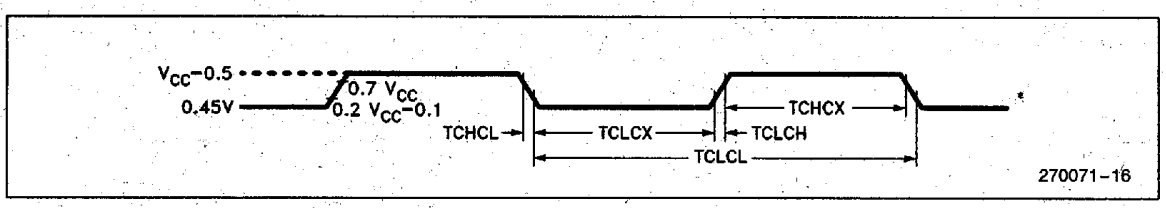


Figure 7. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

INTEL CORP (UP/PRPHLS)

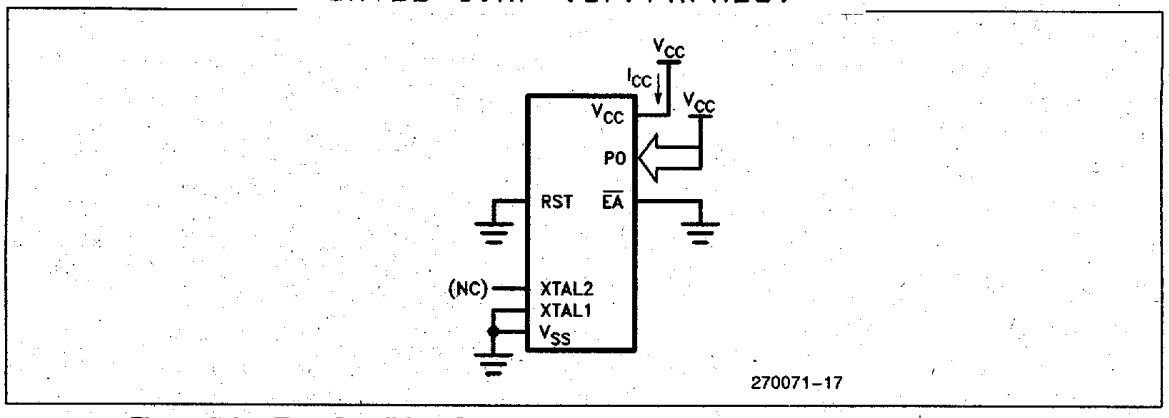


Figure 8. I_{CC} Test Condition, Power Down Mode. All other pins are disconnected.

EXPLANATION OF THE A.C. SYMBOLS

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address.
C: Clock.
D: Input data.
H: Logic level HIGH.
I: Instruction (program memory contents).
L: Logic level LOW, or ALE.
P: PSEN.
Q: Output data.
R: READ signal.
T: Time.
V: Valid.
W: WRITE signal.
X: No longer a valid logic level.
Z: Float.

EXAMPLE:

TAVLL = Time for Address Valid to ALE Low.
TLLPL = Time for ALE Low to $\overline{PSEN}$ Low.

4

INTEL CORP (UP/PRPHLS)

A.C. CHARACTERISTICS (Over Specified Operating Conditions)

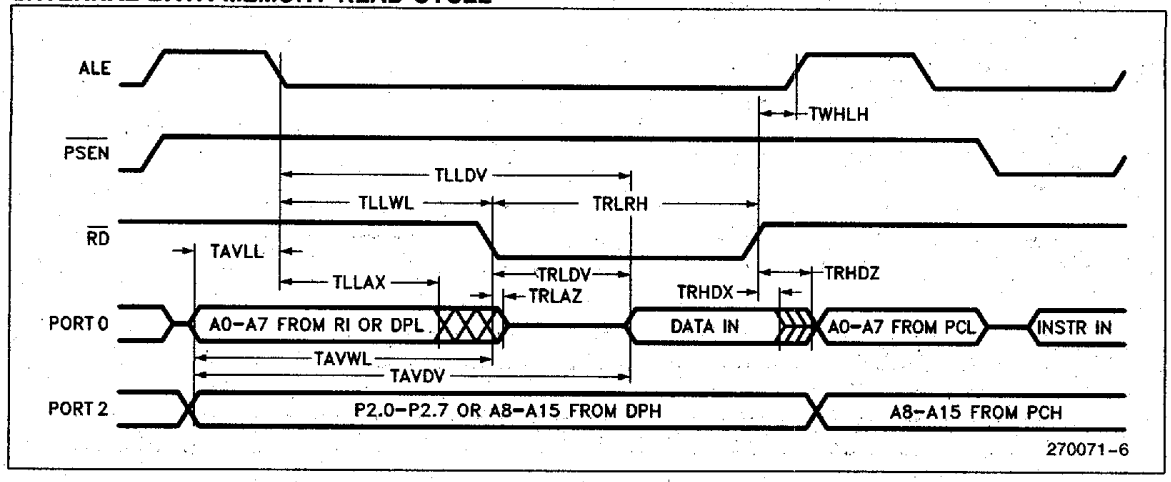
Capacitance for Port 0, ALE, and PSEN = 100 pF, Load Capacitance for All Other Outputs = 80 pF

EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS

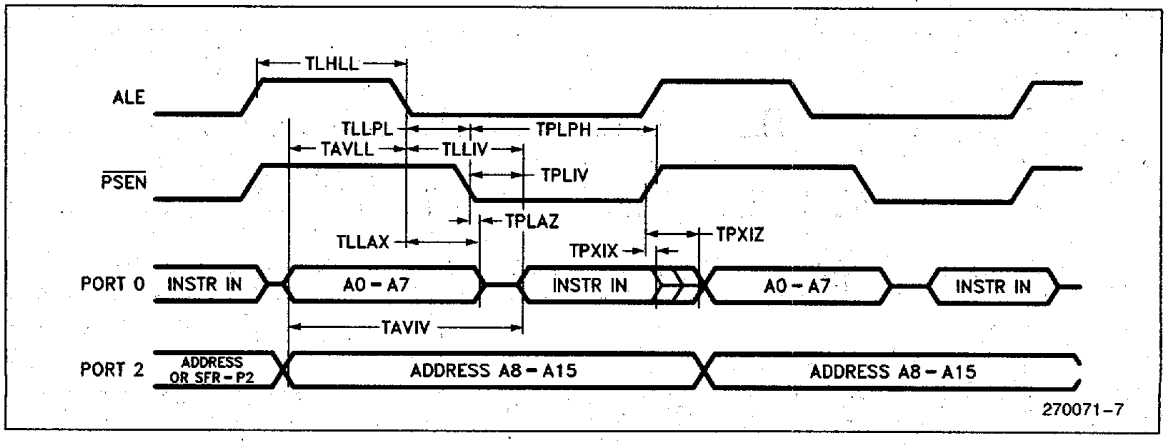
Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	12	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	28		TCLCL−55		ns
TLLAX	Address Hold After ALE Low	48		TCLCL−35		ns
TLLIV	ALE Low to Valid Instr In		223		4TCLCL−110	ns
TLLPL	ALE Low to $\overline{\text{PSEN}}$ Low	43		TCLCL−40		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	205		3TCLCL−45		ns
TPLIV	$\overline{\text{PSEN}}$ Low to Valid Instr In		135		3TCLCL−115	ns
TPXIX	Input Instr Hold After $\overline{\text{PSEN}}$	0		0		ns
TPXIZ	Input Instr Float After $\overline{\text{PSEN}}$		58		TCLCL−25	ns
TAVIV	Address to Valid Instr In		302		5TCLCL−115	ns
TPLAZ	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
TRLRH	$\overline{\text{RD}}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{\text{WR}}$ Pulse Width	400		6TCLCL−100		ns
TRLDV	$\overline{\text{RD}}$ Low to Valid Data In		242		5TCLCL−175	ns
TRHDX	Data Hold After $\overline{\text{RD}}$	0		0		ns
TRHDZ	Data Float After $\overline{\text{RD}}$		97		2TCLCL−70	ns
TLLDV	ALE Low to Valid Data In		507		8TCLCL−160	ns
TAVDV	Address to Valid Data In		575		9TCLCL−175	ns
TLLWL	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	203		4TCLCL−130		ns
TQVWX	Data Valid to $\overline{\text{WR}}$ Transition	23		TCLCL−60		ns
TWHQX	Data Hold After $\overline{\text{WR}}$	33		TCLCL−50		ns
TRLAZ	$\overline{\text{RD}}$ Low to Address Float		0		0	ns
TWHLH	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	43	123	TCLCL−40	TCLCL+40	ns

INTEL CORP (UP/PRPHLS)

EXTERNAL DATA MEMORY READ CYCLE

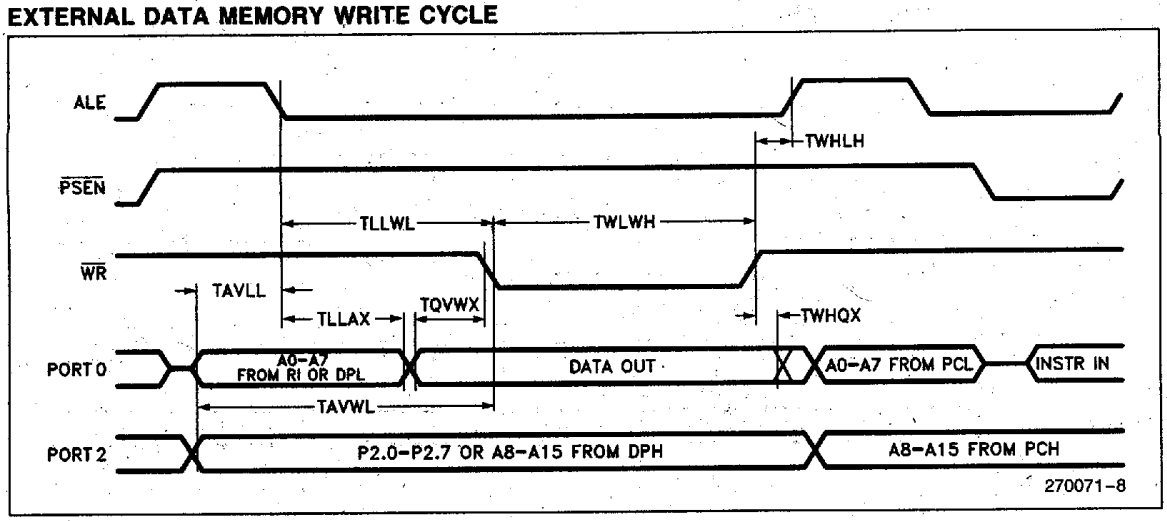


EXTERNAL PROGRAM MEMORY READ CYCLE

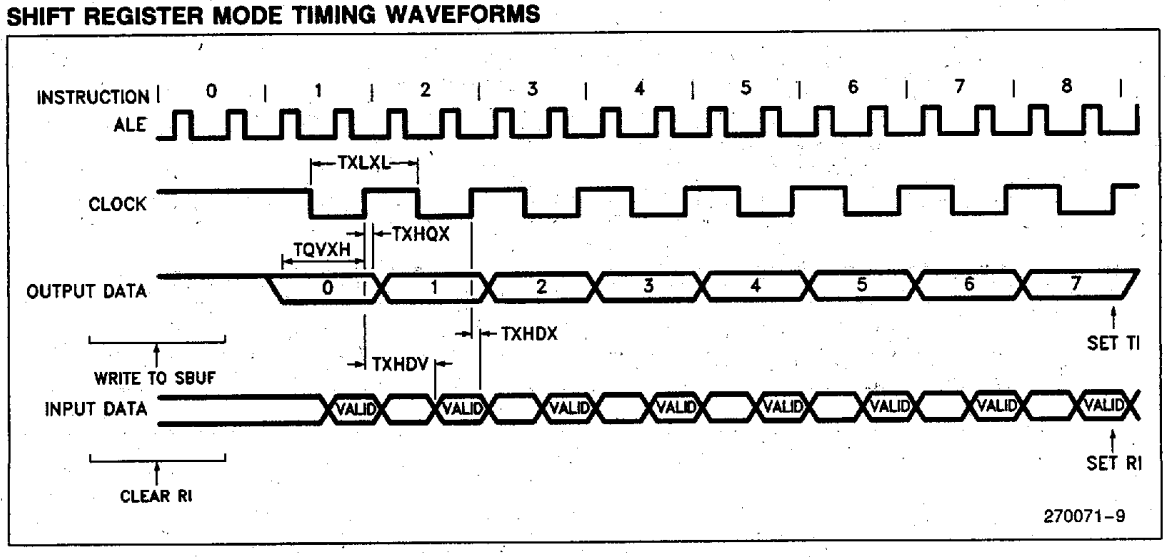


4

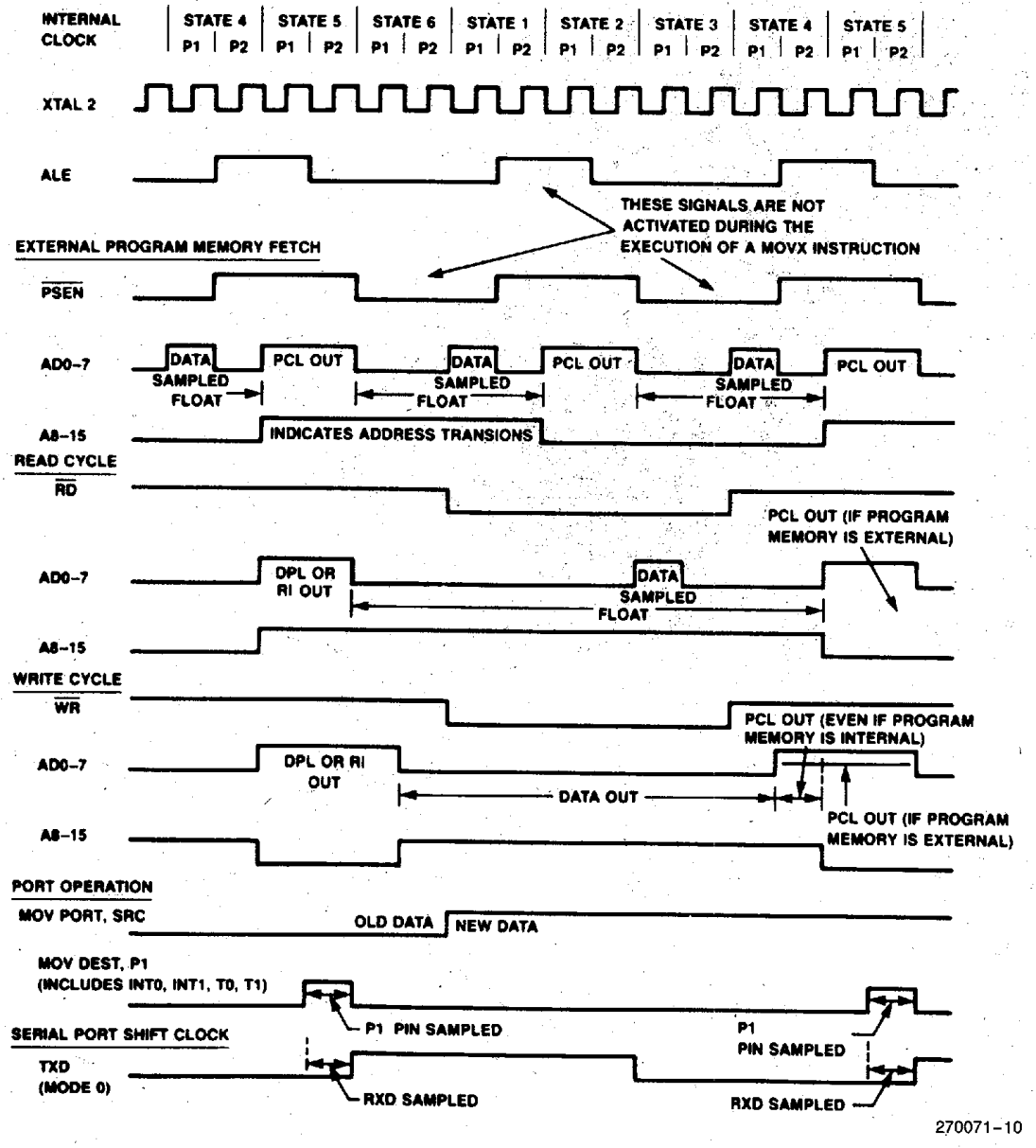
EXTERNAL DATA MEMORY WRITE CYCLE



SHIFT REGISTER MODE TIMING WAVEFORMS



CLOCK WAVEFORMS



270071-10

NOTE:
This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component.

INTEL CORP (UP/PRPHLS)

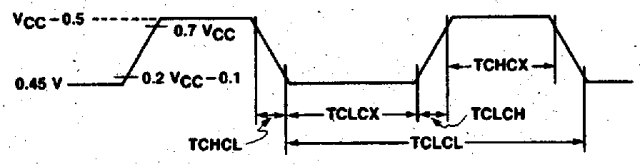
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	12	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

SERIAL PORT TIMING—SHIFT REGISTER MODE (Over Specified Operating Conditions)

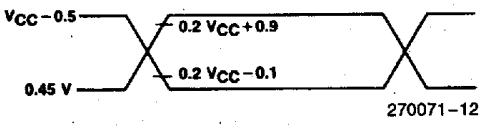
Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL−133		ns
TXHQX	Output Data Hold After Clock Rising Edge	50		2TCLCL−117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL−133	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



270071-11

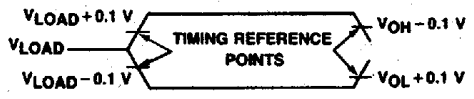
A.C. TESTING: INPUT/OUTPUT WAVEFORMS



270071-12

AC inputs during testing are driven at V_{CC} −0.5 for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min. for a Logic "1" and V_{IL} max. for a Logic "0".

FLOAT WAVEFORM



270071-13

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.