

## MC10125

### *Quad MECL to TTL Translator*

The MC10125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10125 incorporates differential inputs and Schottky TTL “totem pole” outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The  $V_{BB}$  reference voltage is available on pin 1 for use in single-ended input biasing. The outputs of the MC10125 go to a low logic level whenever the inputs are left floating.

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### **Rochester Electronics Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

### **Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

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*The original manufacturer’s datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. ‘Typical’ values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

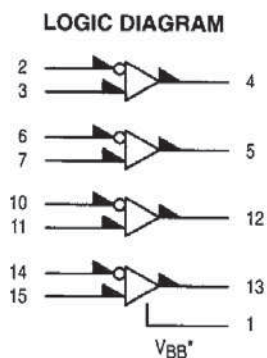
## Quad MECL to TTL Translator

The MC10125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10125 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/ non-inverting translator or as a differential line receiver. The  $V_{BB}$  reference voltage is available on pin 1 for use in single-ended input biasing. The outputs of the MC10125 go to a low logic level whenever the inputs are left floating.

Power supply requirements are ground, +5.0 Volts and -5.2 Volts. Propagation delay of the MC10125 is typically 4.5 ns. The MC10125 has fanout of 10 TTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or TTL out. This device has an input common mode noise rejection of  $\pm 1.0$  Volt.

An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL logic from the noisy TTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.

$P_D = 380$  mW typ/pkg (No Load)  
 $t_{pd} = 4.5$  ns typ (50% to +1.5 Vdc out)  
 $t_r, t_f = 2.5$  ns typ (1.0 V to 2.0 V)



Gnd = PIN 16  
 $V_{CC}$  (+5.0Vdc) = PIN 9  
 $V_{EE}$  (-5.2Vdc) = PIN 8

\* $V_{BB}$  to be used to supply bias to the MC10125 only and bypassed (when used) with 0.01  $\mu$ F to 0.1  $\mu$ F capacitor to ground (0 V).  $V_{BB}$  can source < 1.0 mA.

When the input pin with the bubble goes positive, the output goes negative.

## MC10125



**L SUFFIX**  
CERAMIC PACKAGE  
CASE 620-10

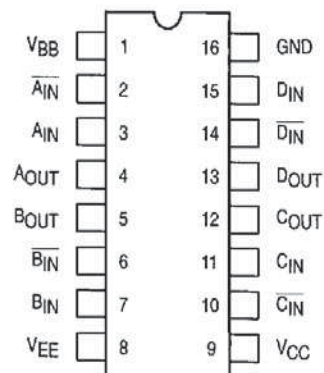


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08



**FN SUFFIX**  
PLCC  
CASE 775-02

### DIP PIN ASSIGNMENT



Pin assignment is for Dual-In-Line Package.  
For PLCC pin assignment, see the Pin Conversion  
Tables on page 8-11.

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## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits						Unit	
			-30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min		Max
Negative Power Supply Drain Current	I <sub>E</sub>	8		-44			-40		-44	mAdc
Positive Power Supply Drain Current	I <sub>CCH</sub>	9		52			52		52	mAdc
	I <sub>CCL</sub>	9		39			39		39	mAdc
Input Current	I <sub>inH</sub> <sup>1</sup>	2		180			115		115	μAdc
Input Leakage Current	I <sub>CBO</sub>	2		1.5			1.0		1.0	μAdc
High Output Voltage	V <sub>OH</sub>	4	2.5		2.5			2.5		Vdc
Low Output Voltage	V <sub>OL</sub>	4		0.5			0.5		0.5	Vdc
High Threshold Voltage	V <sub>OHA</sub>	4	2.5		2.5			2.5		Vdc
Low Threshold Voltage	V <sub>OLA</sub>	4		0.5			0.5		0.5	Vdc
Indeterminate Input Protection Tests	V <sub>OLS1</sub>	4		0.5			0.5		0.5	Vdc
	V <sub>OLS2</sub>	4		0.5			0.5		0.5	Vdc
Short Circuit Current	I <sub>OS</sub>	4	40	100	40		100	40	100	mAdc
Reference Voltage	V <sub>BB</sub>	1	-1.420	-1.280	-1.350		-1.230	-1.295	-1.150	Vdc
Common Mode Rejection Tests	V <sub>OH</sub>	4	2.5		2.5			2.5		Vdc
		4	2.5		2.5			2.5		Vdc
	V <sub>OL</sub>	4		0.5			0.5		0.5	Vdc
		4		0.5			0.5		0.5	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay (50% to +1.5Vdc)	t <sub>6+5-</sub>	5	1.0	6.0	1.0	4.5	6.0	1.0	6.0	
	t <sub>6-5+</sub>	5	1.0	6.0	1.0	4.5	6.0	1.0	6.0	
	t <sub>2+4-</sub>	4	1.0	6.0	1.0	4.5	6.0	1.0	6.0	
	t <sub>2-4+</sub>	4	1.0	6.0	1.0	4.5	6.0	1.0	6.0	
Rise Time (+1.0V to 2.0V)	t <sub>4+</sub>	4		3.3			3.3		3.3	
Fall Time (+1.0V to 2.0V)	t <sub>4-</sub>	4		3.3			3.3		3.3	

1. Individually test each output, apply V<sub>IHmax</sub> to pin under test.

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## ELECTRICAL CHARACTERISTICS (continued)

② Test Temperature			TEST VOLTAGE VALUES (Volts)						Gnd	Output Condition	
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>IHH</sub>	V <sub>ILH</sub>			
-30°C			-0.890	-1.890	-1.205	-1.500	+0.110	-0.890			
+25°C			-0.810	-1.850	-1.105	-1.475	+0.190	-0.850			
+85°C			-0.700	-1.825	-1.035	-1.440	+0.300	-0.825			
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						Gnd	Output Condition	
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>IHH</sub>	V <sub>ILH</sub>			
Negative Power Supply Drain Current	I <sub>E</sub>	8							16		
Positive Power Supply Drain Current	I <sub>CCH</sub>	9	2,6,10,14						16		
	I <sub>CCL</sub>	9		2,6,10,14					16		
Input Current	I <sub>inH</sub> <sup>1</sup>	2	2,6,10,14						16		
Input Leakage Current	I <sub>CBO</sub>	2							16		
High Output Voltage	V <sub>OH</sub>	4		2,6,10,14					16	-2.0mA	
Low Output Voltage	V <sub>OL</sub>	4	2,6,10,14						16	20mA	
High Threshold Voltage	V <sub>OHA</sub>	4		6,10,14		2			16	-2.0mA	
Low Threshold Voltage	V <sub>OLA</sub>	4	6,10,14			2			16	20mA	
Indeterminate Input Protection Tests	V <sub>OLS1</sub>	4							16	20mA	
	V <sub>OLS2</sub>	4							16	20mA	
Short Circuit Current	I <sub>OS</sub>	4		2,6,10,14					4, 16		
Reference Voltage	V <sub>BB</sub>	1		2,6,10,14							
Common Mode Rejection Tests	V <sub>OH</sub>	4						3	2	16	-2.0mA
		4								16	-2.0mA
	V <sub>OL</sub>	4						2	3	16	20mA
		4								16	20mA
Switching Times (50Ω Load)			Pulse In	Pulse Out	C <sub>L</sub> (pF)						
Propagation Delay (50% to +1.5Vdc)	t <sub>6+5-</sub>	5	6	5	25				16		
	t <sub>6-5+</sub>	5	6	5	25				16		
	t <sub>2+4-</sub>	4	2	4	25				16		
	t <sub>2-4+</sub>	4	2	4	25				16		
Rise Time (+1.0V to 2.0V)	t <sub>4+</sub>	4	2	4	25				16		
Fall Time (+1.0V to 2.0V)	t <sub>4-</sub>	4	2	4	25				16		

1. Individually test each output, apply V<sub>IHmax</sub> to pin under test.

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ELECTRICAL CHARACTERISTICS (continued)

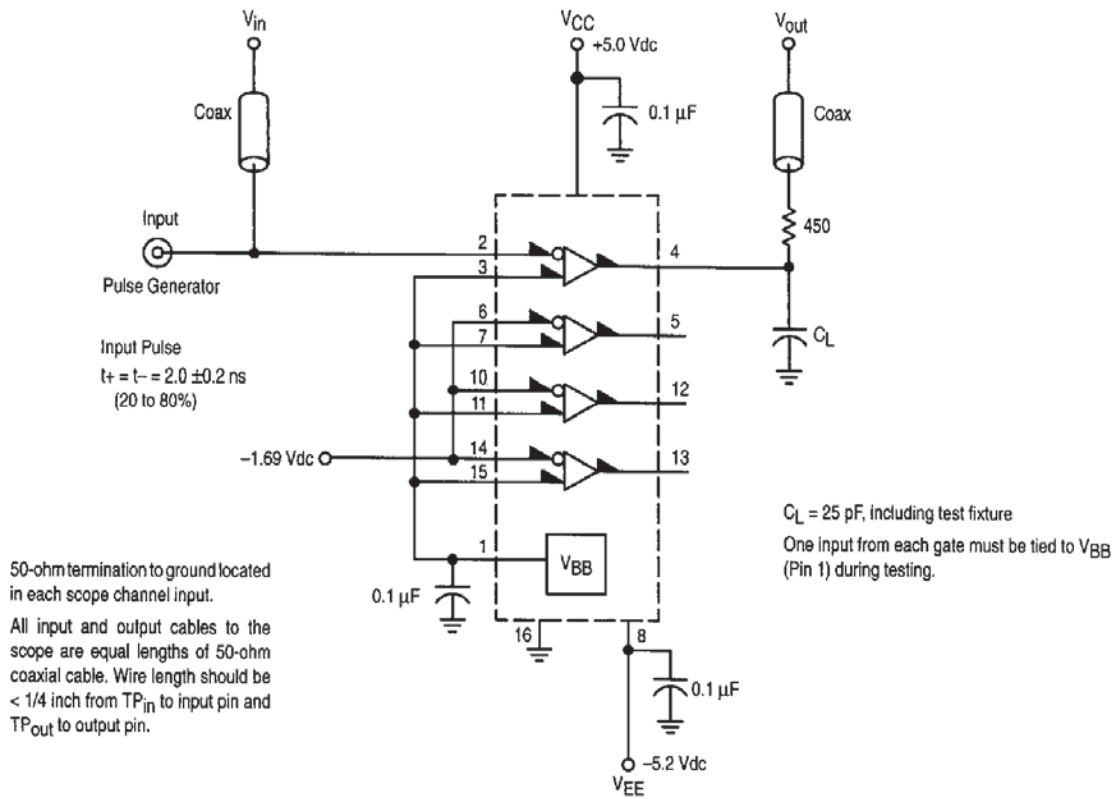
@ Test Temperature -30°C +25°C +85°C			TEST VOLTAGE VALUES (Volts)					Gnd	Output Condition
			V <sub>IHH</sub>	V <sub>ILH</sub>	V <sub>BB</sub>	V <sub>CC</sub>	V <sub>VEE</sub>		
			-1.890	-2.890	From Pin 1	+5.0	-5.2		
			-1.810	-2.850		+5.0	-5.2		
			-1.700	-2.825		+5.0	-5.2		
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					Gnd	Output Condition
			V <sub>IHH</sub>	V <sub>ILH</sub>	V <sub>BB</sub>	V <sub>CC</sub>	V <sub>VEE</sub>		
Negative Power Supply Drain Current	I <sub>E</sub>	8			3,7,11,15	9	8	16	
Positive Power Supply Drain Current	I <sub>OCH</sub>	9			3,7,11,15	9	8	16	
	I <sub>OCL</sub>	9			3,7,11,15	9	8	16	
Input Current	I <sub>inH</sub> <sup>1</sup>	2			3,7,11,15	9	8	16	
Input Leakage Current	I <sub>CBO</sub>	2			3,7,11,15	9	2,6,8,10,14	16	
High Output Voltage	V <sub>OH</sub>	4			3,7,11,15	9	8	16	-2.0mA
Low Output Voltage	V <sub>OL</sub>	4			3,7,11,15	9	8	16	20mA
High Threshold Voltage	V <sub>OHA</sub>	4			3,7,11,15	9	8	16	-2.0mA
Low Threshold Voltage	V <sub>OLA</sub>	4			3,7,11,15	9	8	16	20mA
Indeterminate Input Protection Tests	V <sub>OLS1</sub>	4				9	2,3,6,7,8,10,11,14,15	16	20mA
	V <sub>OLS2</sub>	4				9	8	16	20mA
Short Circuit Current	I <sub>OS</sub>	4			3,7,11,15	9	8	4, 16	
Reference Voltage	V <sub>BB</sub>	1			3,7,11,15				
Common Mode Rejection Tests	V <sub>OH</sub>	4				9	8	16	-2.0mA
		4	3	2		9	8	16	-2.0mA
	V <sub>OL</sub>	4				9	8	16	20mA
		4	2	3		9	8	16	20mA
Switching Times (50Ω Load)									
Propagation Delay (50% to +1.5Vdc)	t <sub>6+5-</sub>	5			3,7,11,15	9	8	16	
	t <sub>6-5+</sub>	5			3,7,11,15	9	8	16	
	t <sub>2+4-</sub>	4			3,7,11,15	9	8	16	
	t <sub>2-4+</sub>	4			3,7,11,15	9	8	16	
Rise Time (+1.0V to 2.0V)	t <sub>4+</sub>	4			3,7,11,15	9	8	16	
Fall Time (+1.0V to 2.0V)	t <sub>4-</sub>	4			3,7,11,15	9	8	16	

1. Individually test each output, apply V<sub>IHmax</sub> to pin under test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

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SWITCHING TIME TEST CIRCUIT



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