SN54104, SN54105, SN74104, SN74105

Gated J-K Master-Slave Flip-Flops

These J-K master-slave flip-flops feature a buffered clock input, direct preset and clear, gated J and K inputs, and a common JK input. The clock buffer offers typical TTL high noise immunity, low clock-line loading, and, in most cases, eliminates the need for stringent control of system-clock rise and fall times. When activated, the direct preset and clear inputs control the state of both the master and slave flip-flops independent of the clock and synchronous-input states. Gated inputs may be used to perform a wide variety of control functions without the need for external gates, and the common JK input simplifies hardware design for applications utilizing a single gate-control source.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

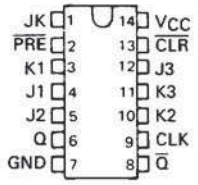
Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

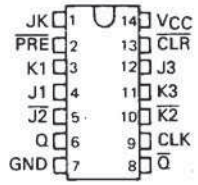
REVISED DECEMBER 1983

- **Buffered Clock Input**
- **Direct Preset and Clear**
- **Common JK Gate Input**

SN54104 . . . J OR W PACKAGE
SN74104 . . . J OR N PACKAGE



SN54105 . . . J OR W PACKAGE
SN74105 . . . J OR N PACKAGE



logic

FUNCTION TABLE

INPUT AT t_n			OUTPUT AT t_{n+1}	
JK	J†	K†	Q	$\overline{Q}$
L‡	X	X	Q_n	$\overline{Q}_n$
H	L‡	L‡	Q_n	$\overline{Q}_n$
H	L	H	L	H
H	H	L	H	L
H	H	H	$\overline{Q}_n$	Q_n

† SN54104/SN74104J = J1 · J2 · J3.
K = K1 · K2 · K3
SN54105/SN74105J = J1 · $\overline{J2}$ · J3.
K = K1 · $\overline{K2}$ · K3

‡ These low-levels must be maintained while the clock is low.

NOTES:
A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse
C. H = high, L = low, X = irrelevant

description

These J-K master-slave flip-flops feature a buffered clock input, direct preset and clear, gated J and K inputs, and a common JK input. The clock buffer offers typical TTL high noise immunity, low clock-line loading, and, in most cases, eliminates the need for stringent control of system-clock rise and fall times. When activated, the direct preset and clear inputs control the state of both the master and slave flip-flops independent of the clock and synchronous-input states. Gated inputs may be used to perform a wide variety of control functions without the need for external gates, and the common JK input simplifies hardware design for applications utilizing a single gate-control source.

Due to the internal clock buffer, the JK input gates accept data when the clock line is low, and transfer of data from the master to the slave occurs during the clock-line transition from the low state to the high state. When the clock line is high, the data inputs are inhibited.

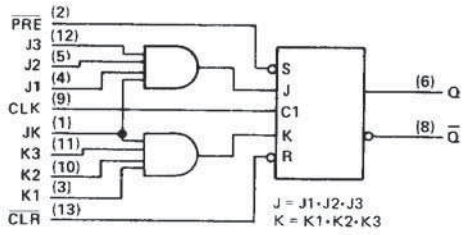
The SN54104/SN74104 includes internal capacitive loading on the J and K input gates and, as the input setup and hold times are lengthened, this circuit displays improved performance in systems where appreciable clock skew is anticipated.

The SN54105/SN74105 offers an inverting data input to each of the J and K input gates for additional control flexibility. As the input setup and hold times are not lengthened, this circuit permits operation at higher toggle rates than the SN54104/SN74104.

These TTL circuits feature one-volt typical d-c noise margins and are compatible for use with most TTL families. Full fan-out to 10 normalized Series 54/74 loads is available from the outputs. The SN54104 and SN54105 circuits are characterized for operation over the full military temperature range of −55°C to 125°C, and the SN74104 and SN74105 circuits are characterized for operation from 0°C to 70°C.

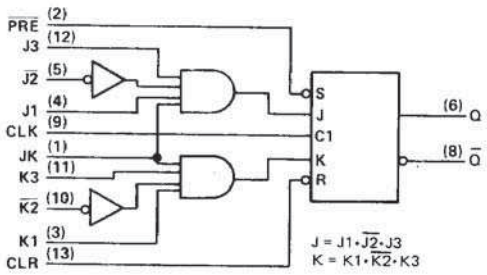
logic diagrams

'104



Pin numbers shown on logic notation are for J or N packages.

'105



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 8 V
Input voltage . . . . . 5.5 V
Voltage applied to any output (See Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54104, SN54105 Circuits . . . . . −55°C to 125°C
SN74104, SN74105 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54'			SN74'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 1)		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−1	mA
I_{OL}	Low-level output current				16			16	mA
t_w	Pulse duration	CLK Low-level	15†			15†			ns
		$\overline{PRE}$ and $\overline{CLR}$	20†			20†			
t_{su}	Setup time for high-level data (See Note 4)	'104	35†			35†			ns
		'105	10†			10†			
t_r	Release time for low-level data (See Note 3)	'104			10†			10†	ns
		'105			1†			1†	
T_A	Operating free-air temperature		−55		125	0		70	°C

† These conditions are recommended at V_{CC} = 5 V, T_A = 25°C.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This rating applied at the Q output with preset held low and at the $\overline{Q}$ output with clear held low.
3. Release time for low-level data is an interval between the release of low-level data and the positive-going edge of the clock pulse; this interval being sufficiently short to ensure recognition of the low-level data.
4. Setup time for high-level data is an interval between the arrival of the high-level data and the positive-going edge of the clock pulse; this interval being sufficiently long to ensure recognition of the high-level data.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{OH}		V_{CC} = MIN, I_{OH} = −1 mA	2.4	2.7		V
V_{OL}		V_{CC} = MIN, I_{OL} = 16 mA		0.2	0.4	V
I_{IH}	$\overline{PRE}$ or $\overline{CLR}$	V_{CC} = MAX, V_I = 4.5 V		8	120	μA
	J or K			4	80	
	All other			2	40	
I_{IL}	$\overline{PRE}$ or $\overline{CLR}$	V_{CC} = MAX, V_I = 0.4 V		−3	−4.75	mA
	J or K			−2.2	−3.2	
	All other			−1.1	−1.6	
I_{CC}	'104	V_{CC} = 5 V		15	24	mA
	'105			17	28	

† For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	CLK	Q or $\overline{Q}$	R_L = 400 Ω, C_L = 15 pF		9	15	ns
t_{PHL}					16	25	

NOTE 5: See General Information Section for load circuits and voltage waveforms.