SN5472, SN54H72, SN54L72, SN7472, SN74H72

AND-Gated J-K Master-Slave Flip-Flops with Preset and Clear

These J-K flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state. The SN5472, SN54H72, and the SN54L72 are characterized for operation over the full military temperature range of -55°C to 125°C while the SN7472 and the SN74H72 are characterized for operation from 0°C to 70°C.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

REVISED DECEMBER 1983

- **Package Options Include Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These J-K flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.

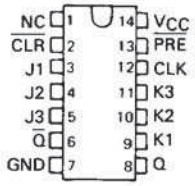
The SN5472, SN54H72, and the SN54L72 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7472 and the SN74H72 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

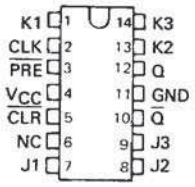
INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

† This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

SN5472, SN54H72, SN54L72 . . . J PACKAGE
SN7472, SN74H72 . . . J OR N PACKAGE
(TOP VIEW)

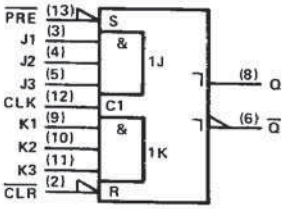


SN5472, SN54H72 . . . W PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol



Pin numbers shown are for J and N packages.

positive logic

$$J = J1 \cdot J2 \cdot J3$$
$$K = K1 \cdot K2 \cdot K3$$

3 TTL DEVICES

logic diagrams

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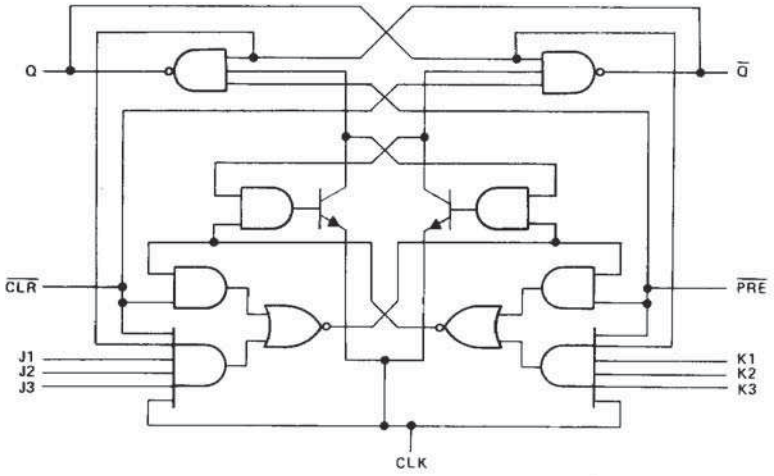

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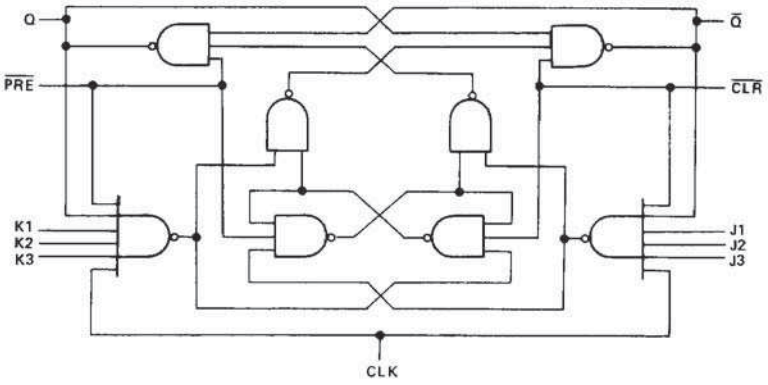

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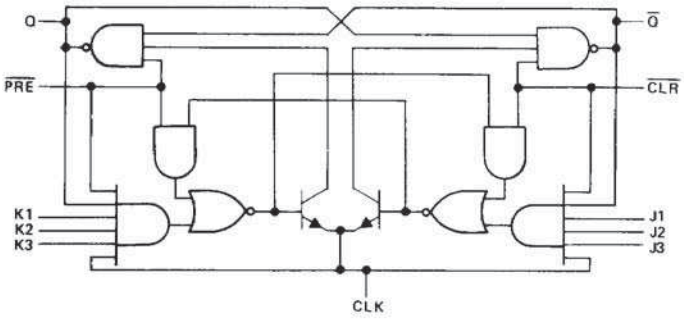

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schematics of inputs and outputs

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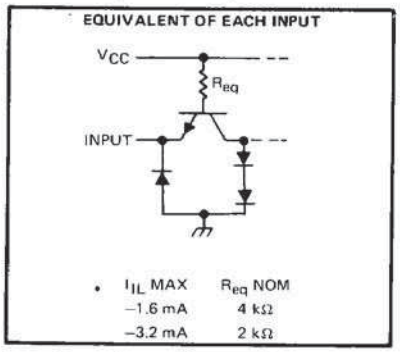

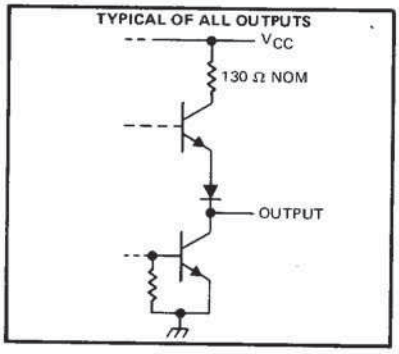

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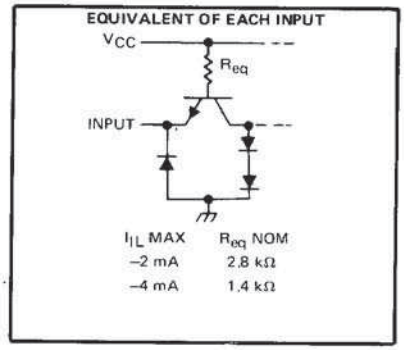

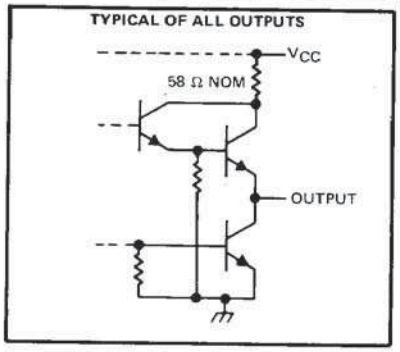

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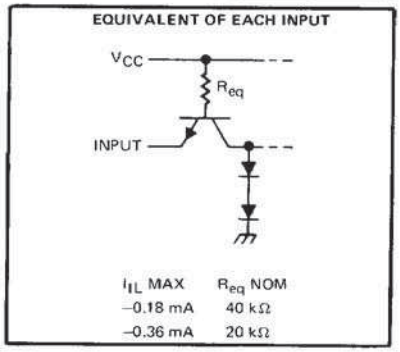

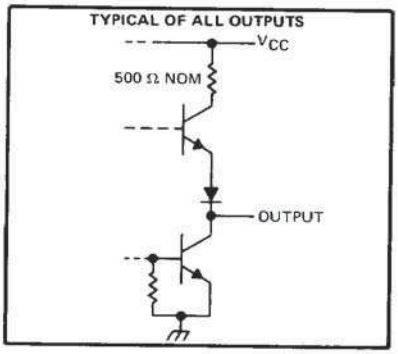

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN5472			SN7472			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				16			16	mA
t_w	Pulse duration	CLK high	20			20			ns
		CLK low	47			47			
		$\overline{PRE}$ or $\overline{CLR}$	25			25			
t_{su}	Input setup time before CLK↑		0			0			ns
t_h	Input hold time-data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †	SN5472			SN7472			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	J or K	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
	All other				80			80	
I_{IL}	J or K	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
	All other				−3.2			−3.2	
I_{OS}§		V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}		V_{CC} = MAX, See Note 2		10	20		10	20	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 400 Ω, C_L = 15 pF	15	20		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$			16	25	ns
t_{PHL}					25	40	ns
t_{PLH}	CLK	Q or $\overline{Q}$			16	25	ns
t_{PHL}					25	40	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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recommended operating conditions

			SN54H72			SN74H72			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.5			−0.5	mA
I_{OL}	Low-level output current				20			20	mA
t_w	Pulse duration	CLK high	12			12			ns
		CLK low	28			28			
		$\overline{CLR}$ or $\overline{PRE}$	16			16			
t_{su}	Setup time, before CLK↑	data high or low	0			0			ns
t_h	Hold time-data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †	SN54H72			SN74H72			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −8 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −0.5 mA	2.4	3.4		2.4	3.4		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA		0.2	0.4		0.2	0.4	V
I_I		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	J, K or CLK	V_{CC} = MAX, V_I = 2.4 V			50			50	μA
	$\overline{PRE}$ or $\overline{CLR}$★				100			100	
I_{IL}	J, K or CLR	V_{CC} = MAX, V_I = 0.4 V			−2			−2	mA
	$\overline{PRE}$ or $\overline{CLR}$★				−4			−4	
I_{OS}§		V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CC}		V_{CC} = MAX, See Note 2		16	25		16	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
★ Clear is tested with preset high and preset is tested with clear high.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 280 Ω, C_L = 25 pF	25	30		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$			6	13	ns
t_{PHL}					12	24	ns
t_{PLH}	CLK	Q or $\overline{Q}$			14	21	ns
t_{PHL}					22	27	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage	Clock input			0.6	V
		All other inputs			0.7	
I_{OH}	High-level output current				−0.1	mA
I_{OL}	Low-level output current				2	mA
t_w	Pulse duration	CLK high or low	200			ns
		$\overline{PRE}$ or $\overline{CLR}$ low	100			
t_{su}	Setup time before CLK ↑		0			ns
t_h	Hold time, data after CLK ↓		0			ns
T_A	Operating free-air temperature		−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †	MIN	TYP‡	MAX	UNIT
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −0.1 mA	2.4	3.3		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OL} = 2 mA		0.15	0.3	V
I_I	J or K	V_{CC} = MAX, V_I = 5.5 V			0.1	mA
	All other				0.2	
I_{IH}	J or K	V_{CC} = MAX, V_I = 2.4 V			10	μA
	$\overline{PRE}$ or $\overline{CLR}$				20	
	CLK				−200	
I_{IL}	J or K	V_{CC} = MAX, V_I = 0.3 V			−0.18	mA
	All other				−0.36	
I_{OS}		V_{CC} = MAX	−3		−15	mA
I_{CC}		V_{CC} = MAX, See Note 2		0.76	1.44	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 4 kΩ, C_L = 50 pF	2.5	3		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$			35	75	ns
t_{PHL}	$\overline{PRE}$ or $\overline{CLR}$ (CLK high)	$\overline{Q}$ or Q			60	150	ns
	$\overline{PRE}$ or $\overline{CLR}$ (CLK low)					200	
t_{PLH}	CLK	Q or $\overline{Q}$		10	35	75	ns
t_{PHL}				10	60	150	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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