SN54H108, SN74H108

Dual J-K Negative-Edge-Triggered Flip-Flops

These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, and asynchronous preset inputs to each flip-flop as well as common clock and asynchronous clear inputs. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

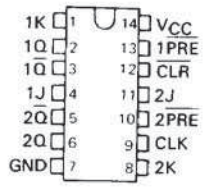
The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

TYPES SN54H108, SN74H108
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

REVISED DECEMBER 1983

- **Package Options Include Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54H108 . . . J OR W PACKAGE
SN74H108 . . . J OR N PACKAGE
(TOP VIEW)

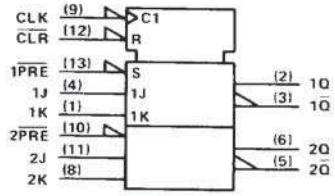


description

These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, and asynchronous preset inputs to each flip-flop as well as common clock and asynchronous clear inputs. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

The SN54H108 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74H108 is characterized for operation from 0°C to 70°C.

logic symbol



Pin numbers shown are for J and N packages.

3 TTL DEVICES

FUNCTION TABLE

INPUTS					OUTPUTS	
PRĒ	CLR̄	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

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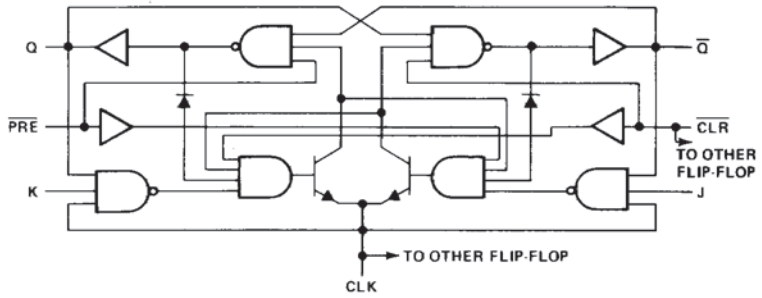
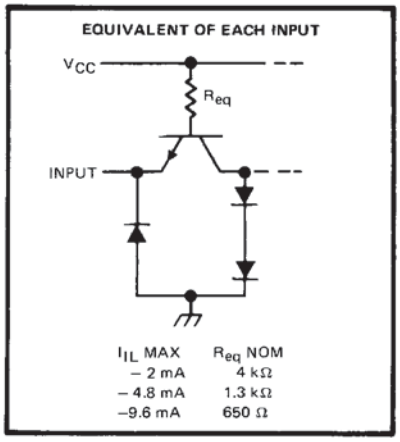
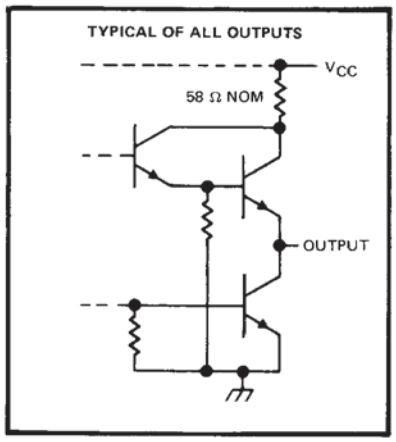
logic diagram



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54H' . . . . . −55°C to 125°C
SN74H' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54H108			SN74H108			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.5			−0.5	mA
I_{OL}	Low-level output current				20			20	mA
t_w	Pulse duration	CLK high	10			10			ns
		CLK low	15			15			
		$\overline{CLR}$ or $\overline{PRE}$ low	16			16			
t_{su}	Setup time before CLK ↓	High-level data	10			10			ns
		Low-level data	13			13			
t_h	Hold time-data after CLK ↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54H108			SN74H108			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −8 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −0.5 mA	2.4	3.4		2.4	3.4		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA		0.2	0.4		0.2	0.4	V
I_I		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	Any J or K	V_{CC} = MAX, V_I = 2.4 V			50			50	μA
	$\overline{CLR}$				200			200	
	$\overline{PRE}$				100			100	
	CLK		0		−1	0		−1	mA
I_{IL}	Any J or K	V_{CC} = MAX, V_I = 0.4 V		−1	−2		−1	−2	mA
	$\overline{CLR}$			−2	−4		−2	−4	
	$\overline{PRE}$			−1	−2		−1	−2	
	CLK			−6	−9.6		−6	−9.6	
I_{OS}§		V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CC}		V_{CC} = MAX, See Note 2		20	38		20	38	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 280 Ω, C_L = 25 pF	40	50		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$			8	12	ns
t_{PHL}	$\overline{PRE}$ or $\overline{CLR}$ (CLK high)	$\overline{Q}$ or Q			15	20	ns
	$\overline{PRE}$ or $\overline{CLR}$ (CLK low)				23	35	
t_{PLH}	CLK	Q or $\overline{Q}$			10	15	ns
t_{PHL}					16	20	

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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