# SN54290, SN54293, SN54LS290, SN54LS293
# SN74290, SN74293, SN74LS290, SN74LS293

*Decade and 4-Bit Binary Counters*

The SN54290/SN74290, SN54LS290/SN74LS290, SN54293/SN74293, and SN54LS293/SN74LS293 counters are electrically and functionally identical to the SN5490A/SN7490A, SN54LS90/SN74LS90, SN5493A/SN7493A, and SN54LS93/SN74LS93, respectively. Only the arrangement of the terminals has been changed for the ‘290, ‘LS290, ‘293, and ‘LS293.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the ‘290 and ‘LS290 and divide-by-eight for the ‘293 and ‘LS293. All of these counters have a gated zero reset and the ‘290 and ‘LS290 also have gated set-to-nine inputs for use in BCD nine’s complement applications.

## Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

## Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer’s datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. ‘Typical’ values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

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'290, 'LS290 . . . DECADE COUNTERS
'293, 'LS293 . . . 4-BIT BINARY COUNTERS

- GND and $V_{CC}$ on Corner Pins (Pins 7 and 14 Respectively)

## description

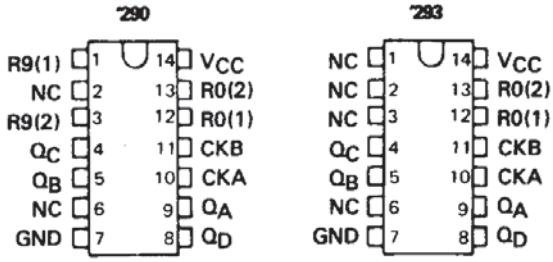
The SN54290/SN74290, SN54LS290/SN74LS290, SN54293/SN74293, and SN54LS293/SN74LS293 counters are electrically and functionally identical to the SN5490A/SN7490A, SN54LS90/SN74LS90, SN5493A/SN7493A, and SN54LS93/SN74LS93, respectively. Only the arrangement of the terminals has been changed for the '290, 'LS290, '293, and 'LS293.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '290 and 'LS290 and divide-by-eight for the '293 and 'LS293.

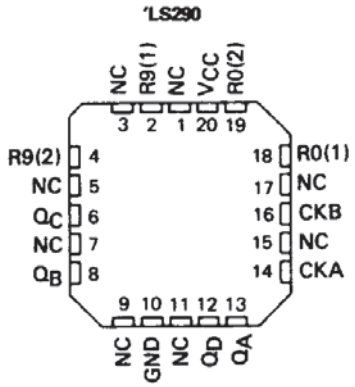
All of these counters have a gated zero reset and the '290 and 'LS290 also have gated set-to-nine inputs for use in BCD nine's complement applications.

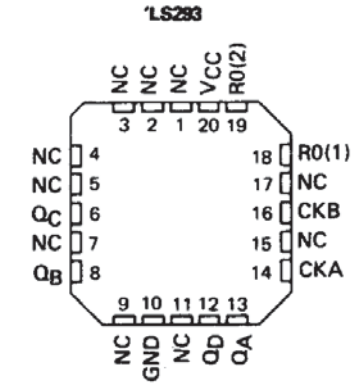
To use the maximum count length (decade or four-bit binary) of these counters, the B input is connected to the $Q_A$ output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '290 and 'LS290 counters by connecting the $Q_D$ output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output $Q_A$.

SN54290, SN54LS290, SN54293, SN54LS293 . . . J OR W PACKAGE
SN74290, SN74293 . . . N PACKAGE
SN74LS290, SN74LS293 . . . D OR N PACKAGE
(TOP VIEW)




SN54LS290, SN54LS293 . . . FK PACKAGE
(TOP VIEW)



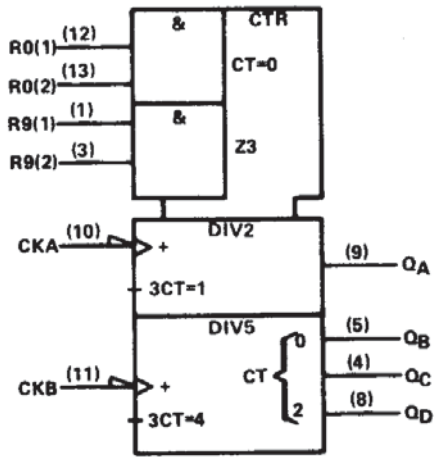

NC - No internal connection

2 TTL Devices

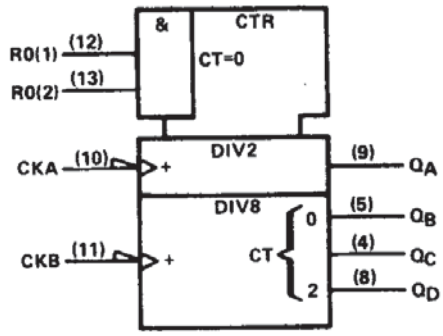
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

## logic symbols†

'290, 'LS290




'293, 'LS293




† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.





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**'290, 'LS290**
**BCD COUNT SEQUENCE**
**(See Note A)**

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

**'290, 'LS290**
**BI-QUINARY (5-2)**
**(See Note B)**

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | $Q_A$ | $Q_D$ | $Q_C$ | $Q_B$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

**'290, 'LS290**
**RESET/COUNT FUNCTION TABLE**

| RESET INPUTS | | | | OUTPUT | | | |
|---|---|---|---|---|---|---|---|
| $R_{0(1)}$ | $R_{0(2)}$ | $R_{9(1)}$ | $R_{9(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | X | L | L | L | L |
| H | H | X | L | L | L | L | L |
| X | X | H | H | H | L | L | H |
| X | L | X | L | COUNT | | | |
| L | X | L | X | COUNT | | | |
| L | X | X | L | COUNT | | | |
| X | L | L | X | COUNT | | | |

**'293, 'LS293**
**RESET/COUNT FUNCTION TABLE**

| RESET INPUTS | | OUTPUT | | | |
|---|---|---|---|---|---|
| $R_{0(1)}$ | $R_{0(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | L | L | L |
| L | X | COUNT | | | |
| X | L | COUNT | | | |

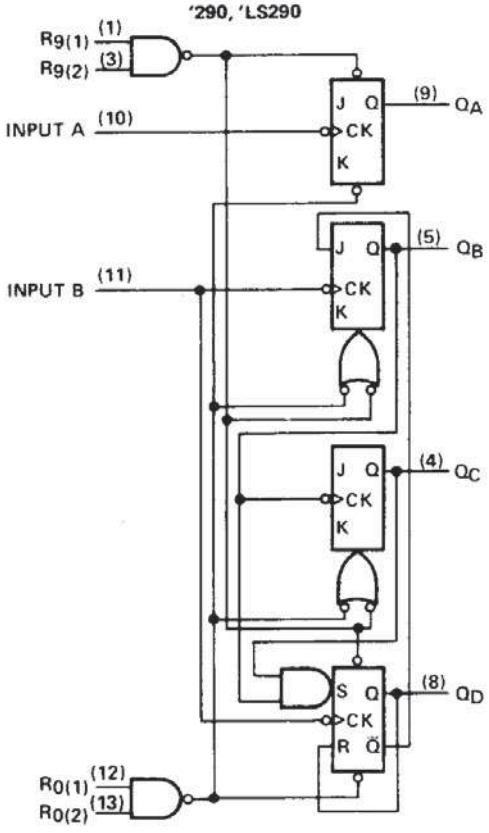
**'293, 'LS293**
**COUNT SEQUENCE**
**(See Note C)**

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

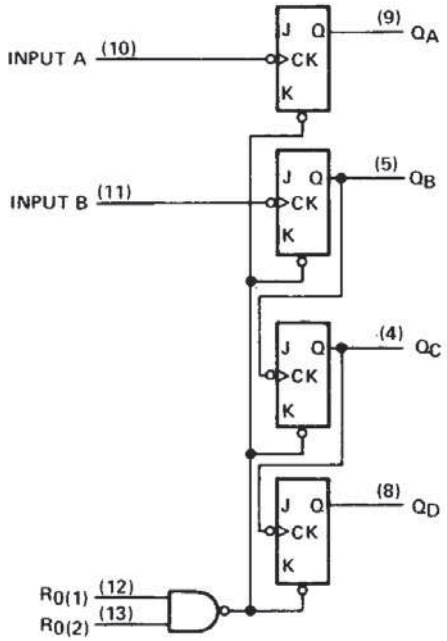
NOTES: A. Output $Q_A$ is connected to input B for BCD count.
B. Output $Q_D$ is connected to input A for bi-quinary count.
C. Output $Q_A$ is connected to input B.
D. H = high level, L = low level, X = irrelevant

**logic diagrams (positive logic)**

'290, 'LS290

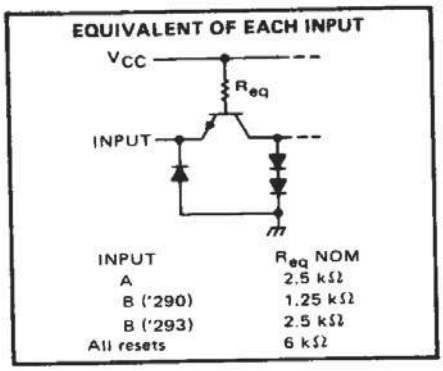


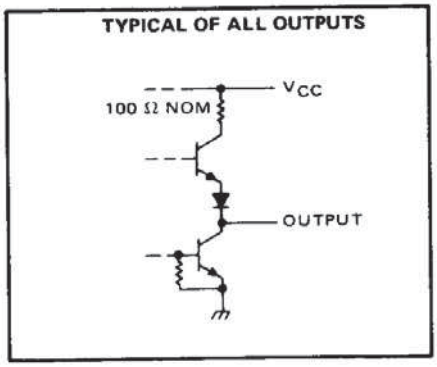

'293, 'LS293




Pin numbers shown are for D, J, N, and W packages.
The J and K inputs shown without connection are for reference only and are functionally at a high level.

## schematics of inputs and outputs






## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two $R_0$ inputs, and for the '290 circuit, it also applies between the two R9 inputs.

## recommended operating conditions

| | | SN54' | | | SN74' | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | | −800 | | | −800 | μA |
| Low-level output current, $I_{OL}$ | | | | 16 | | | 16 | mA |
| Count frequency, $f_{count}$ | A input | 0 | | 32 | 0 | | 32 | MHz |
| | B input | 0 | | 16 | 0 | | 16 | |
| Pulse width, $t_w$ | A input | 15 | | | 15 | | | ns |
| | B input | 30 | | | 30 | | | |
| | Reset inputs | 15 | | | 15 | | | |
| Reset inactive-state setup time, $t_{su}$ | | 25 | | | 25 | | | ns |
| Operating free-air temperature, $T_A$ | | −55 | | 125 | 0 | | 70 | °C |



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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS† | | '290 MIN | '290 TYP‡ | '290 MAX | '293 MIN | '293 TYP‡ | '293 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −800 μA | | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA¶ | | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | Any reset | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | | 40 | | | 40 | μA |
| | | A input | | | | | 80 | | | 80 | |
| | | B input | | | | | 120 | | | 80 | |
| $I_{IL}$ | Low-level input current | Any reset | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −1.6 | | | −1.6 | mA |
| | | A input | | | | | −3.2 | | | −3.2 | |
| | | B input | | | | | −4.8 | | | −3.2 | |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = MAX | SN54' | −20 | | −57 | −20 | | −57 | mA |
| | | | | SN74' | −18 | | −57 | −18 | | −57 | |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX, See Note 3 | | | 29 | 42 | | 26 | 39 | mA |

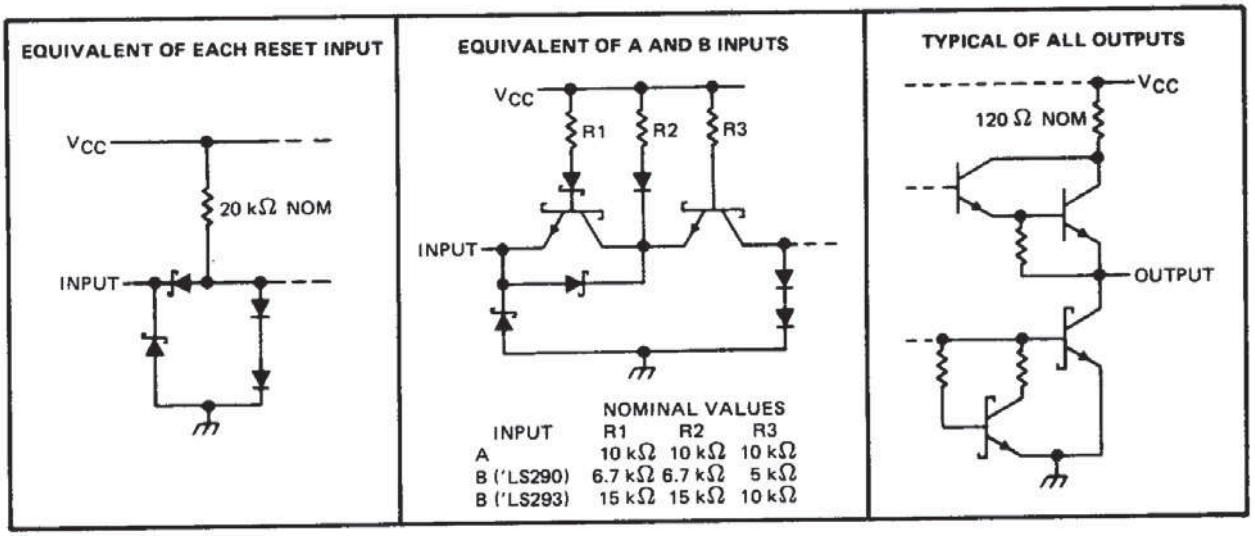
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time.
¶$Q_A$ outputs are tested at $I_{OL}$ = 16 mA plus the limit value of $I_{IL}$ for the B input. This permits driving the B input while maintaining full fan-out capability.
NOTE 3: $I_{CC}$ is measured with all outputs open, both $R_0$ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER# | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | '290 MIN | '290 TYP | '290 MAX | '293 MIN | '293 TYP | '293 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | A | $Q_A$ | $C_L$ = 15 pF, $R_L$ = 400 Ω, See Note 4 | 32 | 42 | | 32 | 42 | | MHz |
| | B | $Q_B$ | | 16 | | | 16 | | | |
| $t_{PLH}$ | A | $Q_A$ | | | 10 | 16 | | 10 | 16 | ns |
| $t_{PHL}$ | | | | | 12 | 18 | | 12 | 18 | |
| $t_{PLH}$ | A | $Q_D$ | | | 32 | 48 | | 46 | 70 | ns |
| $t_{PHL}$ | | | | | 34 | 50 | | 46 | 70 | |
| $t_{PLH}$ | B | $Q_B$ | | | 10 | 16 | | 10 | 16 | ns |
| $t_{PHL}$ | | | | | 14 | 21 | | 14 | 21 | |
| $t_{PLH}$ | B | $Q_C$ | | | 21 | 32 | | 21 | 32 | ns |
| $t_{PHL}$ | | | | | 23 | 35 | | 23 | 35 | |
| $t_{PLH}$ | B | $Q_D$ | | | 21 | 32 | | 34 | 51 | ns |
| $t_{PHL}$ | | | | | 23 | 35 | | 34 | 51 | |
| $t_{PHL}$ | Set-to-0 | Any | | | 26 | 40 | | 26 | 40 | ns |
| $t_{PLH}$ | Set-to-9 | $Q_A$, $Q_D$ | | | 20 | 30 | | | | ns |
| $t_{PHL}$ | | $Q_B$, $Q_C$ | | | 26 | 40 | | | | |

#$f_{max}$ = maximum count frequency
$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

## schematics of inputs and outputs






## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 5) . . . . . 7 V
Input voltage: R inputs . . . . . 7 V
A and B inputs . . . . . 5.5 V
Operating free-air temperature range: SN54LS290, SN54LS293 . . . . . −55°C to 125°C
SN74LS290, SN74LS293 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 5: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | | SN54LS' | | | SN74LS' | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | | −400 | | | −400 | μA |
| Low-level output current, $I_{OL}$ | | | | 4 | | | 8 | mA |
| Count frequency, $f_{count}$ | A input | 0 | | 32 | 0 | | 32 | MHz |
| | B input | 0 | | 16 | 0 | | 16 | |
| Pulse width, $t_w$ | A input | 15 | | | 15 | | | ns |
| | B input | 30 | | | 30 | | | |
| | Reset inputs | 30 | | | 30 | | | |
| Reset inactive-state setup time, $t_{su}$ | | 25 | | | 25 | | | ns |
| Operating free-air temperature, $T_A$ | | −55 | | 125 | 0 | | 70 | °C |



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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS† | | | SN54LS' | | | SN74LS' | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, | $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = $V_{IL}$ max, | $V_{IH}$ = 2 V, $I_{OH}$ = −400 μA | | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = $V_{IL}$ max, | $V_{IH}$ = 2 V, | $I_{OL}$ = 4 mA¶ | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | | | $I_{OL}$ = 8 mA¶ | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | Any reset | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| | | A input | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | | 0.2 | | | 0.2 | |
| | | B of 'LS290 | | | | | | 0.4 | | | 0.4 | |
| | | B of 'LS293 | | | | | | 0.2 | | | 0.2 | |
| $I_{IH}$ | High-level input current | Any reset | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| | | A input | | | | | | 40 | | | 40 | |
| | | B of 'LS290 | | | | | | 80 | | | 80 | |
| | | B of 'LS293 | | | | | | 40 | | | 40 | |
| $I_{IL}$ | Low-level input current | Any reset | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| | | A input | | | | | | −2.4 | | | −2.4 | |
| | | B of 'LS290 | | | | | | −3.2 | | | −3.2 | |
| | | B of 'LS293 | | | | | | −1.6 | | | −1.6 | |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = MAX | | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX, | See Note 3 | 'LS290 | | 9 | 15 | | 9 | 15 | mA |
| | | | | | 'LS293 | | 9 | 15 | | 9 | 15 | |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
¶$Q_A$ outputs are tested at specified $I_{OL}$ plus the limit value of $I_{IL}$ for the B input. This permits driving the B input while maintaining full fan-out capability.
NOTE 3: $I_{CC}$ is measured with all outputs open, both $R_0$ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER# | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | 'LS290 | | | 'LS293 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $f_{max}$ | A | $Q_A$ | $C_L$ = 15 pF, $R_L$ = 2 kΩ, See Note 4 | 32 | 42 | | 32 | 42 | | MHz |
| | B | $Q_B$ | | 16 | | | 16 | | | |
| $t_{PLH}$ | A | $Q_A$ | | | 10 | 16 | | 10 | 16 | ns |
| $t_{PHL}$ | | | | | 12 | 18 | | 12 | 18 | |
| $t_{PLH}$ | A | $Q_D$ | | | 32 | 48 | | 46 | 70 | ns |
| $t_{PHL}$ | | | | | 34 | 50 | | 46 | 70 | |
| $t_{PLH}$ | B | $Q_B$ | | | 10 | 16 | | 10 | 16 | ns |
| $t_{PHL}$ | | | | | 14 | 21 | | 14 | 21 | |
| $t_{PLH}$ | B | $Q_C$ | | | 21 | 32 | | 21 | 32 | ns |
| $t_{PHL}$ | | | | | 23 | 35 | | 23 | 35 | |
| $t_{PLH}$ | B | $Q_D$ | | | 21 | 32 | | 34 | 51 | ns |
| $t_{PHL}$ | | | | | 23 | 35 | | 34 | 51 | |
| $t_{PHL}$ | Set-to-0 | Any | | | 26 | 40 | | 26 | 40 | ns |
| $t_{PLH}$ | Set-to-9 | $Q_A$, $Q_D$ | | | 20 | 30 | | | | ns |
| $t_{PHL}$ | | $Q_B$, $Q_C$ | | | 26 | 40 | | | | |

#$f_{max}$ = maximum count frequency
$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
NOTE 4: Load circuits and voltage waveforms are shown in Section 1.