SN54LS640 thru SN54LS642, SN54LS644, SN54LS645
SN74LS640 thru SN74LS642, SN74LS644, SN74LS645

Octal Bus Transceivers

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

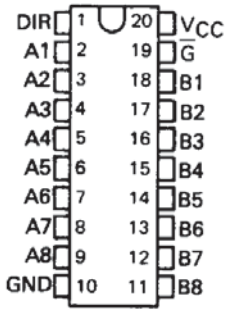
OCTAL BUS TRANSCEIVERS

D2420, APRIL 1979—REVISED MARCH 1988

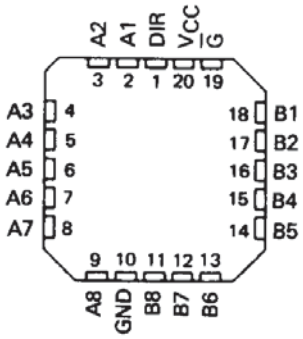
- **SN74LS64X-1 Versions Rated at I_{OL} of 48 mA**
- **Bi-directional Bus Transceivers in High-Density 20-Pin Packages**
- **Hysteresis at Bus Inputs Improves Noise Margins**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**

DEVICE	OUTPUT	LOGIC
'LS640	3-State	Inverting
'LS641	Open-Collector	True
'LS642	Open-Collector	Inverting
'LS644	Open-Collector	True and inverting
'LS645	3-State	True

SN54LS' . . . J PACKAGE
SN74LS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS' . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C.

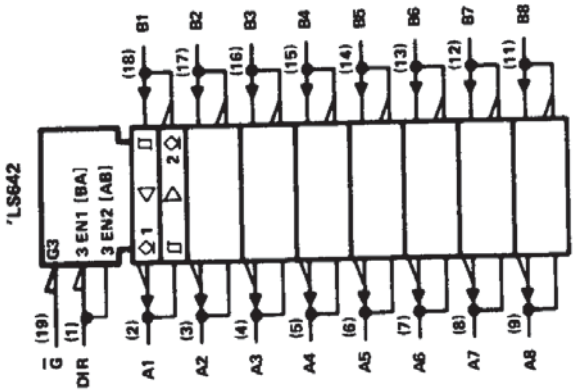
FUNCTION TABLE

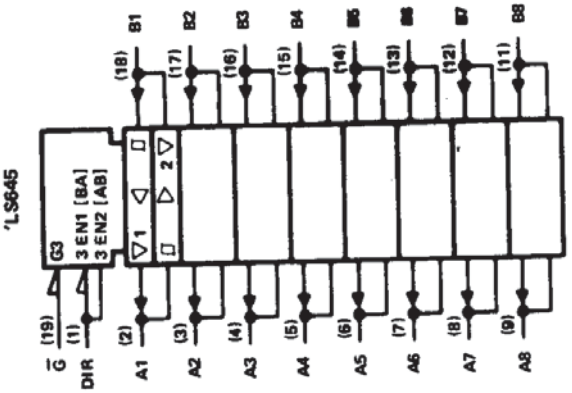
CONTROL INPUTS		OPERATION		
$\overline{G}$	DIR	'LS640 'LS642	'LS641 'LS645	'LS644
L	L	$\overline{B}$ data to A bus	B data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

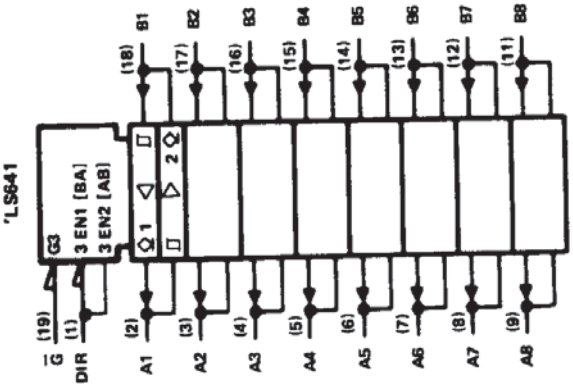
H = high level, L = low level, X = irrelevant

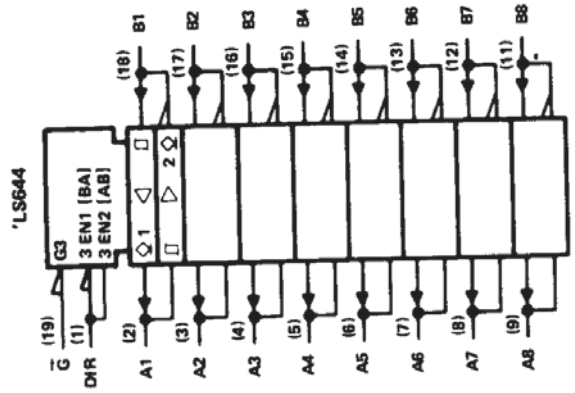
2 TTL Devices

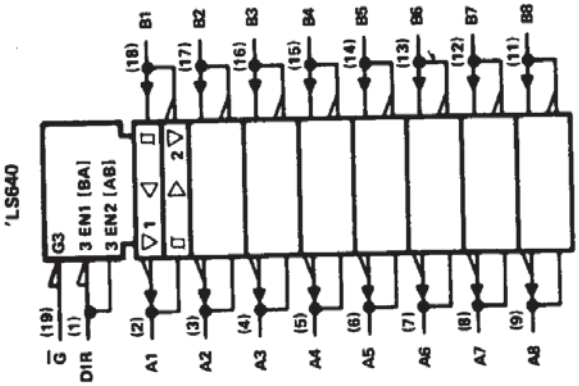
logic symbols†











† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

TEXAS INSTRUMENTS
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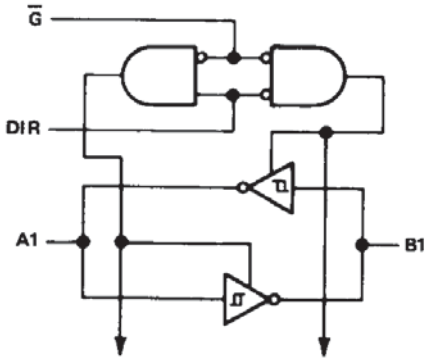
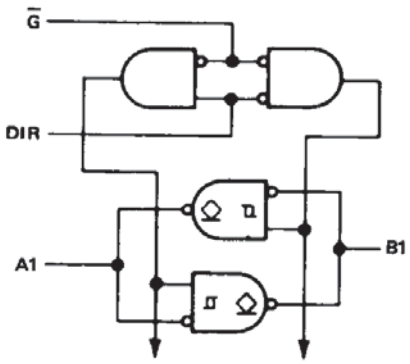
logic diagrams (positive logic)

'LS640



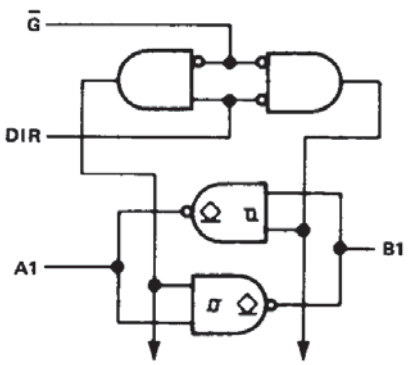
TO SEVEN OTHER TRANSCEIVERS

'LS641



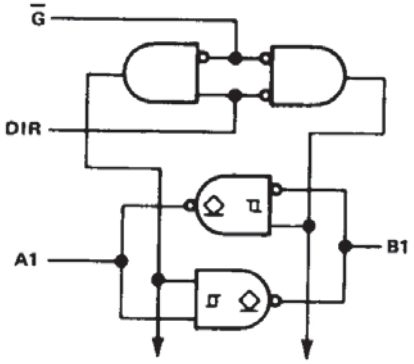
TO SEVEN OTHER TRANSCEIVERS

'LS642



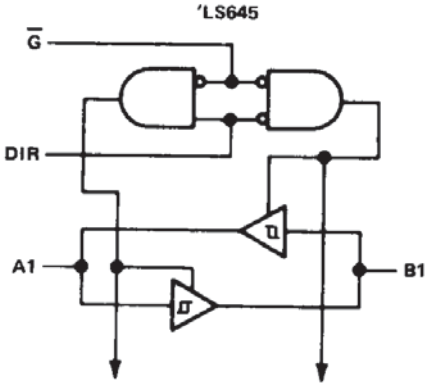
TO SEVEN OTHER TRANSCEIVERS

'LS644



TO SEVEN OTHER TRANSCEIVERS

'LS645



TO SEVEN OTHER TRANSCEIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54LS640, SN54LS645 . . . . . −55°C to 125°C
SN74LS640, SN74LS645 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER		SN54LS640 SN54LS645			SN74LS640 SN74LS645			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-lvel input voltage	2			2			V
V_{IL}	Low-level input voltage			0.5			0.6	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The 48-mA limit applies for the SN74LS640-1 and SN74LS645-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡			SN54LS640 SN54LS645			SN74LS640 SN74LS645			UNIT
					MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA					−1.5			−1.5	V
Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN,		A or B input	0.1	0.4		0.2	0.4		V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX		I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX		I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
				I_{OL} = 48 mA#					0.4	0.5	
I_{OZH}		V_{CC} = MAX, $\overline{G}$ at 2 V,		V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = MAX, $\overline{G}$ at 2 V,		V_O = 0.4 V			−0.4			−0.4	mA
I_I	A or B	V_{CC} = MAX		V_I = 5.5 V			0.1			0.1	mA
	DIR or $\overline{G}$			V_I = 7 V			0.1			0.1	
I_{IH}		V_{CC} = MAX, V_{IH} = 2.7 V					20			20	μA
I_{IL}		V_{CC} = MAX, V_{IL} = 0.4 V					−0.4			−0.4	mA
I_{OS}¶		V_{CC} = MAX			−40		−225	−40		−225	mA
I_{CC}	Outputs high	V_{CC} = MAX, Outputs open				48	70		48	70	mA
	Outputs low					62	90		62	90	
	Outputs at Hi-Z					64	95		64	95	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
#The 48-mA condition applies for the SN74LS640-1 and SN74LS645-1 only.

TEXAS INSTRUMENTS
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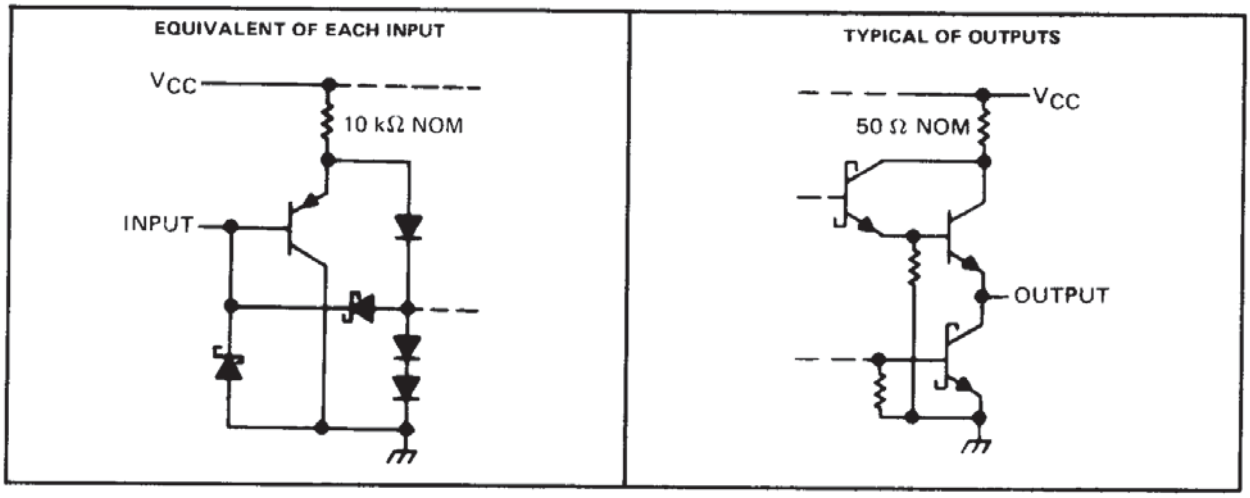
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS640, 'LS640-1			'LS645, 'LS645-1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	C_L = 45 pF, R_L = 667 Ω, See Note 2		6	10		8	15	ns
		B	A			6	10		8	15	
t_{PHL}	Propagation delay time, high-to-low-level output	A	B			8	15		11	15	ns
		B	A			8	15		11	15	
t_{PZL}	Output enable time to low level	$\overline{G}$	A			31	40		31	40	ns
		$\overline{G}$	B			31	40		31	40	
t_{PZH}	Output enable time to high level	$\overline{G}$	A			23	40		26	40	ns
		$\overline{G}$	B			23	40		26	40	
t_{PLZ}	Output disable time from low level	$\overline{G}$	A	C_L = 5 pF, R_L = 667 Ω, See Note 2		15	25		15	25	ns
		$\overline{G}$	B			15	25		15	25	
t_{PHZ}	Output disable time from high level	$\overline{G}$	A			15	25		15	25	ns
		$\overline{G}$	B			15	25		15	25	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



TYPICAL CHARACTERISTICS

SN54LS'
INVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

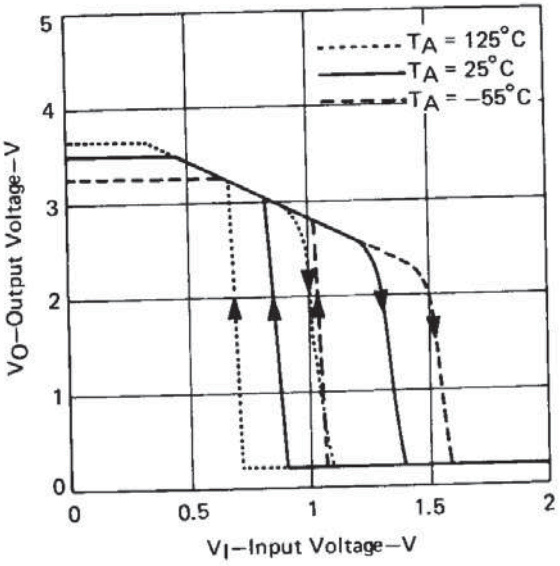


FIGURE 1

SN74LS'
INVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

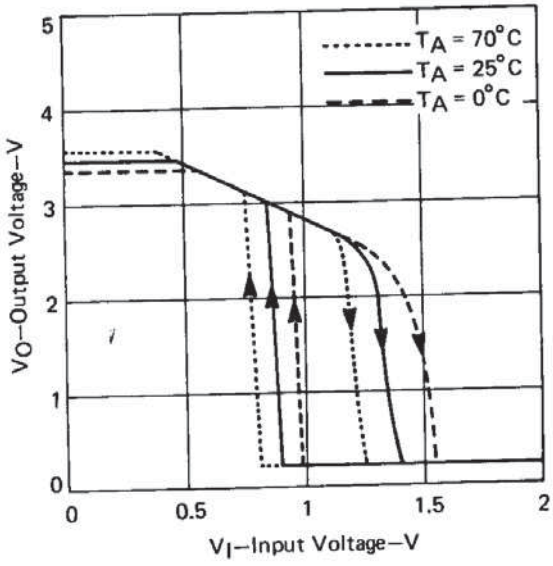


FIGURE 2

SN54LS'
NONINVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

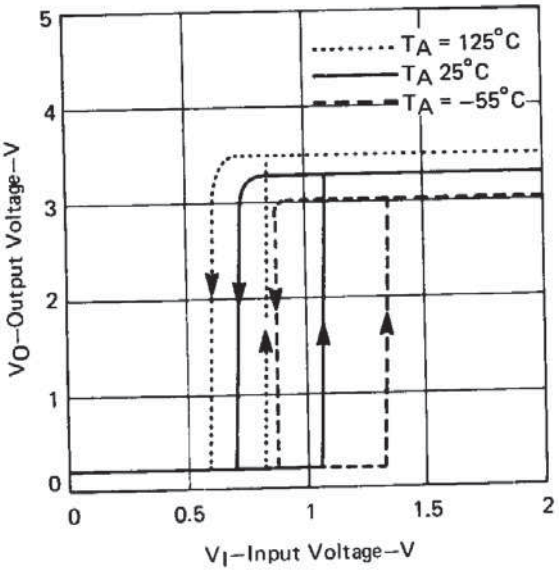


FIGURE 3

SN74LS'
NONINVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

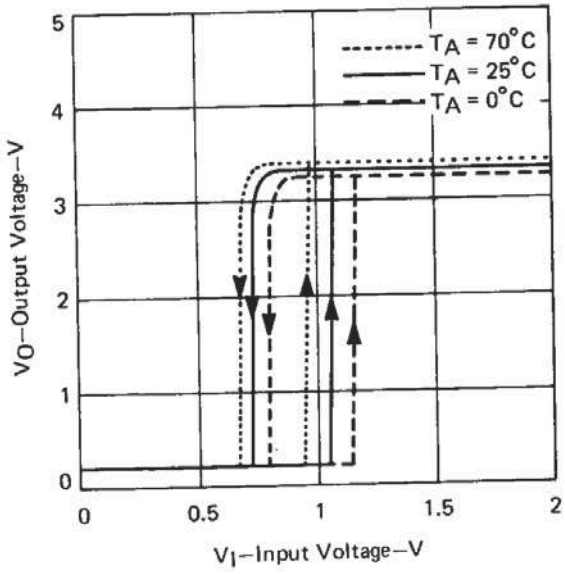


FIGURE 4

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54LS641, SN54LS642, SN54LS644 . . . . . −55°C to 125°C
SN74LS641, SN74LS642, SN74LS644 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER		SN54LS641 SN54LS642 SN54LS644			SN74LS641 SN74LS642 SN74LS644			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.5			0.6	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
							48§	
T_A	Operating free-air temperature	−55		125	0		70	°C

§The 48 mA limit applies for the SN74LS641-1, SN74LS642-1, and SN74LS644-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS641 SN54LS642 SN54LS644			SN74LS641 SN74LS642 SN74LS644			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN,	A or B input	0.1	0.4		0.2	0.4		V
I_{OH}		V_{CC} = MIN, V_{IL} = MAX,	V_{IH} = 2 V, V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = MIN,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{IH} = 2 V,	I_{OL} = 24 mA					0.35	0.5	
		V_{IL} = MAX	I_{OL} = 48 mA§					0.4	0.5	
I_I	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
	DIR or $\overline{G}$		V_I = 7 V			0.1			0.1	
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{CC}	Outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70	mA
	Outputs low				62	90		62	90	
	Outputs at Hi-Z				64	95		64	95	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The 48 mA condition applies for the SN74LS641-1, SN74LS642-1, and SN74LS644-1 only.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS641, 'LS641-1			'LS642, 'LS642-1			'LS644, 'LS644-1			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	A	B	C_L = 45 pF, R_L = 667 Ω, See Note 2		17	25		19	25		17	25	ns
	B	A			17	25		19	25		19	25	
t_{PHL} Propagation delay time, high-to-low-level output	A	B			16	25		14	25		14	25	ns
	B	A			16	25		14	25		16	25	
t_{PLH} Output disable time from low level	$\overline{G}$, DIR	A			23	40		26	40		26	40	ns
	$\overline{G}$, DIR	B			25	40		28	40		25	40	
t_{PHL} Output enable time from high level	$\overline{G}$, DIR	A			34	50		43	60		43	60	ns
	$\overline{G}$, DIR	B			37	50		39	60		37	50	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

TYPICAL OF OUTPUTS

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