SN54S226, SN74S226

4-Bit Parallel Latched Bus Transceivers

These high-performance Schottky TTL quadruple bus transceivers employ dual-rank bidirectional four-bit transparent latches and feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The bus-management functions implemented and the high-impedance controls offered provide the designer with a controller/transceiver that interfaces and drives system bus-organized lines directly. They are particularly attractive for implementing bidirectional transceivers and data-bus controllers.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

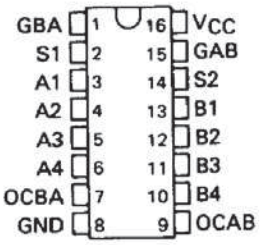
Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

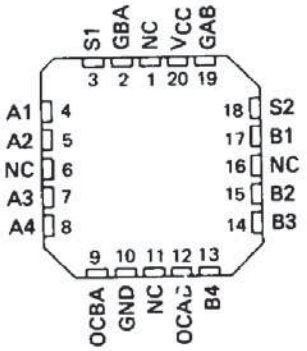
OCTOBER 1976—REVISED DECEMBER 1983

- Universal Transceivers for Implementing System Bus Controllers
- Dual-Rank 4-Bit Transparent Latches Provide:
  - Exchange of Data Between 2 Buses In One Clock Pulse
  - Bus-to-Bus Isolation
  - Rapid Data Transfer
  - Full Storage Capability
- Hysteresis at Data Inputs Enhances Noise Rejection
- Separate Output-Control Inputs Provide Independent Enable/Disable for Either Bus Output
- 3-State Outputs Drive Bus Lines Directly

SN54S226 . . . J OR W PACKAGE
SN74S226 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54S226 . . . FK PACKAGE
SN74S226 . . . FN PACKAGE
(TOP VIEW)



NC - No internal correction

description

These high-performance Schottky TTL quadruple bus transceivers employ dual-rank bidirectional four-bit transparent latches and feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The bus-management functions implemented and the high-impedance controls offered provide the designer with a controller/transceiver that interfaces and drives system bus-organized lines directly. They are particularly attractive for implementing:

Bidirectional bus transceivers
Data-bus controllers

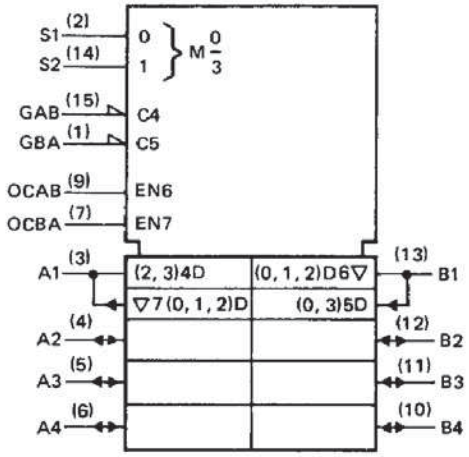
The bus-management functions, under control of the function-select (S1, S2) inputs, provide complete data integrity for each of the four modes described in the function table. Directional transparency provides for routing data from or to either bus, and the dual store and dual readout capabilities can be used to perform the exchange of data between the two bus lines in the equivalent of a single clock pulse. Storage of data is accomplished by selecting the latch function, setting up the data, and taking the appropriate strobe input low. As long as the strobe is held high, the data is latched for the selected function. Further control is offered through the availability of independent output controls that can be used to enable or disable the outputs as shown in the output-control function table, regardless of the latch function in process. Store operations can be performed with the outputs disabled to a high impedance (Hi-Z). In the Hi-Z state the inputs/outputs neither load nor drive the bus lines significantly. The p-n-p inputs feature typically 400 millivolts of hysteresis to enhance noise rejection.

BUS-MANAGEMENT FUNCTION TABLE

MODE CONTROLS S2	S1	STROBES GAB	GBA	A-TO-B LATCHES 1	2	B-TO-A LATCHES 1	2	OPERATION
L	L	X	L	Latch	Trans	Trans	Trans	Pass B to A
			H			Latch	Trans	Read out stored data
L	H	X	X	Latch	Trans	Latch	Trans	Read out stored data
H	L	L	X	Trans	Trans	Latch	Trans	Pass A to B
		H		Latch	Trans			Read out stored data
H	H	L	L	Trans	Latch	Trans	Latch	Read in both buses
		H	H	Latch	Latch	Latch	Latch	Store bus data

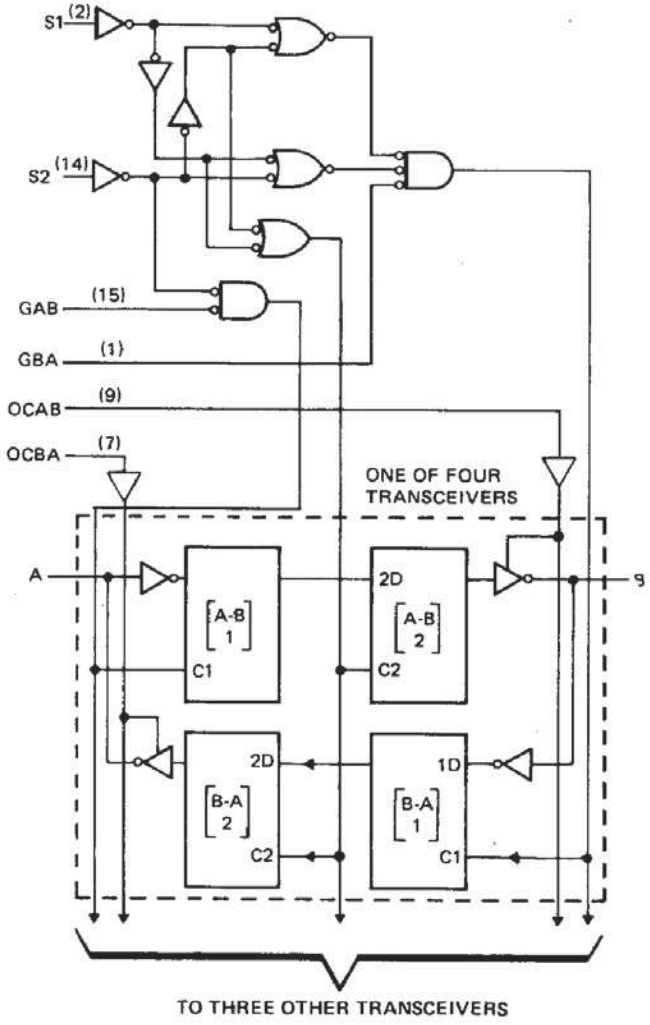
H = high level L = low level X = irrelevant Latch = latched Trans = transparent

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

logic diagram (positive logic)



Pin numbers shown on logic notation are for D, J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54S226 (see Note 2)	−55°C to 125°C
SN74S226	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54S226 in the J package operating at temperatures above 113°C requires a heat-sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 48°C/W.

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recommended operating conditions

		SN54S226			SN74S226			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−6.5			−10.3	mA
Width of strobe pulse		30			20			ns
Setup time, t_{su}	To Strobe	30↑			20↑			ns
	To Select	30			20			
Hold time, t_h	To Strobe	0↑			0↑			ns
	To Select	0			0			
Operating free-air temperature, T_A (see Note 2)		−55		125	0		70	°C

↑ The arrow indicates that the low-to-high transition of the strobe input is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	SN54S226	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	2.4	3.3		V
		SN74S226		2.4	2.9		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 15 mA			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V			100	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V			−250	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V			100	μA
I_{IL}	Low-level input current	GAB, GBA	V_{CC} = MAX, V_I = 0.5 V			−0.38	mA
		All other inputs				−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−50		−180	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		125	185	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTES: 2. An SN54S226 in the J package operating at temperatures above 113°C requires a heat-sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 48°C/W.
3. I_{CC} is measured with all inputs (and outputs) grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

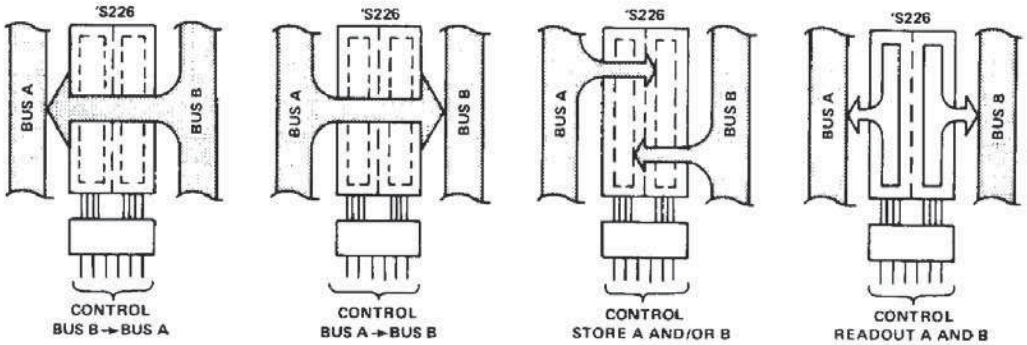
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	B or A	C_L = 50 pF, R_L = 280 Ω, See Note 4		20	30	ns
t_{PHL}					15	30	
t_{PLH}	Select	Any			25	37	ns
t_{PHL}					19	30	
t_{PLH}	Strobe GBA or GAB	A or B			25	37	ns
t_{PHL}					19	30	
t_{PZH}	Output Control OCBA or OCAB	A or B			12	20	ns
t_{PZL}					12	20	
t_{PHZ}	Output Control OCBA or OCAB	A or B	C_L = 5 pF, R_L = 280 Ω, See Note 4		10	15	ns
t_{PLZ}					10	15	

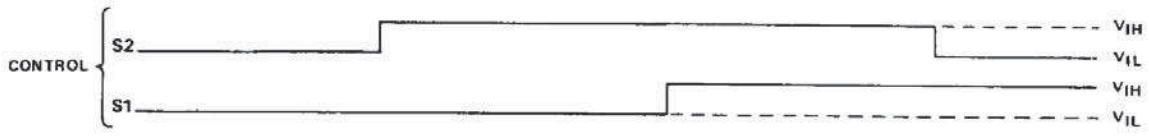
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low level
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level
NOTE 4: See General Information Section for load circuits and voltage waveforms.

applications

3 TTL DEVICES

The following examples demonstrate four fundamental bus-management functions that can be performed with the 'S226. Exchange of data on the two bus lines can be accomplished with a single high-to-low transition at S2 when S1 is high.





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