

SN54S64, SN54S65, SN74S64, SN74S65

4-2-3-2 Input AND-OR-INVERT Gates

These devices contain 4-2-3-2 input AND-OR-INVERT gates. They perform the Boolean function $Y=ABCD+EF+GHI+JK$. The 'S64 has totem-pole outputs and the 'S65 has open-collector outputs. The SN54S64 and the SN54S65 are characterized for operation over the full military temperature range of -55°C to 125°C while the SN74S64 and the SN74S65 are characterized for operation from 0°C to 70°C.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

**SN54S64, SN54S65,
SN74S64, SN74S65**
4-2-3-2 INPUT AND-OR-INVERT GATES
SDLS205 - DECEMBER 1983 - REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs

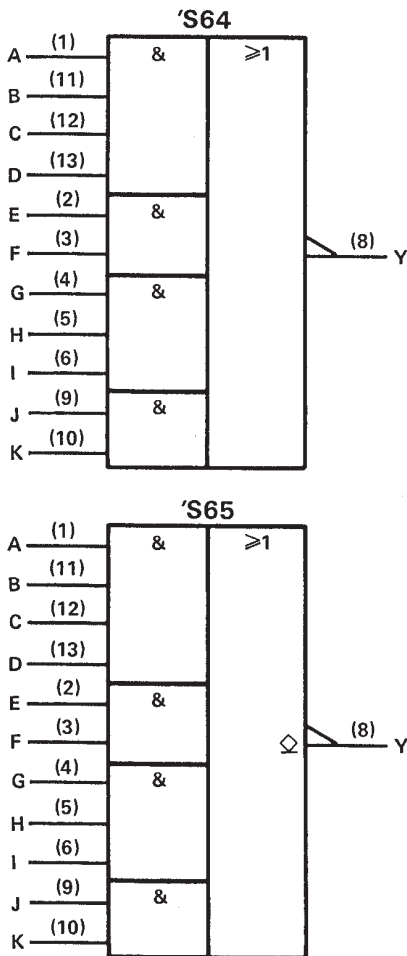
- Dependable Texas Instruments Quality and Reliability

description

These devices contain 4-2-3-2 input AND-OR-INVERT gates. They perform the Boolean function $Y = \overline{ABCD + EF + GHI + JK}$. The 'S64 has totem-pole outputs and the 'S65 has open-collector outputs.

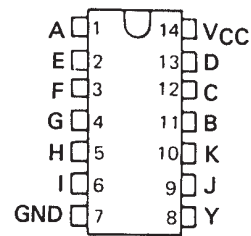
The SN54S64 and the SN54S65 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74S64 and the SN74S65 are characterized for operation from 0°C to 70°C.

logic symbols†

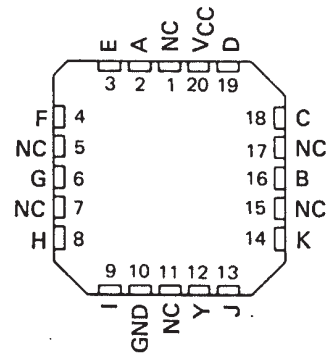


†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

SN54S64, SN54S65 . . . J OR W PACKAGE
SN74S64, SN74S65 . . . D OR N PACKAGE
(TOP VIEW)

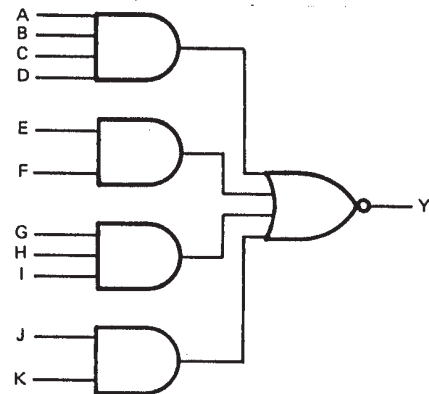


SN54S64, SN54S65 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

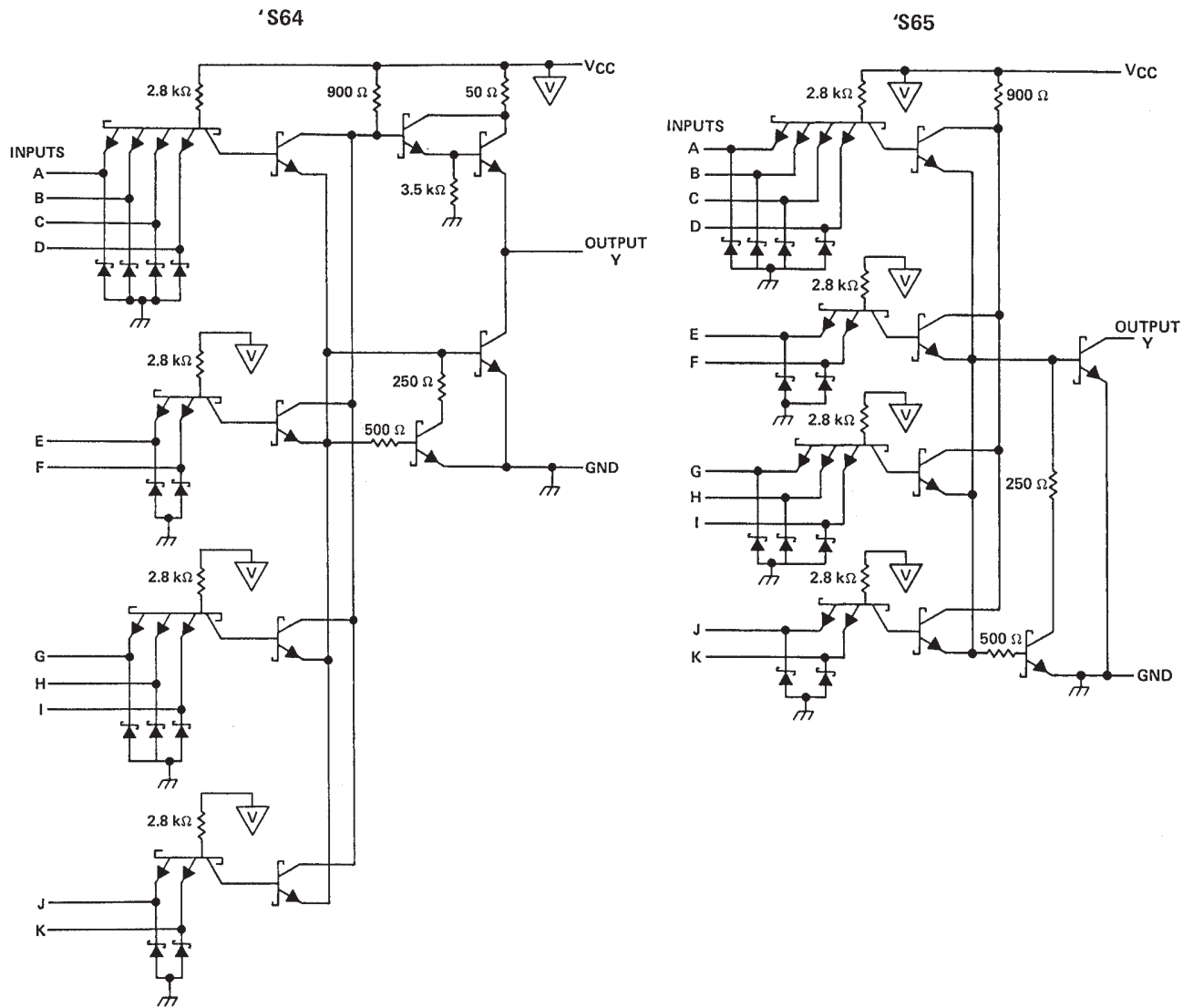
logic diagram (each device) (positive logic)



**SN54S64, SN54S65,
SN74S64, SN74S65**
4-2-3-2 INPUT AND-OR-INVERT GATES

SDLS205 – DECEMBER 1983 – REVISED MARCH 1988

schematics (each gate)



Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage, 'S65	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C



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SN54S64, SN54S65 4-2-3-2 INPUT AND-OR-INVERT GATES

SDLS205 – DECEMBER 1983 – REVISED MARCH 1988

recommended operating conditions

	SN54S64			SN74S64			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			-1			-1	mA
I_{OL} Low-level output current			20			20	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S64		SN74S64		UNIT		
		MIN	TYP ‡	MAX	MIN		TYP ‡	MAX
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2		-1.2	V	
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4	V	
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5		0.5	V	
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1		1	mA	
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50		50	μA	
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2		-2	mA	
$I_{OS} §$	$V_{CC} = \text{MAX}$	-40		-100	-40	-100	mA	
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0$		7	12.5		7	12.5	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		8.5	16		8.5	16	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH}	Any	Y	$R_L = 280 \Omega, C_L = 15 \text{ pF}$		3.5	5.5	ns	
t_{PHL}					3.5	5.5	ns	
t_{PLH}			$R_L = 280 \Omega, C_L = 50 \text{ pF}$			5		ns
t_{PHL}						5.5		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

SN54S65, SN74S65

4-2-3-2 INPUT AND-OR-INVERT GATES

SDLS205 – DECEMBER 1983 – REVISED MARCH 1988

recommended operating conditions

	SN54S65			SN74S65			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
V _{OH} High-level output voltage			5.5			5.5	V
I _{OL} Low-level output current			20			20	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S65			SN74S65			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IK}	V _{CC} = MIN, I _I = -18 mA			1.2			1.2	V	
I _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, V _{OH} = 5.5 V						0.25	mA	
	V _{CC} = MIN, V _{IL} = 0.7 V, V _{OH} = 5.5 V			0.25					
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 20 mA	0.2	0.4		0.2	0.4		V	
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA	
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			50			50	μA	
I _{IL}	V _{CC} = MAX, V _I = 0.5 V			-2			-2	mA	
I _{CCH}	V _{CC} = MAX, V _I = 0			6	11		6	11	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V			8.5	16		8.5	16	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	Any	Y	R _L = 280 Ω,	C _L = 15 pF	2	5	7.5	ns
t _{PHL}					2	5.5	8.5	ns
t _{PLH}			R _L = 280 Ω,	C _L = 50 pF	8		ns	
t _{PHL}					6.5		ns	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
JM38510/07402BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
JM38510/07402BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SN54S64J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN74S64D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74S64DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74S64N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74S64N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74S65D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74S65DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74S65N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SNJ54S64FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54S64J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SNJ54S64W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

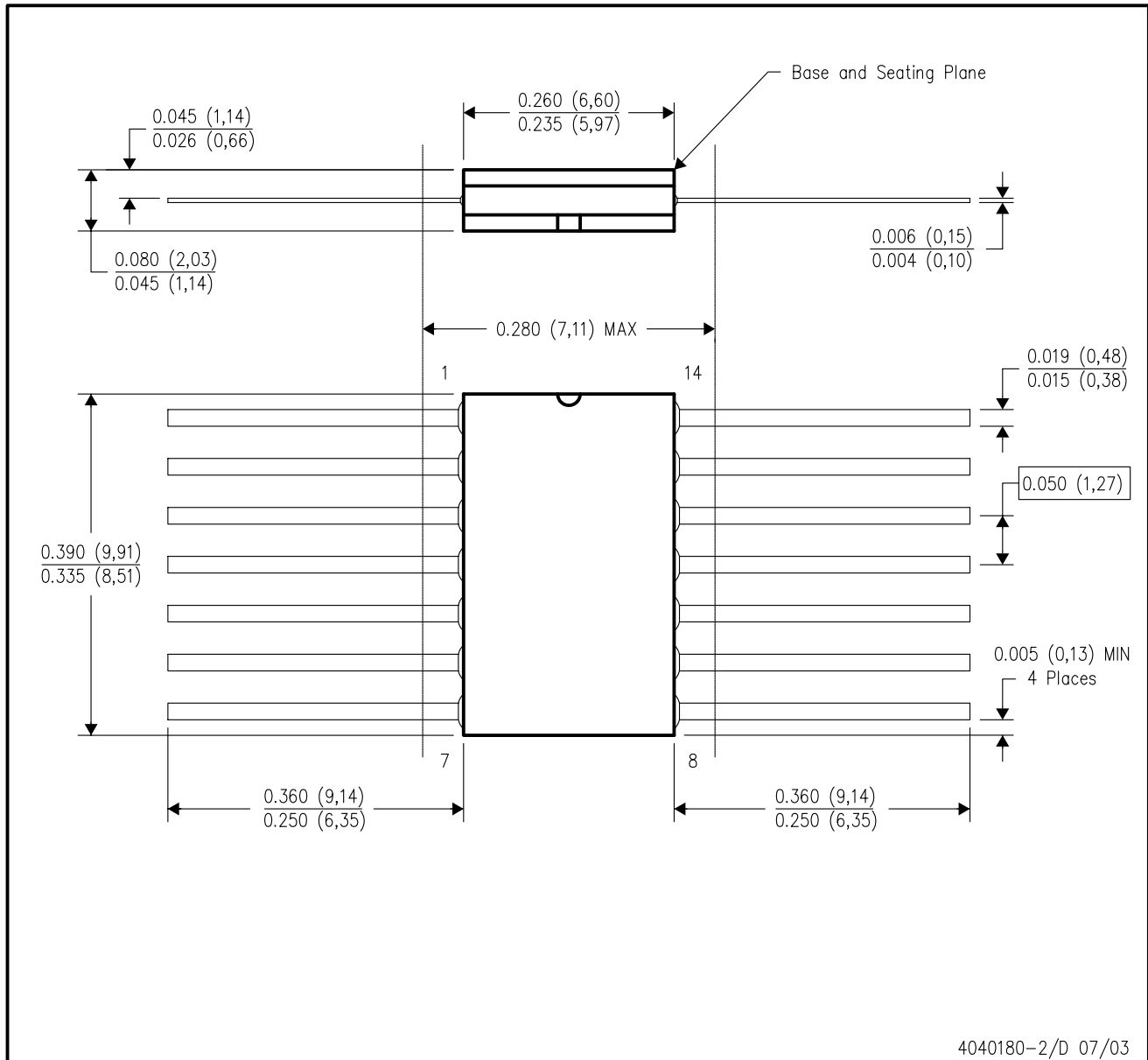


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

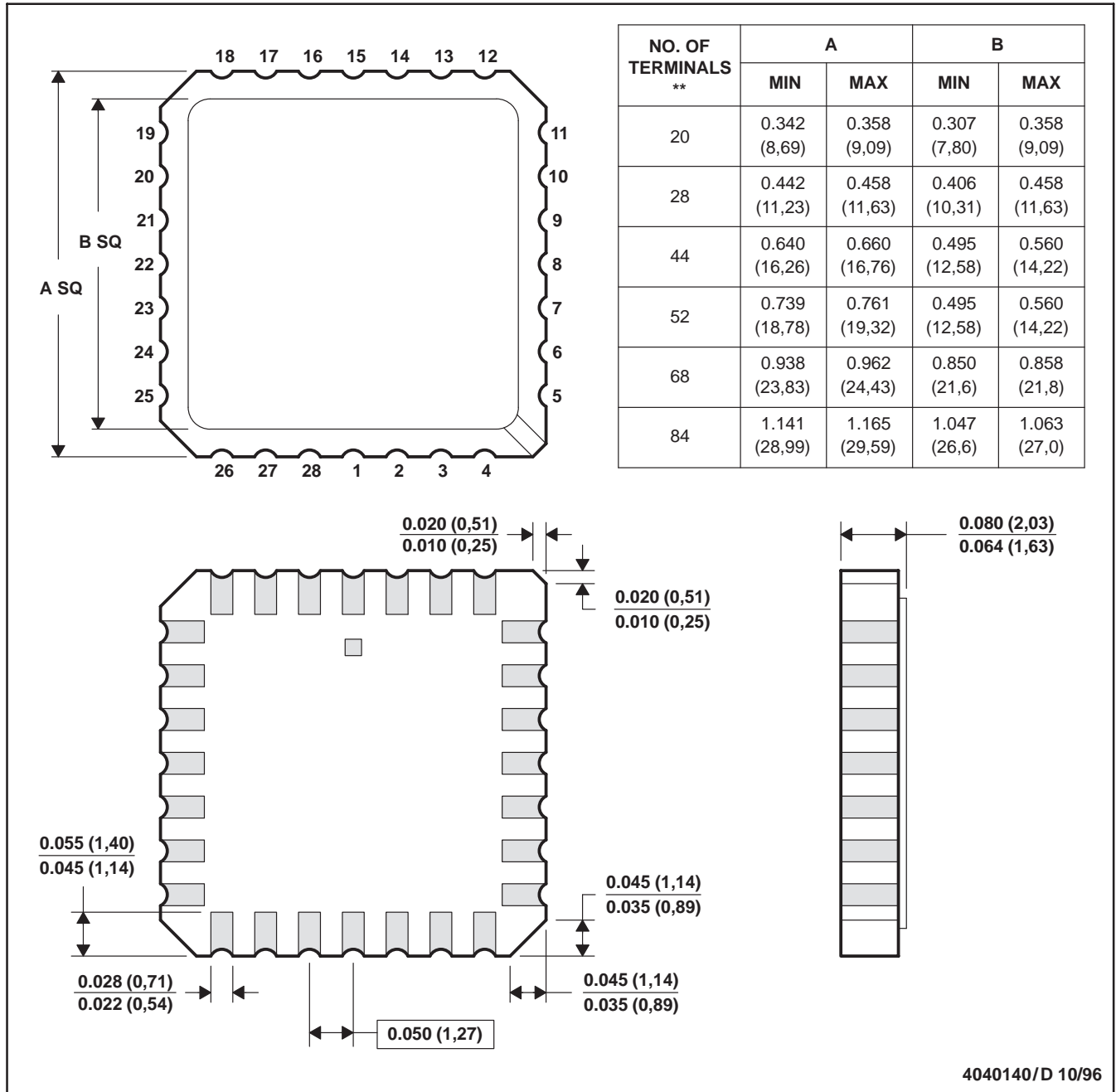


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

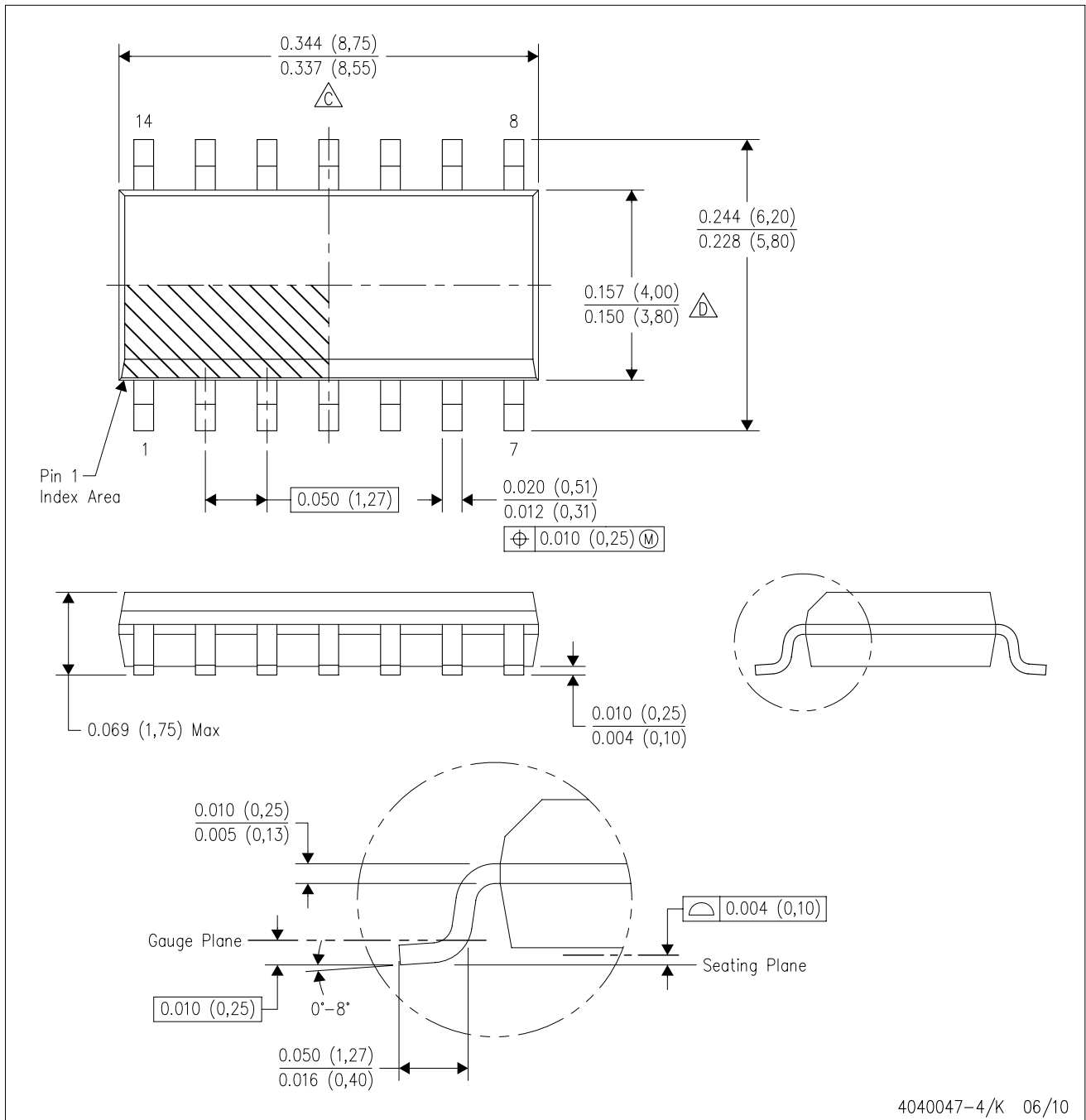


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

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