SN74ALS632B, SN74AS632

32-Bit Parallel Error Detection and Correction Circuits

The 'ALS632B and 'AS632 devices are 32-bit parallel error detection and correction circuits (EDACs). The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in the memory. Single-bit errors in the 32-bit data word are flagged and corrected.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

• ISO-9001
• AS9120 certification
• Qualified Manufacturers List (QML) MIL-PRF-38535
    • Class Q Military
    • Class V Space Level
• Qualified Suppliers List of Distributors (QSLD)
    • Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

- Detects and Corrects Single-Bit Errors

- Detects and Flags Dual-Bit Errors

- Built-In Diagnostic Capability

- Fast Write and Read Cycle Processing Times

- Byte-Write Capability

- Dependable Texas Instruments Quality and Reliability

description

The 'ALS632B and 'AS632 devices are 32-bit parallel error detection and correction circuits (EDACs). The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

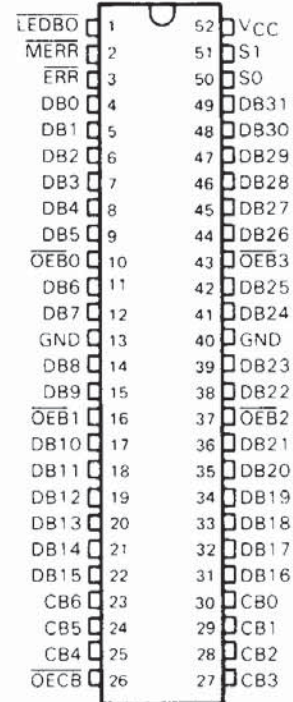Single-bit errors in the 32-bit data word are flagged and corrected.

Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit data word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.
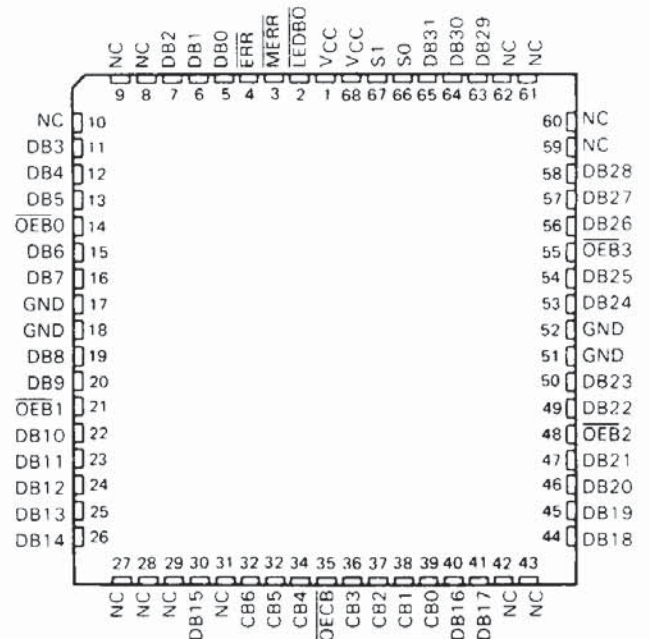
Read-modify-write (byte-control) operations can be performed by using output latch enable, $\overline{LEDBO}$, and the individual $\overline{OEB0}$ thru $\overline{OEB3}$ byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

N OR JD PACKAGE
(TOP VIEW)

Pin	Signal		Signal	Pin
1	$\overline{LEDBO}$		VCC	52
2	$\overline{MERR}$		S1	51
3	ERR		S0	50
4	DB0		DB31	49
5	DB1		DB30	48
6	DB2		DB29	47
7	DB3		DB28	46
8	DB4		DB27	45
9	DB5		DB26	44
10	$\overline{OEB0}$		$\overline{OEB3}$	43
11	DB6		DB25	42
12	DB7		DB24	41
13	GND		GND	40
14	DB8		DB23	39
15	DB9		DB22	38
16	$\overline{OEB1}$		$\overline{OEB2}$	37
17	DB10		DB21	36
18	DB11		DB20	35
19	DB12		DB19	34
20	DB13		DB18	33
21	DB14		DB17	32
22	DB15		DB16	31
23	CB6		CB0	30
24	CB5		CB1	29
25	CB4		CB2	28
26	$\overline{OECB}$		CB3	27

FN PACKAGE
(TOP VIEW)

NC   No internal connection

TEXAS
INSTRUMENTS

SN74ALS632B, SN74AS632
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

logic symbol†
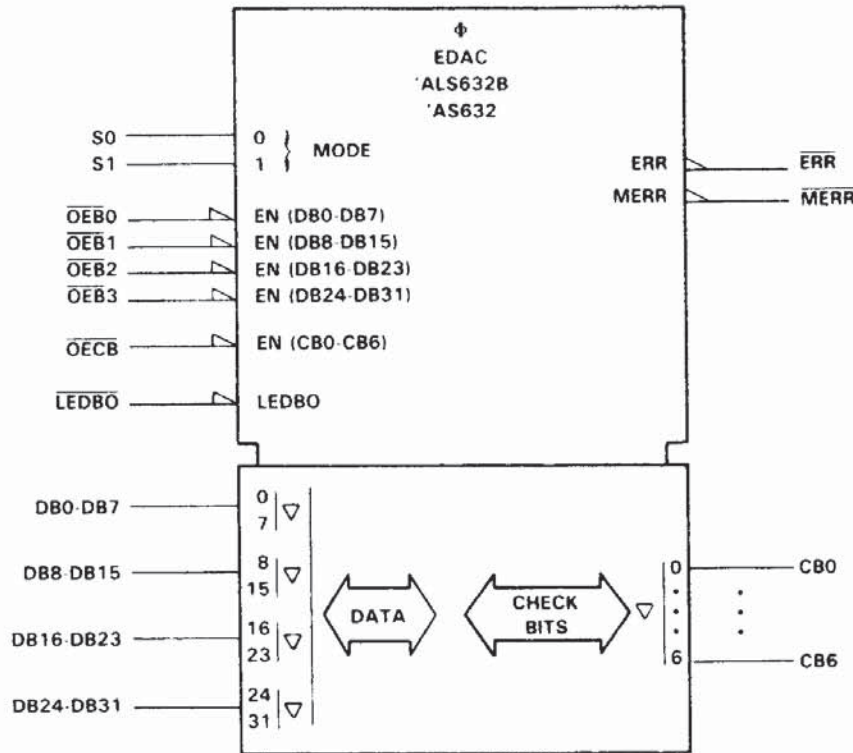
TERMINAL FUNCTIONS

PIN NAME	DESCRIPTION
CB0-CB6	Check Bit data port. This 7-bit I/O port is used to output check bits during write cycles and input memory check bits during read cycles.
DB0-DB31	Data port. This 32-bit I/O port is used to input processor data during memory write cycles and used to output corrected data during memory read cycles.
$\overline{ERR}$	Single-Bit Error Flag. This active-low output signals when a single-bit error has occurred. When more than two errors occur, this output is unpredictable.
GND	Ground
$\overline{LEDBO}$	Output Latch Enable. This input controls the output data latch that stores the corrected data word. When low, data is allowed to flow through the latch. When taken high, data present at the inputs of the output data latch is stored.
$\overline{MERR}$	Multiple-Bit Error Flag. This active-low output signals when a double-bit error has occurred. When more than two errors occur, this output is unpredictable.
NC	No internal connection
$\overline{OEB0}$-$\overline{OEB31}$	Data Output Enable controls. These active-low inputs are used to enable data onto the data bus (DB0-DB31). Each input controls 8-bits for byte control operations. $\overline{OEB0}$ controls DB0-DB7, $\overline{OEB1}$ controls DB8-DB15, $\overline{OEB2}$ controls DB16-DB23, and $\overline{OEB3}$ controls DB24-DB31.
$\overline{OECB}$	Check Bit Output Enable control. This active-low input is used to enable the check bits onto the check bit bus (CB0-CB6).
S0,S1	Mode Select controls. These control inputs select the mode of the EDAC. See function tables for details.
V_{CC}	Supply voltage

for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.

Designing and Manufacturing
Surface Mount Assemblies

T-90-20

Elizabeth Gunther, Charles Hutchins, and Paul Peterson

The competitive nature of the semiconductor industry has driven vendors to minimize the size of electronic components, so that more functions can be achieved in a given volume. In addition, improved electrical performance, decreased mass, and the potential for lower system cost are all by-products of compacted packaging and circuitry which hold interest to component manufacturers and users alike.

Surface Mount Technology (SMT) offers an excellent method of reducing component size. A typical memory array can be reduced to 50 percent of its original PWB size with single-sided mounting, and 25 to 30 percent with double-sided mounting. Logic designs cannot achieve the same dramatic reduction, but decreases up to 40 to 60 percent can be achieved for single-sided and double-sided assemblies respectively.

The key design and manufacturing process issues must be understood in order to fully reap the benefits of Surface Mount Technology. This article gives a general overview of the key aspects of design, process, and manufacturing of surface mounted assemblies, and offers surface mount as an opportunity to lower a system's cost without sacrificing reliability.

Components

Most surface mount components are at least one-third the size of the comparable through-hole mounted device (Figure 1). The 68-pin chip carrier is approximately one square inch, while the 64-pin DIP is approximately three square inches. The 20-pin chip carrier is slightly larger than 0.1 square inch, while the 20-pin DIP is 0.3 square inch. Similarly, other IC packages are reduced to approximately one-third the size of comparable lead count packages. The passive components

occupy approximately one-tenth the board area, and this is why they have been used in most small consumer products built in the last couple of years.

There were many references in the recent past to problems with component availability, cost, and standardization. This area of SMT has probably received more attention than any other. Several recent magazine articles now state that significantly more components (particularly actives) are now available and that cost parity has been achieved on most of them. The effort by various industry committees on standardization has also been effective.

Thus, although more needs to be accomplished in these areas, a designer can begin a project with confidence that there will be no insurmountable barriers in this area. There are several consultants and subcontract assembly companies to assist in this effort. It is strongly recommended that all new designs utilize some form of SMT, particularly when space is an important consideration.

Process

The process to manufacture a surface mount assembly (SMA) is very simple. It consists of four basic steps, as shown in Figure 2. First, the solder paste is screened on the PWB. Then the component is placed on the board, with due care to get it positioned correctly. Typical geometries require placement accuracy of less than plus/minus 4 mils. Next the solder is reflowed with either a vapor phase or infrared system. Finally, the assembly is cleaned and is now ready for test. This process, although simple in concept, relies on board and component planarity and solderability. These are easily achievable with the chip carriers and memory modules we will discuss later.

Texas Instruments has installed a Surface Mount Technology Center at its plant in Houston, Texas. At this center, we have a complete and flexible engineering line to assist our customers in converting to Surface Mount Technology.

The engineering line is equipped with a screen printer, pick and place system, vapor phase reflow, and clean-up station that will easily handle PWBs up to 9" × 10". Larger boards up to 14" × 16" can be processed with some additional care. TI uses this engineering line to produce its prototype and demo boards. It is also available to any of TI's customers, free of charge, for use in building test or prototype boards.

The effectiveness of the assembly process can be characterized by the number of unacceptable solder joints formed during the process. Unacceptable joints are defined by their electrical and mechanical (strength and reliability) characteristics. The major problem is open solder joints, followed by bridging and misregistration.
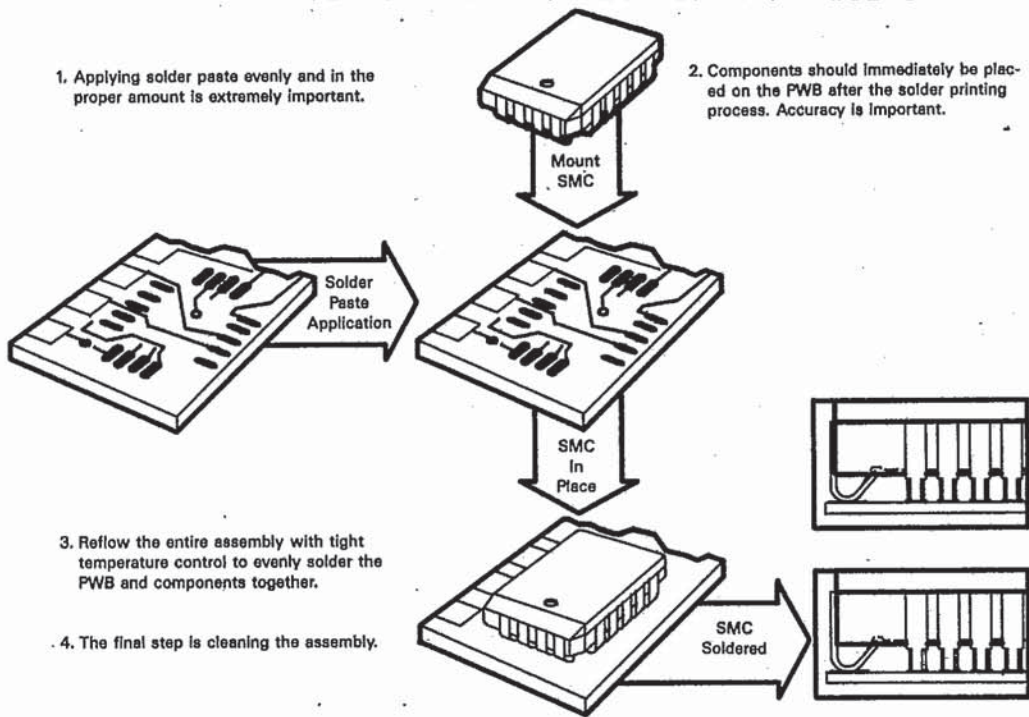

Figure 1. Component Site Reduction

9-3

1. Applying solder paste evenly and in the proper amount is extremely important.

2. Components should immediately be placed on the PWB after the solder printing process. Accuracy is important.

Mount SMC

Solder Paste Application

SMC In Place

3. Reflow the entire assembly with tight temperature control to evenly solder the PWB and components together.

4. The final step is cleaning the assembly.

SMC Soldered

Figure 2. Basic Process Steps

Open circuits are detected at electrical test and are the first defects detected after soldering. At Texas Instruments, 10 PPM or less is the desirable defect level. Several factors that contribute to open solder joints were identified during production start-up. Lead tip planarity of the J-leaded plastic chip carriers is the most important factor in obtaining acceptable process yields. Lead position, lead finish, solder paste composition, and PWB solderability affect process yield as well.

Experiments in which lead tip planarity was confined to specific limits between 1 to 7 mils indicate that a 2 mil planarity requirement produces acceptable results with the process currently in use. Little gain in yield was noted at a 1 mil planarity requirement.

Another interesting result showed that silver in the process, either as a lead finish or in the solder paste, improves yields significantly. One explanation may have to do with the dynamics of the solder during the reflow process as they are affected by the different surface forces acting in the silver and non-silver process.

Design

The design of the PWB, in addition to providing the component interconnections, will provide the proper amount and correct placement of solder paste for a strong fillet formation. The wave soldering process, by comparison, provides a semi-infinite amount of solder, whereas the SMT process will provide only a predetermined amount. Thus, the component connection pad must be correctly placed and be of the proper size.

Further, consideration must be given for inspection, testing, and rework. The density achievable can lead to severe problems at these points if understanding and due care are not exercised in the design. The project team should include members from manufacturing, testing, QA, and purchasing, in addition to the design engineers, from the start. The design and processing of test boards is strongly recommended to provide experience and direction for the major project.

A very practical set of design guidelines is given in Figure 3. These have been used on a number of SMT designs and have given good results. With proper manufacturing techniques as described later, a high yield can be achieved. Component spacings should be approximately equal to the height of the tallest component. This allows an angle of 45 degrees for visual inspection of test probes.

Figure 4 shows the standard footprint for all Small Outline (SO) packages. The larger and more important fillet of an SO package is on the inside of the gull-wing lead. The solder pad, or land, should therefore be designed to extend slightly under the body of the package in order to optimize this fillet. From Table 1 we can see all packages have 50 mil centers with 25 mil spacings between lands. This allows the designer enough space to put traces between pads, and also reduces the occurrence of solder bridging of adjacent lands. Table 1 also summarizes the suggested land lengths and placement, depending on the terminal count of the SO. While not an absolute solution, these land sizes offer a conservative design solution that will meet most vendors' specifications and provide a mechanically and electrically sound solder joint.

- Geometries
  - Trace Width/Space   8/8 MIL Min., 10/10 MIL Typ.
  - IC Lead Solder Pad Size 25 ± 5 MIL × 70 ± 10 MIL
  - Via Hole Size   20 MIL DIA
  - Via Pad Size   40 MIL DIA
  - Cap/Resistor Pad Size   W = MAX Dimensions of Component
                             L = 20 MIL Beyond Metallization
                                 10 MIL Inside Metallization
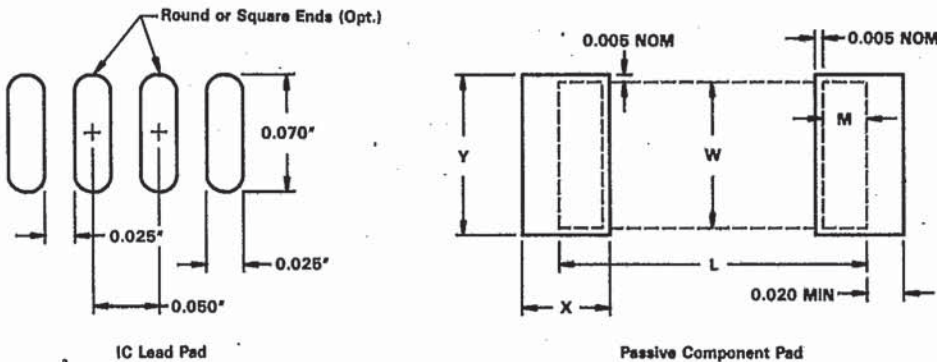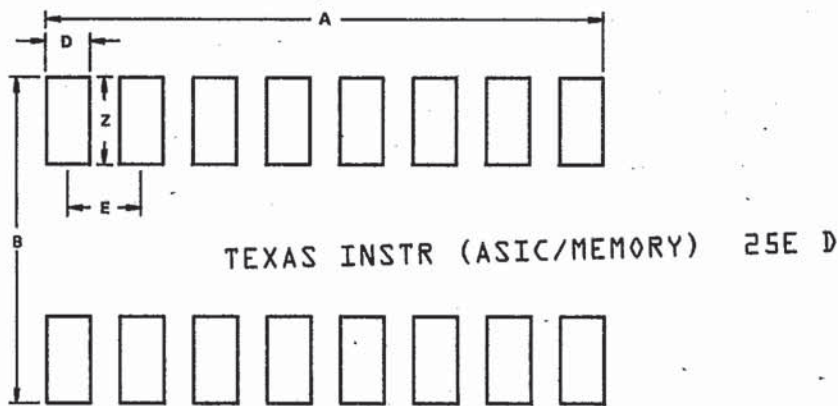 - Solder Mask   5 MIL Larger than IC/Component Pad

IC Lead Pad   Passive Component Pad

Figure 3. PWB Design Guidelines

TEXAS INSTR (ASIC/MEMORY) 25E D

Figure 4. Standard SOIC Footprint

Applications Information

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Table 1. SOIC Footprint Dimensions

No. of Terminals	A	B	Z	D	E
8	.175	.250	.050	.025	.050
14	.325	.250	.050	.025	.050
16	.375	.250	.050	.025	.050
20	.475	.430	.070	.025	.050
24	.575	.430	.070	.025	.050

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Test	4164A PLCC	4164 DIP	Units
Life Test, 125°C	42	64	Fits* —60% UCL
85°C/85% RH	0.17	0.37	%/1000 Hours
Autoclave	0.17	0.96	%/240 Hours
T/C—65/150	0.52	1.44	%/1000 Cycles
T/C 0/125	0.0	0.0	%/2000 Cycles
*Derated to 55°C Assuming 0.5EV Activation Energy			

Figure 5. Failure Rate Comparison 4164A PLCC VS DIP

Manufacturing

The SMT manufacturing area must have the following basic equipment:

- Solder Paste Printer
- Component Pick and Place Machine
- Solder Paste Reflow Machine
- Clean-up System
- Inspection/Process Control Aids
- Electrical Test

The criteria for choosing the above is determined mainly by the size(s) and quantity of PWBs per month, the gross number of components per PWB, and the number of different components per PWB.

The size of the largest PWB is an important criterion in the choice of all of the major items. The printer, pick and place, reflow, and clean-up must all be able to handle it with no difficulty or process nonuniformity. The number and size of the various PWBs that may be produced will secondarily be considered for ease of set up and changeover in the printer and pick and place. The pick and place machine(s) will

probably be the most expensive item in the list above and therefore, should get the most attention.

The gross number of components and PWBs will provide data for choosing the pick and place. Component per hour placement speed should be checked in actual operation, as the interrelationship may affect ultimate speed. The number of different components per board will determine how many feeders and what types of feeders will be required. This is a very key issue, as well as the accuracy of placement.

Reflow

The solder reflow is easily achieved with any of the commercially available equipment. Subtle differences between vapor phase, either batch or in-line, and infrared are overshadowed by the choice of solder paste and the solderability/planarity issue. A batch vapor phase is extremely flexible for different sizes of boards with different component counts. The in-line vapor phase is a good choice for a more automated processing line with standard or similar sized boards. The infrared has the advantage of being less expensive to operate, but requires more alteration to set up the time-temperature profile for a different size PWB. This would be a minimal problem on a manufacturing line building high volumes of the same board.

Clean-up

The most popular flux for SMT is the mildly activated rosin flux (RMA). This was developed in the days of vacuum tube assembly when clean-up was next to impossible. It is noncorrosive but provides sufficient fluxing action for good quality components and PWBs. Thus it is the preferred choice for SMAs with small spacings under most passives and SOICs, where complete cleaning is difficult. A mild solvent, such as Freon TMS, is generally sufficient to achieve a good visual cleanup, and there are several systems available that provide hot vapor, spray, or ultrasonic de-fluxing.

Reliability

With the smaller surface mount packages, there is some concern about component reliability. Texas Instruments addressed the overall DRAM reliability issue several years ago. Through an extensive task force effort, the major problems of the life test, humidity performance, and temperature cycle were identified. The best solutions to these problems required several changes in the design and process of the silicon chip. In doing so, the reliability of the DRAM chip became independent of the package used. Thus, the 64K DRAM in the plastic chip carrier package performs equivalently to the same chip in a DIP as shown in Figure 5. Similar data is available on most semiconductor ICs.

An additional reliability concern originates in the surface mount solder reflow process, which submits components to higher reflow temperatures more suddenly than the wave-soldering methods of DIP components, with oftentimes repeated reflow cycles for rework and repair.

The best method for resolving this issue involves comparing the temperature-time differential of the vapor phase or infrared solder reflow process to the standard temperature

cycling reliability tests to which surface mount components are routinely submitted. Figures 6 and 7 show temperature profiles of the vapor phase and infrared solder reflow processes. In the vapor phase process, the maximum temperature change with time is:

$$\frac{215°C - 25°C}{45 \text{ sec}} = \frac{190°C}{45 \text{ sec}}$$

equaling approximately 4°C/sec. The infrared solder reflow method submits the ICs to a similar, yet less severe temperature over time change of 3°C/second. Comparing these temperature profile ramp-ups to that which a surface mount component undergoes in a temperature cycling reliability test proves that there should be no concern over damage to the component during reflow. In the temp cycling test, the surface mount components were submitted to 1000 cycles of sudden cycling from 150°C to −65°C within three seconds. This represents a temperature-time differential of:

$$\frac{150°C-(-65°C)}{3} = \frac{215°C}{3 \text{ sec}} = \frac{70°C}{\text{sec}}$$

with less than 0.5 percent failures.
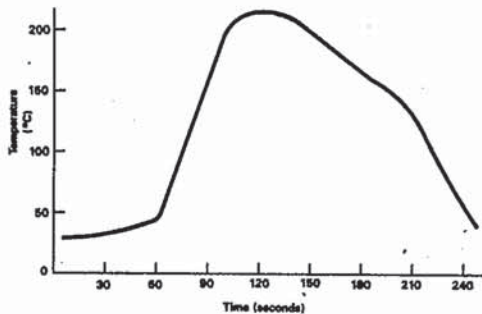
Figure 6. Typical Temperature Profile
for In-Line Vapor Phase Reflow

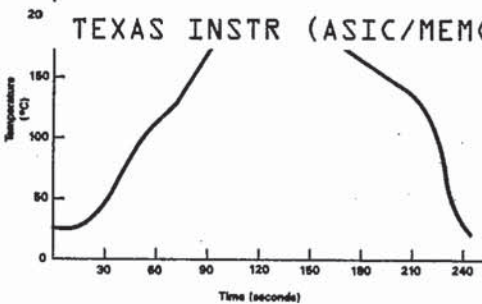TEXAS INSTR (ASIC/MEMORY) 25E D

Figure 7. Typical IR Reflow System Profile

Since the surface mounted components were able to withstand a 70°C/second temperature change of 1000 cycles, they should be able to withstand the less severe conditions of a 4°C/second damage during reflow without reliability degradation.

Another concern in the solder reflow processing of surface mount components is the dwell time in reflow temperatures of 215°C or above. The dwell time for a small PWB populated with surface mount devices is about 20 seconds. For a larger board of about 10″×12″ up to 50 seconds is needed for reflow. A generalized component degradation curve, relating accumulated time and temperature, can be assumed to exist. The shape of the curve for this discussion is assumed to be a decaying parabolic for simplicity and conservatism. There are two generally known points of this curve. The flame retardant mold compound (FRMC) of a plastic package starts to break down at 300°C in two to three seconds. Also, the molding and curing of a surface mount device is performed over several hours at 175°C. These two points are shown on the generalized curve shown in Figure 8, with the "safe" region being the area under the curve. Two points that fall within this region are the industry standard practice of solder dipping leads of several types of ICs, and of the soldering plastic devices on the bottom with Type III surface mount assembly, each submerges the component for three to four seconds in a solder wave.
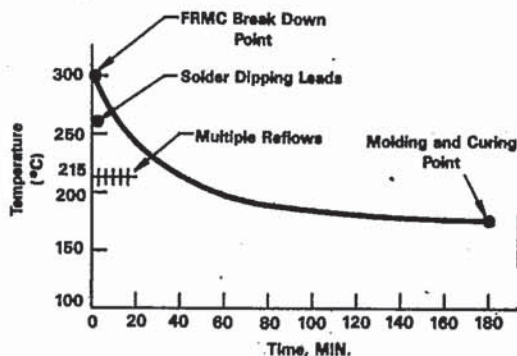

Figure 8. General Plastic Degradation Curve

Summary

Surface mount assembly techniques provide a significant advantage in cost, volume, and reliability over the current "thru-hole" technology. These are well documented, and the manufacturing equipment and related products are becoming readily available to support new production lines. Also, as experience grows, improved products and ideas are developed from the cooperative efforts of vendors and users in standardization organizations and in problem-solving sessions. The broad selection of package types and product technologies available now are sufficient to begin conversion of existing electronic system products for size reduction or feature enhancement. Definitely, new products should be designed with surface mount technology.

Applications Information

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