SN74ALS992, SN74ALS993

9-Bit D-Type Transparent Read-Back Latches with 3-State Outputs

These 9-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus. In addition, they provide a 3-state buffer-type output and are easily implemented in parity applications.

The nine latches of the ‘ALS992 and ‘ALS993 are transparent D-type. While the enable (C) is high, the Q outputs of the ‘ALS992 will follow the data (D) inputs. For the ‘ALS993, the $\overline{Q}$ outputs will provide the complement of what is applied to its data (D) inputs. On both devices, the Q or $\overline{Q}$ outputs will be in the 3-state condition when output enable $\overline{OE}Q$ is high.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer’s datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. ‘Typical’ values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SN74ALS992, SN74ALS993
9-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

D2836, APRIL 1984 · REVISED JANUARY 1986

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- Choice of True or Inverting Logic
  - 'ALS992 . . . True Outputs
  - 'ALS993 . . . Inverting Outputs
- Designed with 9 Bits for Parity Applications
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 9-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus. In addition, they provide a 3-state buffer-type output and are easily implemented in parity applications.

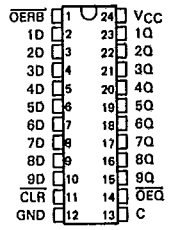
The nine latches of the 'ALS992 and 'ALS993 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS992 will follow the data (D) inputs. For the 'ALS993, the $\overline{Q}$ outputs will provide the complement of what is applied to its data (D) inputs. On both devices, the Q or $\overline{Q}$ outputs will be in the 3-state condition when output enable $\overline{OEQ}$ is high.

Read-back is provided through the read-back control input ($\overline{OERB}$). When the control is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, precautions should be taken not to create a bus-conflict situation.

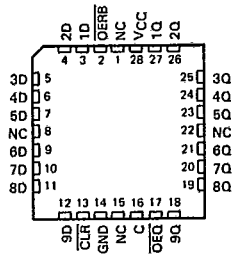
The SN74ALS992 and SN74ALS993 are characterized for operation from 0°C to 70°C.

SN74ALS992 . . . DW OR NT PACKAGE
(TOP VIEW)

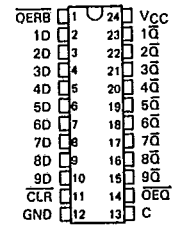
T-46-07-12



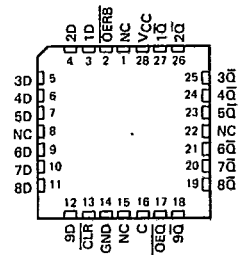
SN74ALS992 . . . FN PACKAGE
(TOP VIEW)



SN74ALS993 . . . DW OR NT PACKAGE
(TOP VIEW)



SN74ALS993 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

2

ALS and AS Circuits

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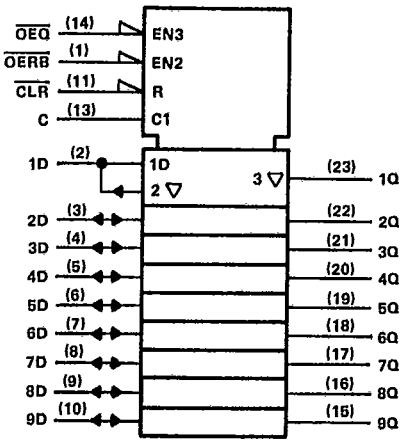
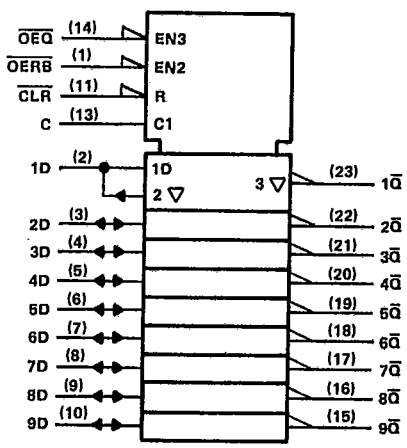
SN74ALS992, SN74ALS993
9-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

logic symbols†

'ALS992



'ALS993



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for DW and NT packages.

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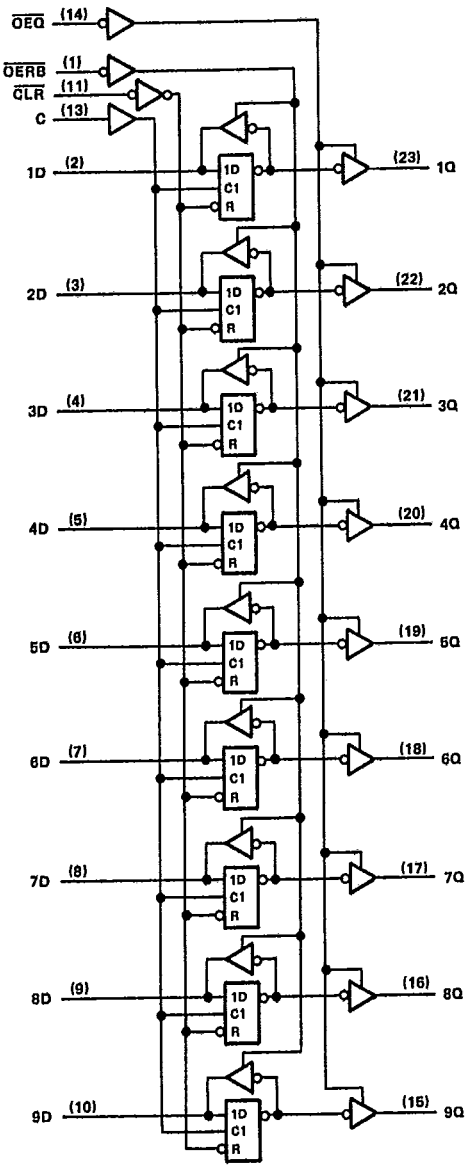
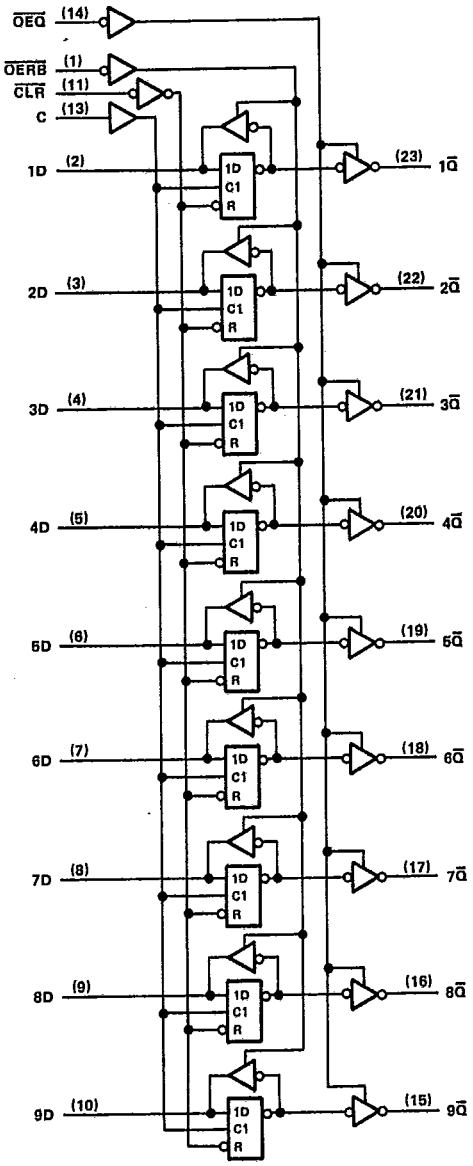
logic diagrams (positive logic)

'ALS992



'ALS993



Pin numbers are for DW and NT packages.

SN74ALS992, SN74ALS993
9-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

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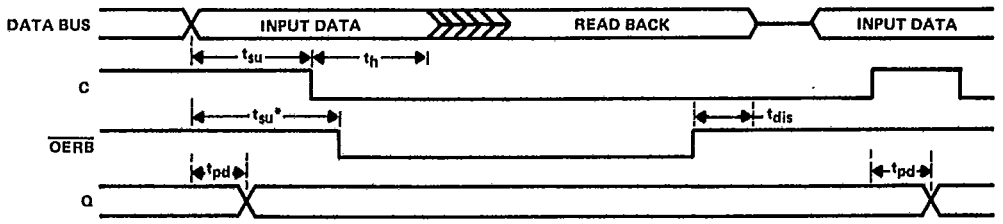
timing diagram



$\overline{CLR}$ = H, $\overline{OEQ}$ = L

*This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, ($\overline{OERB}$, $\overline{OE}$, $\overline{CLR}$, and C inputs) . . . . . 7 V
Voltage applied to D inputs and to disabled 3-state outputs . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q or $\overline{Q}$			−2.6	mA
		D			−0.4	
I_{OL}	Low-level output current	Q or $\overline{Q}$			24	mA
		D			8	
t_w	Pulse duration	Enable C high	10			ns
		$\overline{CLR}$ low	10			
t_{su}	Setup time	Data before C↓	10			ns
		Data before $\overline{OERB}$↓	10			
t_h	Hold time	Data after C↓	5			ns
T_A	Operating free-air temperature		0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	All outputs Q or $\overline{Q}$	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	D	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_{OZH}	Q or $\overline{Q}$	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	
I_I	D inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
	All other	V_{CC} = 5.5 V,	V_I = 7 V			0.1	
I_{IH}	D inputs‡	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
	All other					20	
I_{IL}	D inputs‡	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	All other					−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	'ALS992	V_{CC} = 5.5 V, $\overline{OERB}$ high	Q outputs high		30	50	mA
			Q outputs low		50	80	
			Q outputs disabled		35	55	
	'ALS993	V_{CC} = 5.5 V, $\overline{OERB}$ high	$\overline{Q}$ outputs high		30	50	mA
			$\overline{Q}$ outputs low		52	82	
			$\overline{Q}$outputs disabled		40	60	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output current, I_{OS}.

SN74ALS992, SN74ALS993
9-BIT D-TYPE TRANSPARENT READ-BACK LATCHES
WITH 3-STATE OUTPUTS

'ALS992 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Q		7	10	3	14	ns
t_{PHL}				9	13	4	16	
t_{PLH}	C	Q		12	15	6	20	ns
t_{PHL}				15	19	8	25	
t_{PHL}	$\overline{CLR}$	Q		12	16	6	20	ns
t_{PHL}		D		15	22	8	26	
t_{en}	$\overline{OERB}$	D		11	17	4	21	ns
t_{dis}				6	11	2	14	
t_{en}	$\overline{OEQ}$	Q		11	16	4	18	ns
t_{dis}				6	10	1	14	

'ALS993 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$		11	14	6	20	ns
t_{PHL}				8	11	4	15	
t_{PLH}	C	$\overline{Q}$		16	20	9	28	ns
t_{PHL}				13	16	7	22	
t_{PLH}	$\overline{CLR}$	Q		10	13	5	17	ns
t_{PLH}		D		15	22	8	26	
t_{en}	$\overline{OERB}$	D		11	17	4	21	ns
t_{dis}				6	11	2	14	
t_{en}	$\overline{OEQ}$	$\overline{Q}$		11	16	4	20	ns
t_{dis}				6	10	1	12	

t_{en} = t_{PZH} or t_{PZL}
t_{dis} = t_{PHZ} or t_{PLZ}

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PARAMETER MEASUREMENT INFORMATION

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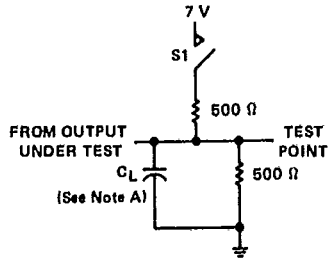
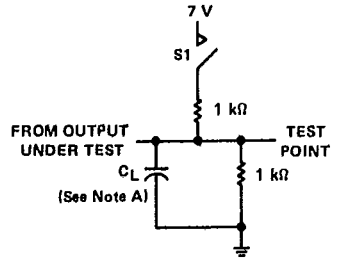
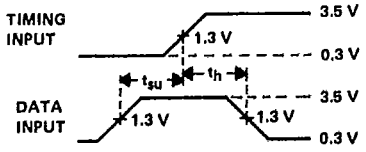


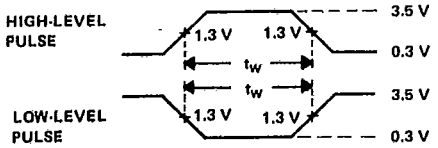
LOAD CIRCUIT FOR
Q OR $\overline{Q}$ OUTPUTS



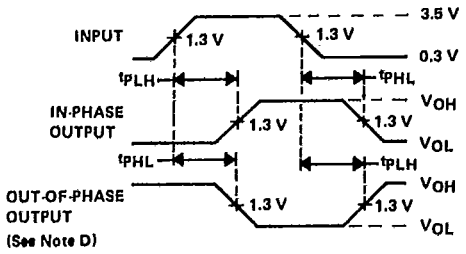
LOAD CIRCUIT FOR D OUTPUTS



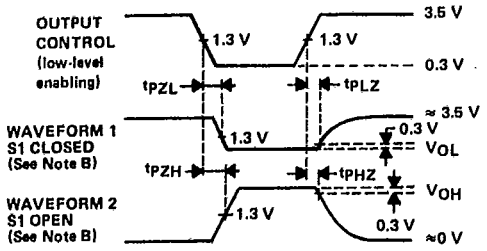
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE WIDTHS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

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