

Design Notes

- 1) EP3C25 device symbol has been pin swapped. DO NOT UPDATE EP3C25 SCHEMATIC SYMBOL FROM LIBRARY!
- 2) CMCS002M is configured as a Cardstac master card.
- 3) Carstac header pins G8-G15 (8 pins) are shared with SRAM device for use as data bus pins. Set SRAM device CE- pin high to disable the SRAM device (pin L4 of FPGA device tied to VCC inside FPGA design).

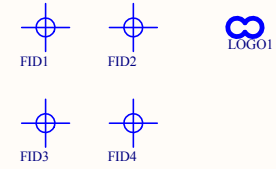


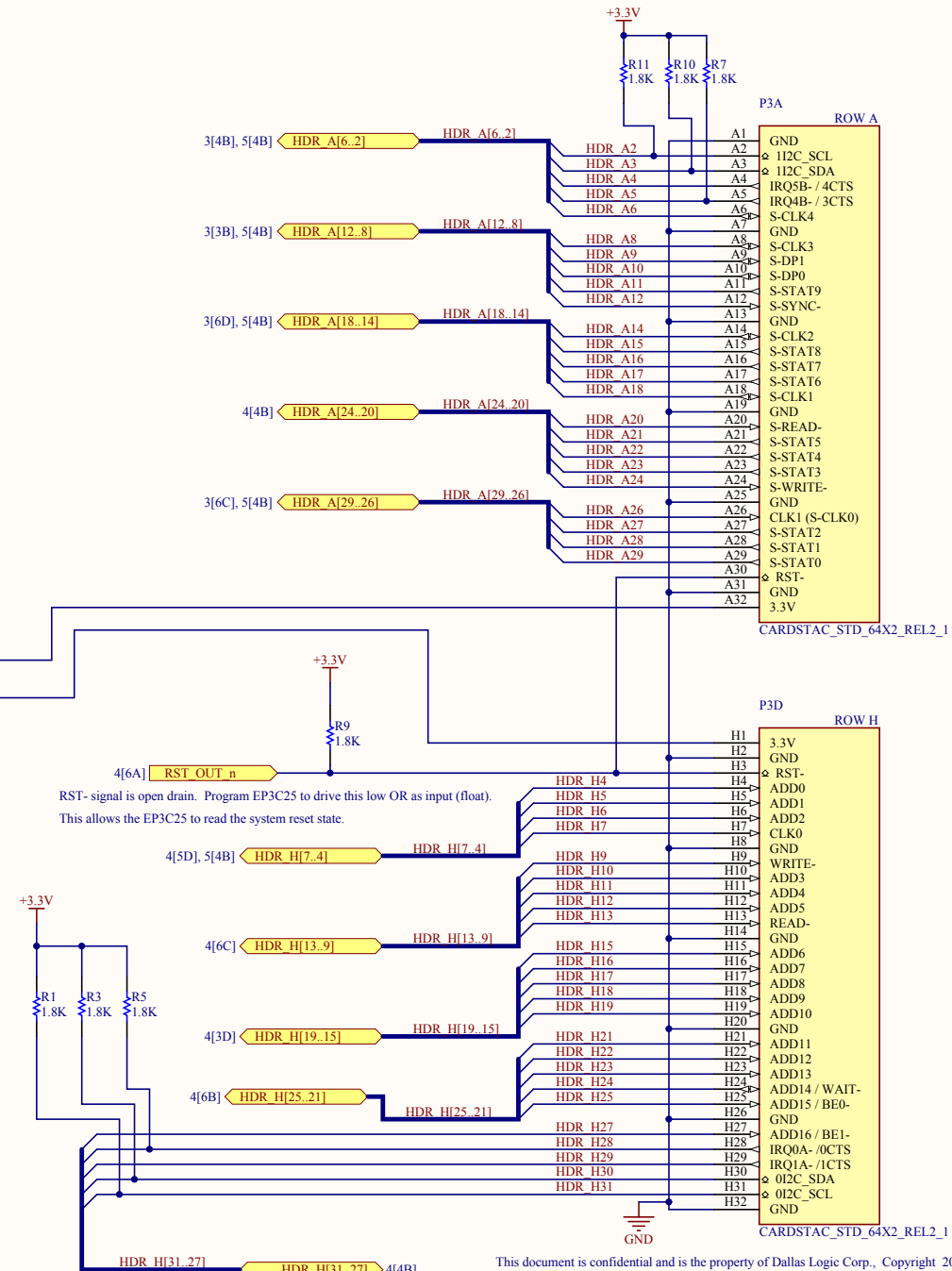
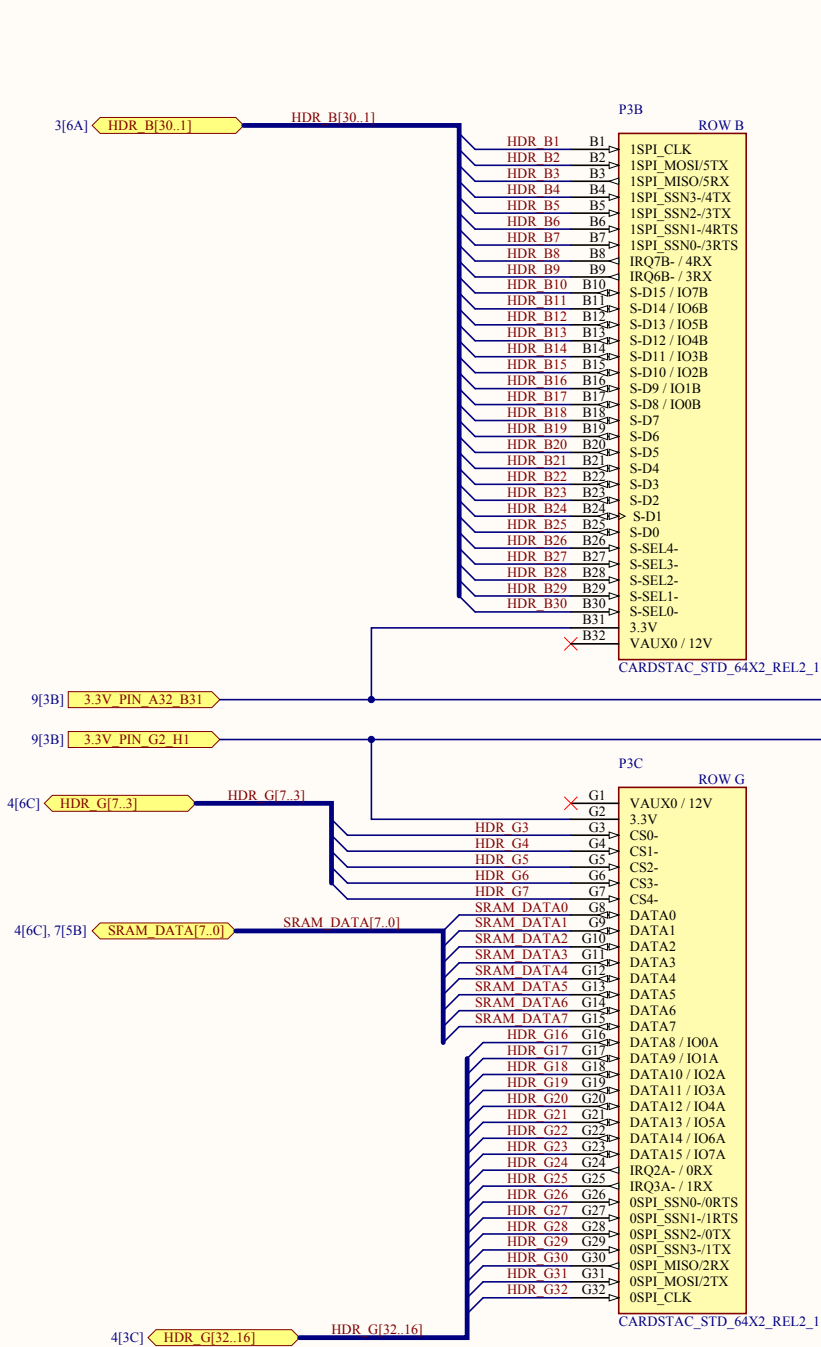
TABLE OF CONTENTS:

- 1- Cover Sheet
- 2- Header Connectors (Cardstac)
- 3- FPGA page 1 (EP3C25)
- 4- FPGA page 2 (EP3C25)
- 5- FPGA page 3 (EP3C25)
- 6- FPGA page 4 (EP3C25)
- 7- SRAM and Oscillator
- 8- Miscellaneous devices, USB Interface, LED
- 9- Power Supply Input

REVISION TABLE			
05-15-09	A	ET	Initial release of the schematic.

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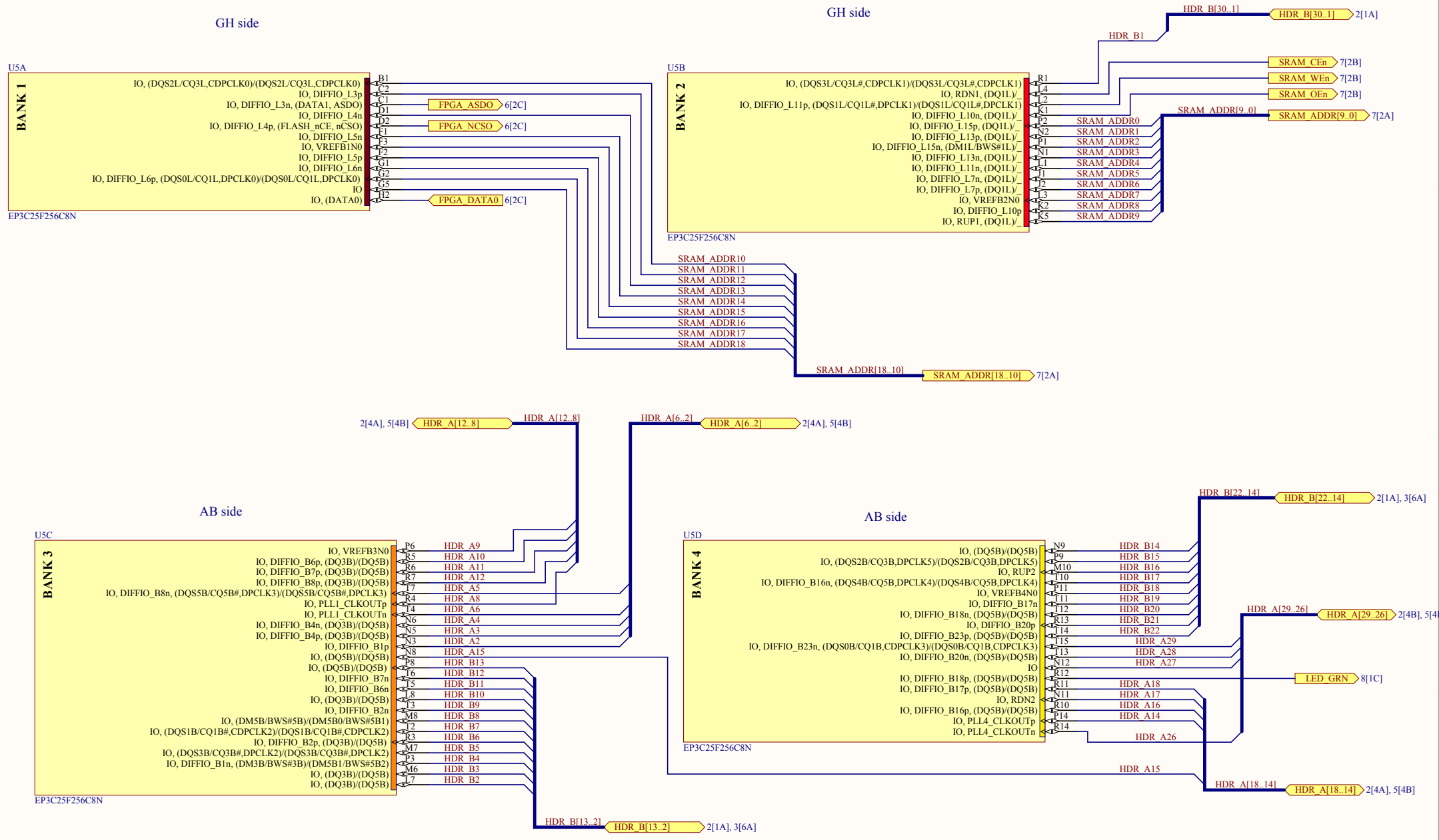
Title Cardstac Cntrl., Std. Size, Altera EP3C25		Dallas Logic Corporation 2300 McDermott Rd. #200-305 Plano TX 75025 USA		
Size: B	Number: CMCS002M	Revision: A	Date: 5/15/2009 Time: 11:41:34 PM Sheet 1 of 9	
File: C:\dallas_logic\altium_dlc\Projects\CMCS002M_REVA\1_TOC.SchDoc				



4[6A] RST_OUT n
 RST- signal is open drain. Program EP3C25 to drive this low OR as input (float).
 This allows the EP3C25 to read the system reset state.

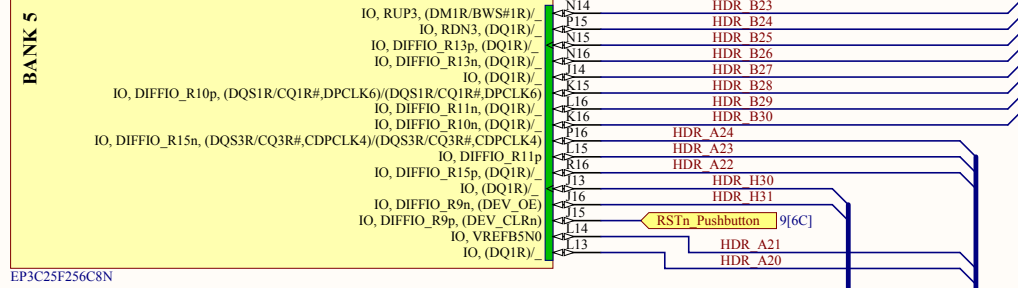
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USE

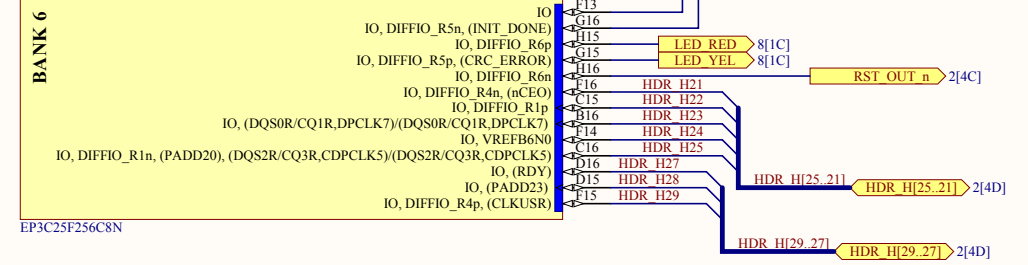
AB side



HDR B[30..23] HDR B[30..23] 2[1A], 3[6A]

GH side

USF



HDR A[24..20] HDR A[24..20] 2[4B]

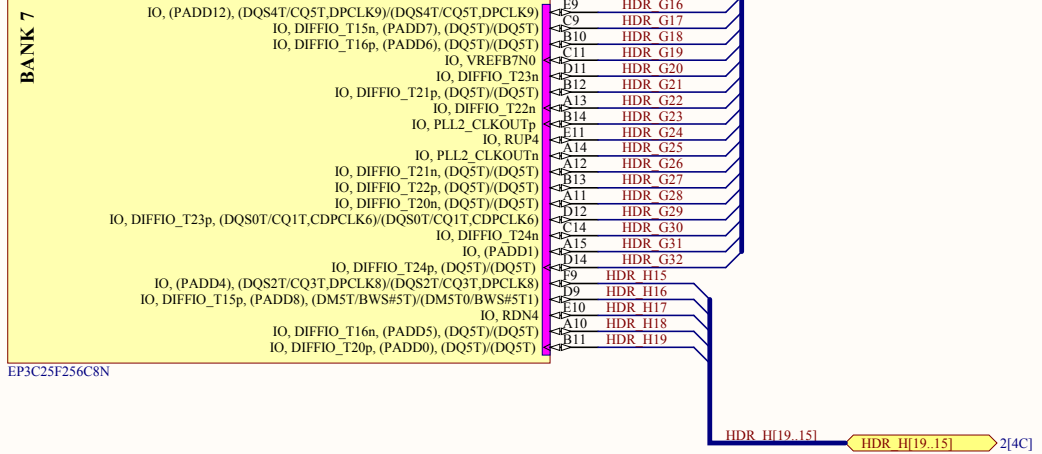
HDR H[31..30] HDR H[31..30] 2[4D]

HDR H[25..21] HDR H[25..21] 2[4D]

HDR H[29..27] HDR H[29..27] 2[4D]

GH side

USG

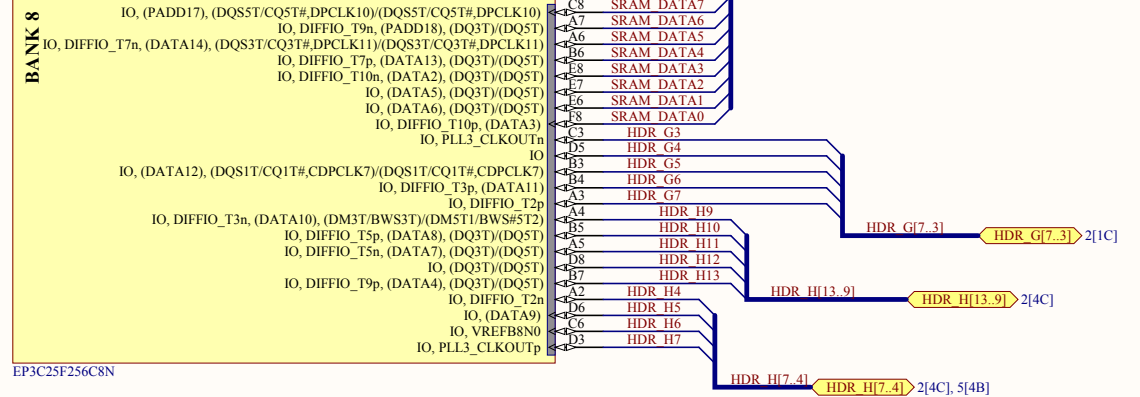


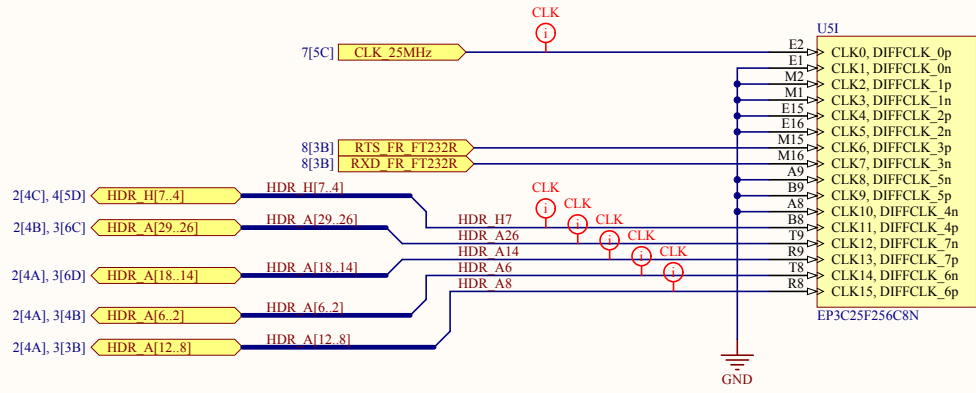
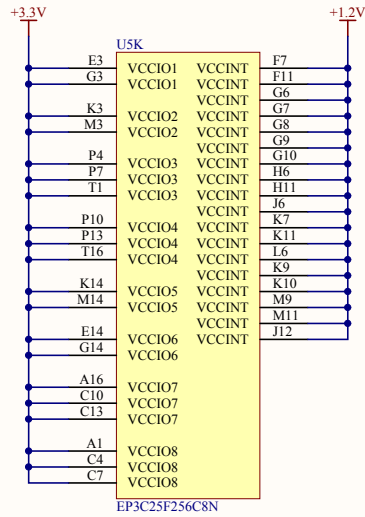
HDR G[32..16] HDR G[32..16] 2[1D]

HDR H[19..15] HDR H[19..15] 2[4C]

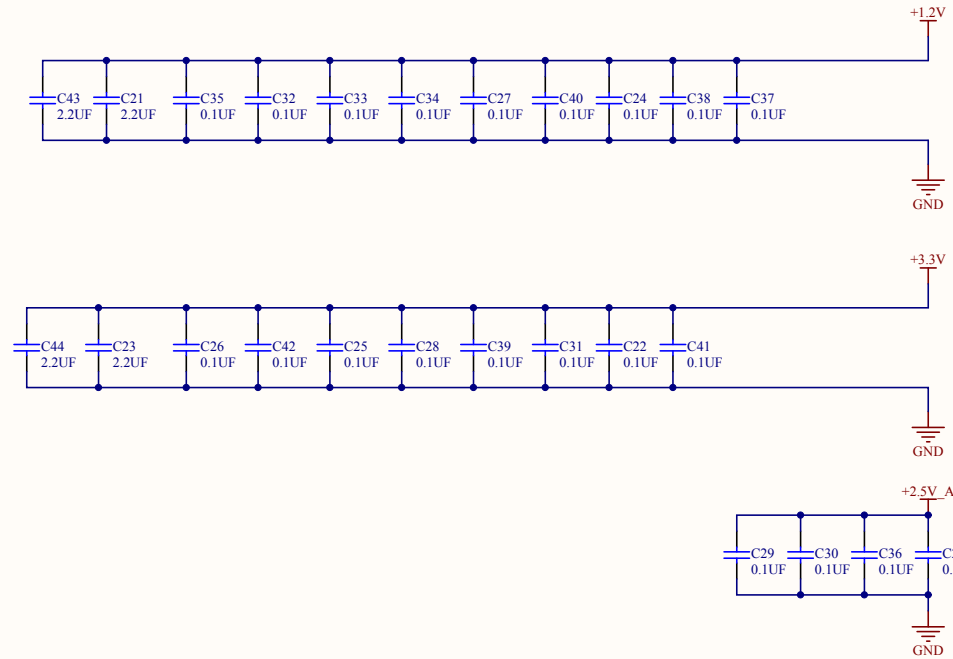
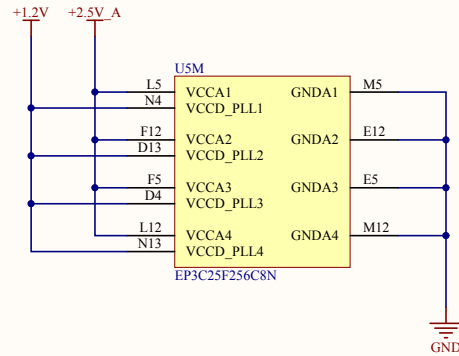
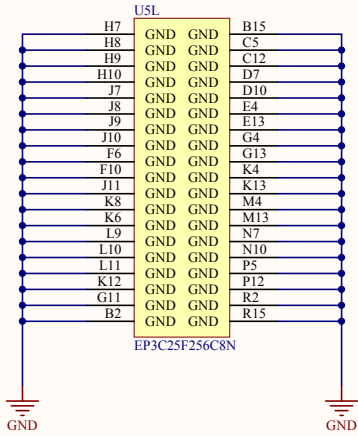
GH side

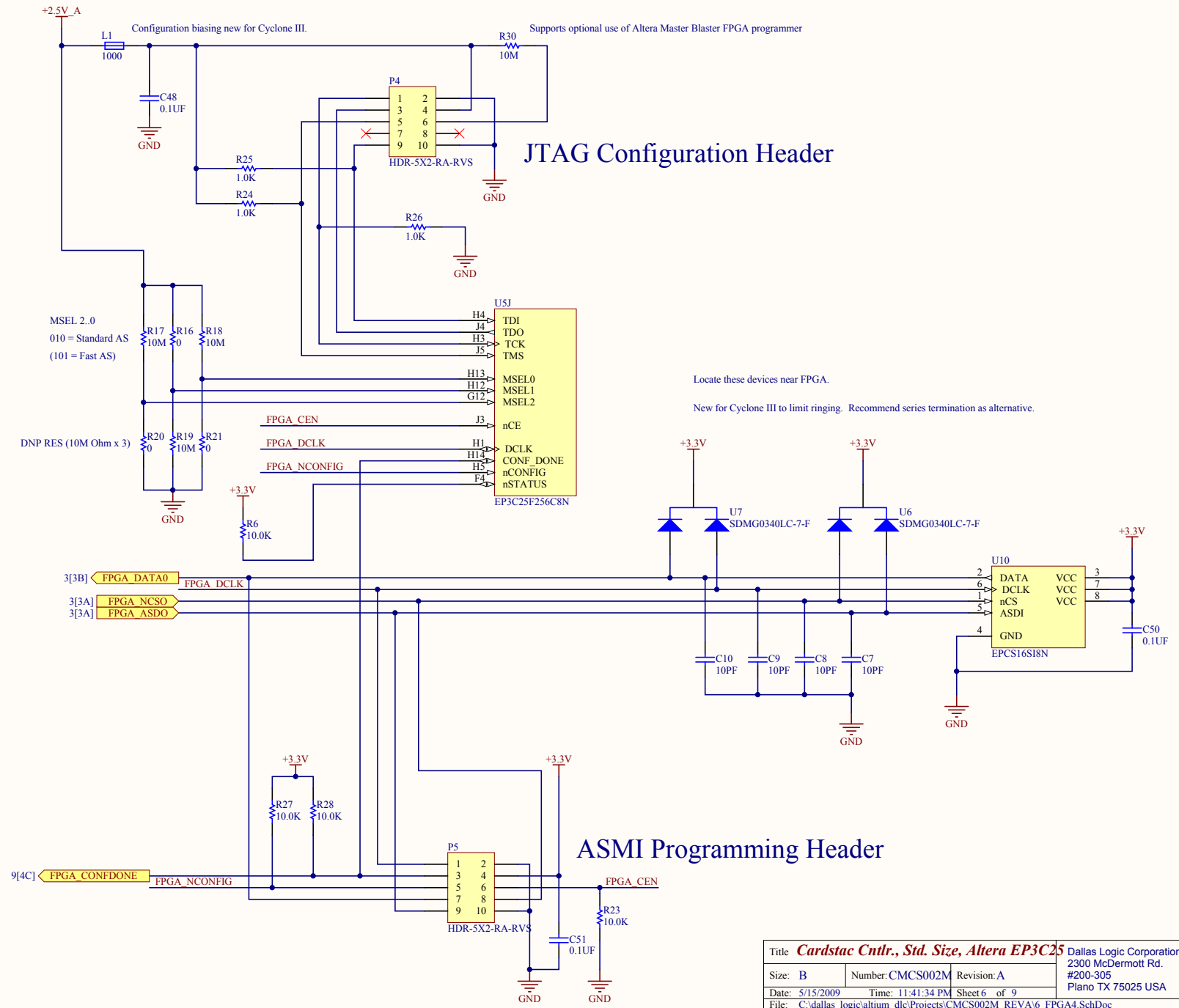
USH



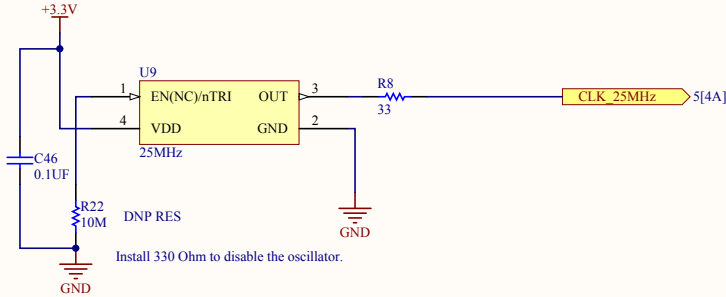
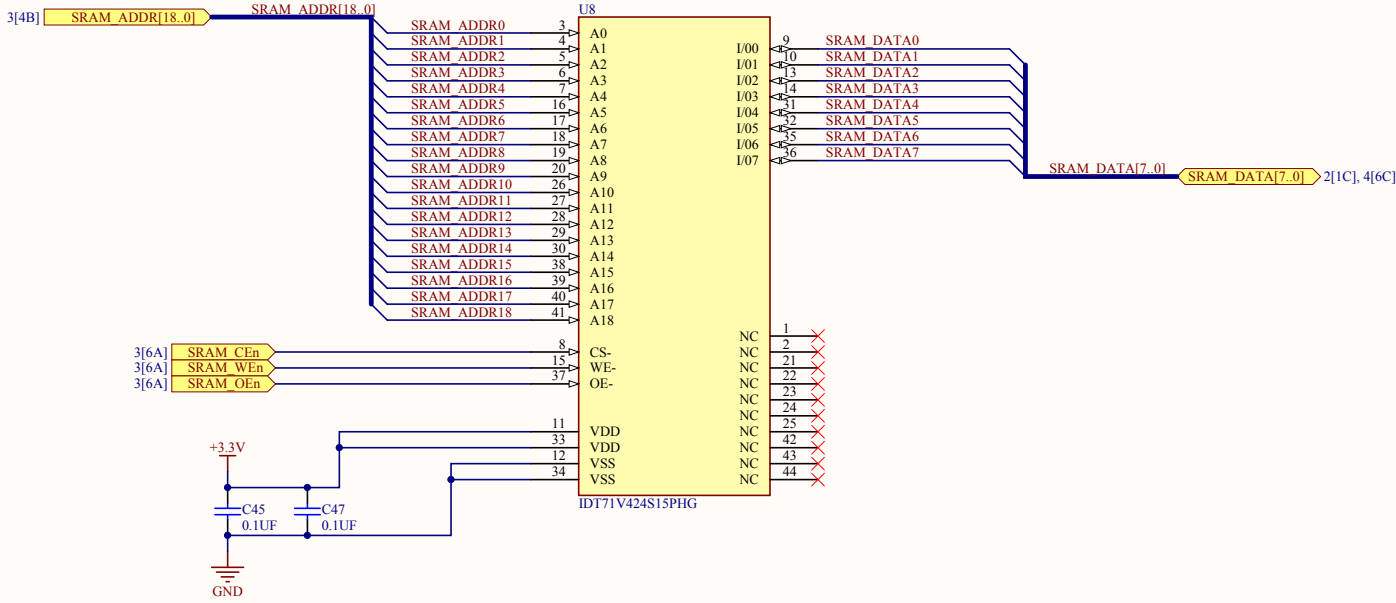


Per EP3C25 pin-out document, tie unused clocks to GND.





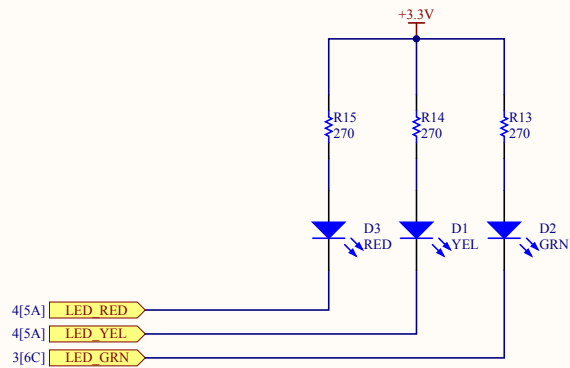
512KX8 SRAM



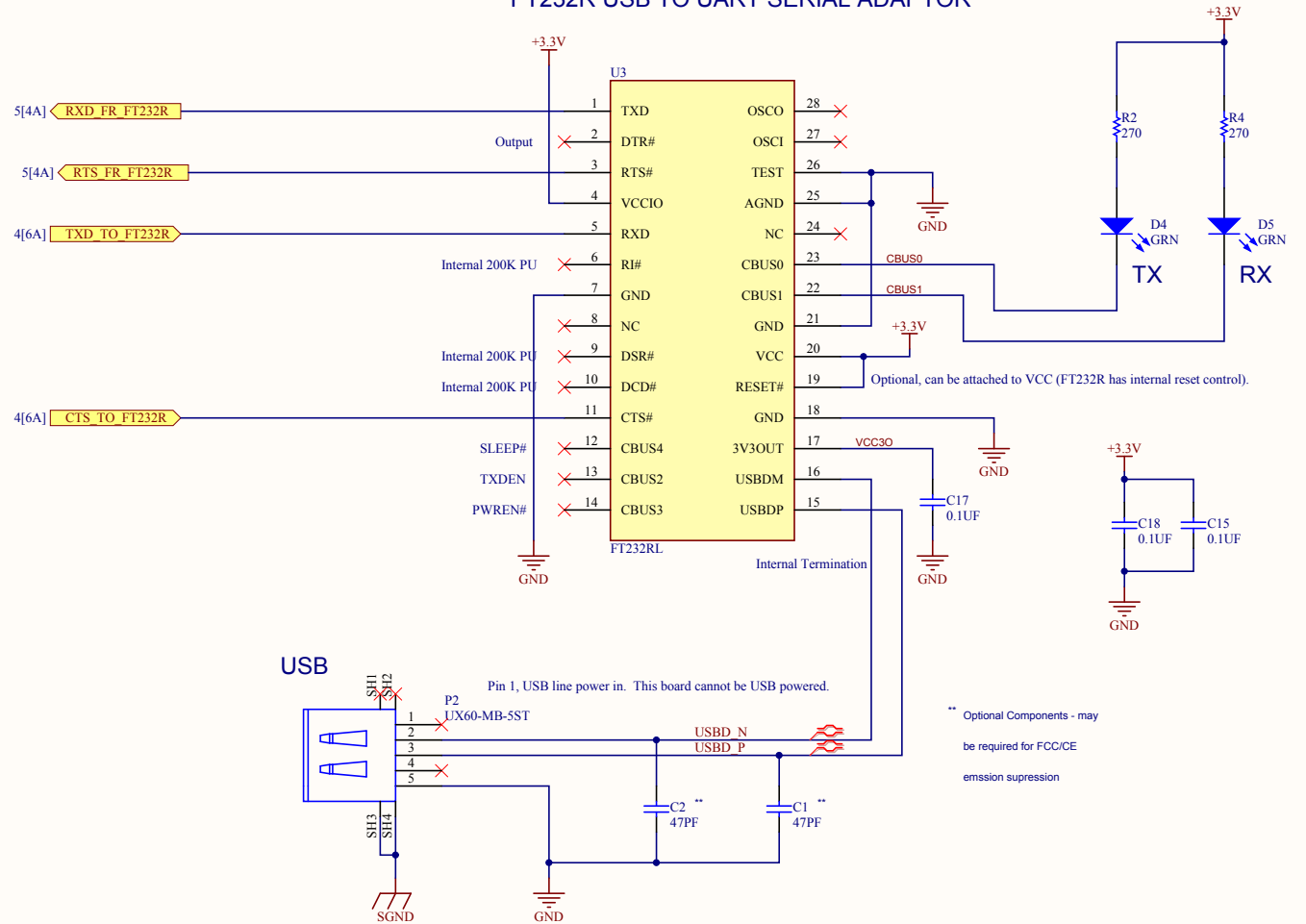
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Size: B	Number: CMCS002M	Revision: A		
Date: 5/15/2009	Time: 11:41:34 PM	Sheet 7 of 9		
File: C:\dallas_logic\altium_dlc\Projects\CMCS002M_REVA\7_SRAM.SchDoc				

Status LEDs



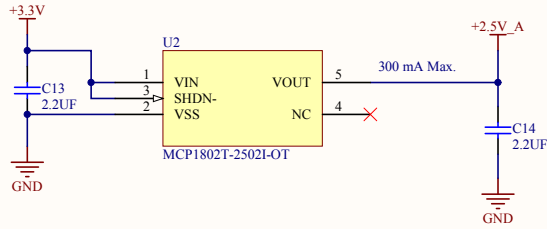
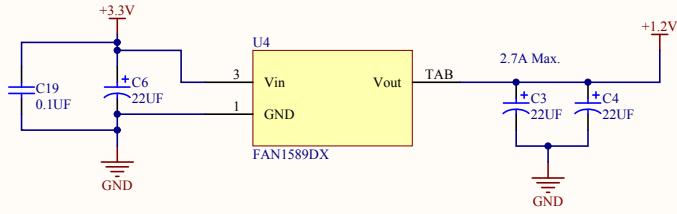
FT232R USB TO UART SERIAL ADAPTOR



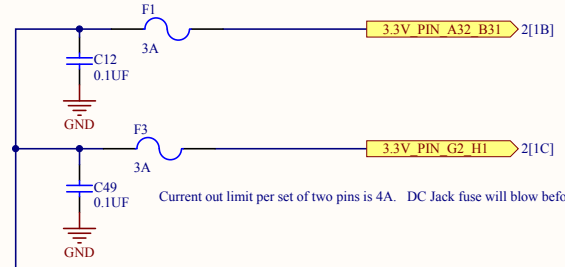
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File: C:\dallas_logic\altium_dlc\Projects\CMCS002M_REVA\8_MISC.SchDoc				

POWER SUPPLY

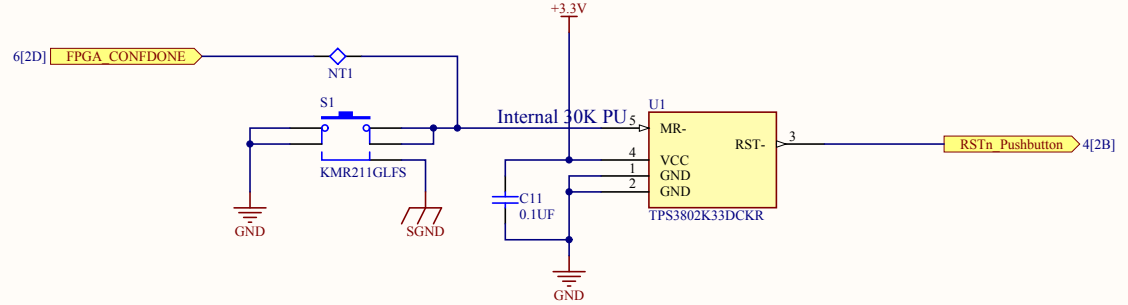
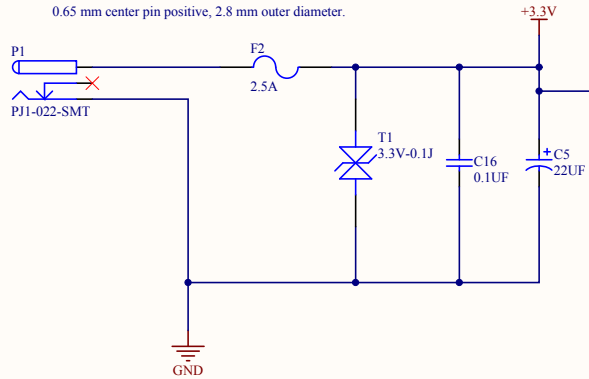


Remove fuses if other card in stack sources 3.3V power rail and local DCJACK is attached and powered (should not do this).
May also pull current in from 3.3V pin (local power from external source).

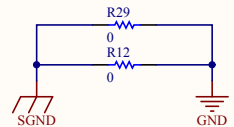


Current out limit per set of two pins is 4A. DC Jack fuse will blow before these will.

DC JACK
INPUT: +3.3V, 2.5A Max.
0.65 mm center pin positive, 2.8 mm outer diameter.



SGND (Shield GND or guard ring) connected to ground power pins at two corners of module.



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