Design Notes

FID2 FID1 LOGO1

FID4 FID3

1) EP4C115E device schematic symbol has been pin swapped. DO NOT UPDATE EP4C115E SCHEMATIC SYMBOL FROM LIBRARY!

2) CMC1003 is configured as a Cardstac master card.

3) FPGA CLOCK PIN INFO:

CMC1003 Clock Pin Utilization
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4) This design will support EP4CE15, EP4CE30, EP4CE40, EP4CE55, EP4CE75, EP4CE115 devices (BGA 484).

5) Enable FPGA IO pin series terminators on all pin header output pins and set minimal slew rate.

TABLE OF CONTENTS:

REVISION TABLE

08-29-11	A	ET	Initial release of the schematic.
10-13-12	B	ET	Added series resistor to FPGA JTAG port on TCK pin.

Title	*Cardstac Cnt., Std. Size, Altera 4CE115*		Dallas Logic Corporation 801 E. Plano Parkway Suite 158 Plano TX 75074 USA
Size: B	Number:CMC1003	Revision:B	
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0.1 INCH HEADER CONNECTORS - 128 PIN (4 row x 32)

3[4A], 3[4D], 4[5A] HDR_B[30..1] → HDR_B[30..1]

P3B — ROW B — CARDSTAC_STD_64X2_REL2_1

HDR_B1	B1	1SPI_CLK
HDR_B2	B2	1SPI_MOSI/5TX
HDR_B3	B3	1SPI_MISO/5RX
HDR_B4	B4	1SPI_SSN3-/4TX
HDR_B5	B5	1SPI_SSN2-/3TX
HDR_B6	B6	1SPI_SSN1-/4RTS
HDR_B7	B7	1SPI_SSN0-/3RTS
HDR_B8	B8	IRQ7B- / 4RX
HDR_B9	B9	IRQ6B- / 3RX
HDR_B10	B10	S-D15 / IO7B
HDR_B11	B11	S-D14 / IO6B
HDR_B12	B12	S-D13 / IO5B
HDR_B13	B13	S-D12 / IO4B
HDR_B14	B14	S-D11 / IO3B
HDR_B15	B15	S-D10 / IO2B
HDR_B16	B16	S-D9 / IO1B
HDR_B17	B17	S-D8 / IO0B
HDR_B18	B18	S-D7
HDR_B19	B19	S-D6
HDR_B20	B20	S-D5
HDR_B21	B21	S-D4
HDR_B22	B22	S-D3
HDR_B23	B23	S-D2
HDR_B24	B24	S-D1
HDR_B25	B25	S-D0
HDR_B26	B26	S-SEL4-
HDR_B27	B27	S-SEL3-
HDR_B28	B28	S-SEL2-
HDR_B29	B29	S-SEL1-
HDR_B30	B30	S-SEL0-
	B31	3.3V
	B32	VAUX0 / 12V

PWR

11[3C] 3.3V_PIN_A32_B31

11[3D] 3.3V_PIN_G2_H1

PWR

P3C — ROW G — CARDSTAC_STD_64X2_REL2_1

	G1	VAUX0 / 12V
	G2	3.3V
HDR_G3	G3	CS0-
HDR_G4	G4	CS1-
HDR_G5	G5	CS2-
HDR_G6	G6	CS3-
HDR_G7	G7	CS4-
HDR_G8	G8	DATA0
HDR_G9	G9	DATA1
HDR_G10	G10	DATA2
HDR_G11	G11	DATA3
HDR_G12	G12	DATA4
HDR_G13	G13	DATA5
HDR_G14	G14	DATA6
HDR_G15	G15	DATA7
HDR_G16	G16	DATA8 / IO0A
HDR_G17	G17	DATA9 / IO1A
HDR_G18	G18	DATA10 / IO2A
HDR_G19	G19	DATA11 / IO3A
HDR_G20	G20	DATA12 / IO4A
HDR_G21	G21	DATA13 / IO5A
HDR_G22	G22	DATA14 / IO6A
HDR_G23	G23	DATA15 / IO7A
HDR_G24	G24	IRQ2A- / 0RX
HDR_G25	G25	IRQ3A- / 1RX
HDR_G26	G26	0SPI_SSN0-/0RTS
HDR_G27	G27	0SPI_SSN1-/1RTS
HDR_G28	G28	0SPI_SSN2-/0TX
HDR_G29	G29	0SPI_SSN3-/1TX
HDR_G30	G30	0SPI_MISO/2RX
HDR_G31	G31	0SPI_MOSI/2TX
HDR_G32	G32	0SPI_CLK

4[5C], 5[4B] HDR_G[32..3] → HDR_G[32..3]

+3.3V

R3 1.8K, R4 1.8K, R2 1.8K

P3A — ROW A — CARDSTAC_STD_64X2_REL2_1

	A1	GND
	A2	I1C_SCL
	A3	I1C_SDA
	A4	IRQ5B- / 4CTS
	A5	IRQ4B- / 3CTS
	A6	S-CLK4
	A7	GND
	A8	S-CLK3
	A9	S-DP1
	A10	S-DP0
	A11	S-STAT9
	A12	S-SYNC-
	A13	GND
	A14	S-CLK2
	A15	S-STAT8
	A16	S-STAT7
	A17	S-STAT6
	A18	S-CLK1
	A19	GND
	A20	S-READ-
	A21	S-STAT5
	A22	S-STAT4
	A23	S-STAT3
	A24	S-WRITE-
	A25	GND
	A26	CLK1 (S-CLK0)
	A27	S-STAT2
	A28	S-STAT1
	A29	S-STAT0
	A30	RST-
	A31	GND
	A32	3.3V

3[4A], 4[5A] HDR_A[6..2] → HDR_A[6..2]

HDR_A2	A2
HDR_A3	A3
HDR_A4	A4
HDR_A5	A5
HDR_A6	A6

3[4B], 3[4C] HDR_A[12..8] → HDR_A[12..8]

HDR_A8	A8
HDR_A9	A9
HDR_A10	A10
HDR_A11	A11
HDR_A12	A12

3[4C] HDR_A[18..14] → HDR_A[18..14]

HDR_A14	A14
HDR_A15	A15
HDR_A16	A16
HDR_A17	A17
HDR_A18	A18

3[4D] HDR_A[24..20] → HDR_A[24..20]

HDR_A20	A20
HDR_A21	A21
HDR_A22	A22
HDR_A23	A23
HDR_A24	A24

3[4D] HDR_A[29..26] → HDR_A[29..26]

HDR_A26	A26
HDR_A27	A27
HDR_A28	A28
HDR_A29	A29

+3.3V

R25 1.8K

4[4A] HDR_H3_A30_RST-

RST- signal is open drain. Program FPGA to drive this low OR as input (float).

This allows the FPGA to read the system reset state.

P3D — ROW H — CARDSTAC_STD_64X2_REL2_1

	H1	3.3V
	H2	GND
	H3	RST-
HDR_H4	H4	ADD0
HDR_H5	H5	ADD1
HDR_H6	H6	ADD2
HDR_H7	H7	CLK0
	H8	GND
HDR_H9	H9	WRITE-
HDR_H10	H10	ADD3
HDR_H11	H11	ADD4
HDR_H12	H12	ADD5
HDR_H13	H13	READ-
	H14	GND
HDR_H15	H15	ADD6
HDR_H16	H16	ADD7
HDR_H17	H17	ADD8
HDR_H18	H18	ADD9
HDR_H19	H19	ADD10
	H20	GND
HDR_H21	H21	ADD11
HDR_H22	H22	ADD12
HDR_H23	H23	ADD13
HDR_H24	H24	ADD14 / WAIT-
HDR_H25	H25	ADD15 / BE0-
	H26	GND
HDR_H27	H27	ADD16 / BE1-
HDR_H28	H28	IRQ0A- /0CTS
HDR_H29	H29	IRQ1A- /1CTS
HDR_H30	H30	0I2C_SDA
HDR_H31	H31	0I2C_SCL
	H32	GND

5[4C] HDR_H[7..4] → HDR_H[7..4]

5[4C] HDR_H[13..9] → HDR_H[13..9]

+3.3V

R20 1.8K, R21 1.8K, R22 1.8K

4[5D], 5[4B] HDR_H[19..15] → HDR_H[19..15]

5[4B] HDR_H[25..21] → HDR_H[25..21]

GND

HDR_H[31..27] → HDR_H[31..27] 4[5D], 5[4A]

Title	*Cardstac Cnt., Std. Size, Altera 4CE115*		Dallas Logic Corporation 801 E. Plano Parkway Suite 158 Plano TX 75074 USA
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FPGA 1

BANK VOLTAGE 3.3V

U8A

BANK 1

IO, DIFFIO_L1p	H7	
IO, DIFFIO_L1n, (DQ2L)/(DQ1L)/(DQ1L)	G3	HDR_B8
IO, DIFFIO_L3p, (nRESET), (DQ2L)/(DQ1L)/(DQ1L)	E4	HDR_B2
IO, DIFFIO_L2n, (DQ2L)/(DQ1L)/(DQ1L)	B1	
IO, VREFB1N0	G5	
IO, DIFFIO_L5p, (DQ2L)/(DQ1L)/(DQ1L)	D2	HDR_B6
IO, DIFFIO_L6n	F6	HDR_B5
IO, DIFFIO_L2p, (DQ2L)/(DQ1L)/(DQ1L)	B2	HDR_B3
IO, DIFFIO_L6p, (DQ2L)/(DQ1L)/(DQ1L)	H6	HDR_B1
IO, DIFFIO_L3n, (DQ2L)/(DQ1L)/(DQ1L)	E3	HDR_B4
IO, DIFFIO_L5n, (DATA1,ASDO)	D1	1SPI_CLK
IO, DIFFIO_L8n, (_)/(DQ1L)/(DQ1L)	E1	HDR_B10
IO, DIFFIO_L23n, (DQ0L)/(DQ1L)/(DQ1L)	J1	HDR_B13
IO, DIFFIO_L7n	H3	
IO, DIFFIO_L8p, (FLASH_nCE,nCSO)	E2	HDR_A4
IO, DIFFIO_L4p, (DQS2L/CQ3L,CDPCLK0)/(DQS2L/CQ3L,CDPCLK0)/(DQS2L/CQ3L,CDPCLK0)	C2	
IO, DIFFIO_L4n, (DQ2L)/(DQ1L)/(DQ1L)	C1	HDR_B7
IO, DIFFIO_L9p, (DM2L)/(DM1L/BWS#1L)/(DM1L/BWS#1L)	F2	HDR_A5
IO	H4	
IO, VREFB1N1	H5	
IO, DIFFIO_L23p	J2	HDR_B12
IO, DIFFIO_L12p, (DQS0L/CQ1L,DPCLK0)/(DQS0L/CQ1L,DPCLK0)/(DQS0L/CQ1L,DPCLK0)	J4	HDR_B9
IO, DIFFIO_L9n, (DQ0L)/(DQ1L)/(DQ1L)	F1	HDR_A9
IO, VREFB1N2	J3	
IO, DIFFIO_L13p	H2	HDR_B11
IO, DIFFIO_L13n	H1	HDR_A10
IO, (DATA0)	K1	

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HDR_B[30..1] → HDR_B[30..1] 2[1A], 3[4D], 4[5A]

HDR_A[6..2] → HDR_A[6..2] 2[4A], 4[5A]

FPGA_ASDO 8[2C]

FPGA_NCSO 8[2C]

HDR_A[12..8] → HDR_A[12..8] 2[4A], 3[4C]

FPGA_DATA0 8[2C]

GND

BANK1

BANK1

BANK VOLTAGE 3.3V

U8B

BANK 2

IO, DIFFIO_L28p, (DQ1L)/(DQ3L)/(DQ1L)	M4	HDR_B14
IO, DIFFIO_L36n	N6	HDR_B16
IO, DIFFIO_L25p, (DQ0L)/(DQ1L)/(DQ1L)	L6	HDR_A12
IO, DIFFIO_L27n	M1	HDR_A11
IO, DIFFIO_L25n, (_)/(DQ1L)/(DQ1L)	M6	HDR_A[12..8] → HDR_A[12..8] 2[4A], 3[4B]
IO, DIFFIO_L28n, (DQ1L)/(DQ3L)/(DQ1L)	M3	HDR_A15
IO, DIFFIO_L32n, (DQ1L)/(DQ3L)/(DQ1L)	N5	HDR_B15
IO, DIFFIO_L27p, (DM0L)/(DM1L/BWS#1L)/(DM1L/BWS#1L)	M2	HDR_A16
IO, VREFB2N0	M5	HDR_B17
IO, DIFFIO_L33n	P3	HDR_B20
IO, DIFFIO_L29p, (DQ1L)/(DQ3L)/(DQ1L)	N2	HDR_A17
IO, DIFFIO_L31n	R1	HDR_A21 HDR_A[18..14] → HDR_A[18..14] 2[4A]
IO, DIFFIO_L30p	P2	HDR_A20
IO, DIFFIO_L29n	N1	
IO, DIFFIO_L34n, (DM1L/BWS#1L)/(DM3L/BWS#3L)/(DM1L/BWS#1L)	U1	HDR_B18
IO, DIFFIO_L33p, (DQS1L/CQ1L#,DPCLK1)/(DQS1L/CQ1L#,DPCLK1)/(DQS1L/CQ1L#,DPCLK1)	P4	HDR_B22
IO, DIFFIO_L38n	W1	HDR_B21
IO, DIFFIO_L31p, (DQ1L)/(DQ3L)/(DQ1L)	R2	HDR_A22 HDR_B25
IO, DIFFIO_L48n, (DM3L/BWS#3L)/(DM3L/BWS#3L)/(DM1L/BWS#1L)	T5	
IO, DIFFIO_L48p, (DQS3L/CQ3L#,CDPCLK1)/(DQS3L/CQ3L#,CDPCLK1)/(DQS3L/CQ3L#,CDPCLK1)	T4	HDR_A23
IO, DIFFIO_L36p, (DQ3L)/(DQ3L)/(DQ1L)	P5	HDR_B26
IO, DIFFIO_L30n, (DQ1L)/(DQ3L)/(DQ1L)	P1	HDR_B19
IO, DIFFIO_L37p, (DQ3L)/(DQ3L)/(DQ1L)	R4	
IO, DIFFIO_L37n, (DQ3L)/(DQ3L)/(DQ1L)	R3	
IO, RUP1	V4	HDR_B29
IO, DIFFIO_L35n	V1	HDR_A24
IO, DIFFIO_L39n	Y1	HDR_A28 HDR_A[24..20] → HDR_A[24..20] 2[4B]
IO, RDN1	V3	HDR_A27
IO, VREFB2N1	T3	
IO, DIFFIO_L40n	AA1	HDR_A29
IO, DIFFIO_L39p, (DQ3L)/(DQ3L)/(DQ1L)	Y2	HDR_A[29..26] → HDR_A[29..26] 2[4B]
IO, DIFFIO_L38p, (DQ3L)/(DQ3L)/(DQ1L)	W2	HDR_B27
IO, VREFB2N2	R5	
IO, DIFFIO_L34p, (DQ1L)/(DQ3L)/(DQ1L)	U2	HDR_B23
IO, DIFFIO_L35p, (DQ3L)/(DQ3L)/(DQ1L)	V2	HDR_B24 HDR_B28

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HDR_B[30..1] → HDR_B[30..1] 2[1A], 3[4A], 4[5A]

GND

BANK2

BANK2

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Dallas Logic Corporation
801 E. Plano Parkway
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FPGA 2

BANK VOLTAGE 3.3V

U8C

BANK 3

IO, DIFFIO_B1n, (DM1B)/(_)/(_)	V5	HDR_A6 SCLK4
IO, DIFFIO_B3p	Y4	HDR_B[30..1] → HDR_B[30..1] 2[1A], 3[4A], 3[4D]
IO, DIFFIO_B5p	AA5	HDR_B30
IO, (DQS1B/CQ1B#,CDPCLK2)/(DQS1B/CQ1B#,CDPCLK2)/(DQS1B/CQ1B#,CDPCLK2)	Y6	LED_YEL → 10[1B]
IO, PLL_1CLKOUTp	AA3	
IO, PLL_1CLKOUTn	AB3	HDR_A26 CLK1
IO, DIFFIO_B4p, (DQ1B)/(_)/(_)	W6	LED_RED → 10[1B]
IO, (DQ1B)/(_)/(_)	AA4	USB_RESET- → 10[3C]
IO, VREFB3N2	AB4	HDR_A[6..2] → HDR_A[6..2] 2[4A], 3[4A]
IO, DIFFIO_B3n, (DQ1B)/(_)/(_)	Y3	HDR_A3
IO, DIFFIO_B7n, (DQ1B)/(_)/(_)	AA6	
IO, DIFFIO_B8p, (DM3B/BWS#3B)/(DM3B/BWS#3B)/(DM5B/BWS#5B)	AB6	
IO, DIFFIO_B8n	AB5	HDR_A2
IO, DIFFIO_B9p, (DQ3B)/(DQ3B)/(DQ5B)	W7	LED_GRN → 10[1B]
IO, DIFFIO_B9n, (DQ3B)/(DQ3B)/(DQ5B)	Y7	HDR_H3_A30_RST- → 2[4C]
IO, DIFFIO_B12n, (DQ3B)/(DQ3B)/(DQ5B)	U9	
IO, DIFFIO_B13p	V8	HDR_A8 SCLK3
IO, DIFFIO_B13n, (DQ3B)/(DQ3B)/(DQ5B)	W8	
IO, DIFFIO_B24p	AA10	ACBUS1
IO, DIFFIO_B23n	Y10	ACBUS0
IO, DIFFIO_B24n	AB10	ACBUS4
IO, VREFB3N1	Y9	
IO, DIFFIO_B15p, (DQS3B/CQ3B#,DPCLK2)/(DQS3B/CQ3B#,DPCLK2)/(DQS3B/CQ3B#,DPCLK2)	V10	
IO, DIFFIO_B15n, (DQ5B)/(DQ3B)/(DQ5B)	U10	
IO, (DQ5B)/(DQ3B)/(DQ5B)	Y8	ACBUS3
IO, DIFFIO_B17n	AB8	ACBUS2
IO, DIFFIO_B18p, (DQ5B)/(DQ3B)/(DQ5B)	AA9	ACBUS6
IO, DIFFIO_B14n, (DM5B/BWS#5B)/(DM3B/BWS#3B)/(DM5B/BWS#5B)	AB7	ACBUS5
IO, VREFB3N0	U11	
IO	V11	HDR_A18 SCLK1
IO, DIFFIO_B23p	W10	HDR_A14 SCLK2
IO, DIFFIO_B14p	AA7	ACBUS9
IO, DIFFIO_B17p, (DQ5B)/(DQ3B)/(DQ5B)	AA8	ACBUS8
IO, DIFFIO_B18n, (DQS5B/CQ5B#,DPCLK3)/(DQS5B/CQ5B#,DPCLK3)/(DQS5B/CQ5B#,DPCLK3)	AB9	ACBUS7

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ACBUS[9..0] → ACBUS[9..0] 10[6C]

ADBUS[7..0] → ADBUS[7..0] 10[6B]

BANK VOLTAGE 3.3V

U8D

BANK 4

IO, DIFFIO_B35n, (DQ4B)/(DQ5B)/(DQ5B)	AB14	ADBUS1
IO, DIFFIO_B32n, (DQ4B)/(DQ5B)/(DQ5B)	AB13	ADBUS0
IO, DIFFIO_B37n, (DQ4B)/(DQ5B)/(DQ5B)	AB15	ADBUS3
IO, DIFFIO_B32p, (_)/(DQ5B)/(DQ5B)	AA13	ADBUS2
IO, VREFB4N2	V12	
IO, DIFFIO_B36p, (DQ4B)/(DQ5B)/(DQ5B)	W13	DDR2_PWR_OFF → 11[1B]
IO, DIFFIO_B36n, (DQS4B/CQ5B,DPCLK4)/(DQS4B/CQ5B,DPCLK4)/(DQS4B/CQ5B,DPCLK4)	V13	
IO, DIFFIO_B40p, (DQ2B)/(DQ5B)/(DQ5B)	AA16	ADBUS5
IO, DIFFIO_B37p, (DQ4B)/(DQ5B)/(DQ5B)	AA15	ADBUS4
IO, DIFFIO_B38p	U12	
IO, DIFFIO_B39p	Y14	
IO, DIFFIO_B39n, (DQ2B)/(DQ5B)/(DQ5B)	Y15	
IO, (DQ0B)/(_)/(_)	AB18	ADBUS7
IO, DIFFIO_B40n, (DQ2B)/(DQ5B)/(DQ5B)	AB16	ADBUS6
IO, DIFFIO_B41p, (DQS2B/CQ3B,DPCLK5)/(DQS2B/CQ3B,DPCLK5)/(DQS2B/CQ3B,DPCLK5)	V13	
IO, DIFFIO_B41n	W14	
IO, DIFFIO_B43p	V14	
IO, DIFFIO_B44p, (DQ2B)/(DQ5B)/(DQ5B)	U14	
IO, DIFFIO_B48p, (DQ0B)/(_)/(_)	W17	HDR_G24
IO, DIFFIO_B35p	AA14	HDR_G25
IO, DIFFIO_B45p, (DQ2B)/(DQ5B)/(DQ5B)	W15	HDR_G23
IO, DIFFIO_B46n, (DQ0B)/(_)/(_)	T15	
IO, DIFFIO_B47p, (DQ0B)/(_)/(_)	AA17	HDR_G[32..3] → HDR_G[32..3] 2[1D], 5[4B]
IO, DIFFIO_B47n	AB17	
IO, VREFB4N1	AA18	
IO, RUP2	AA19	
IO, RDN2	AB19	HDR_H28
IO, DIFFIO_B44n	V15	HDR_H17
IO, DIFFIO_B48n, (DQS0B/CQ1B,CDPCLK3)/(DQS0B/CQ1B,CDPCLK3)/(DQS0B/CQ1B,CDPCLK3)	V17	HDR_H18
IO, DIFFIO_B49p	AA20	HDR_H29
IO, DIFFIO_B49n, (DQ0B)/(_)/(_)	AB20	HDR_H31
IO, VREFB4N0	V16	
IO, PLL4_CLKOUTp	T16	HDR_H[31..27] → HDR_H[31..27] 2[4D], 5[4A]
IO, PLL4_CLKOUTn	R16	HDR_H[19..15] → HDR_H[19..15] 2[4C], 5[4B]
		HDR_H7 CLK0

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BANK3 BANK3 BANK4 BANK4 GND

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Dallas Logic Corporation
801 E. Plano Parkway
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Plano TX 75074 USA

FPGA 3

BANK VOLTAGE 3.3V

U8E

BANK 5

IO, RDN3	T18	
IO, DIFFIO_R50n, (DQS3R/CQ3R#,CDPCLK4)/(DQS3R/CQ3R#,CDPCLK4)/(DQS3R/CQ3R#,CDPCLK4)	W20	HDR_G30
IO, DIFFIO_R51p	AA21	HDR_G31
IO, DIFFIO_R49n, (DQ3R)/(DQ3R)/(DQ1R)	Y22	HDR_G28
IO, VREFB5N2	W19	
IO, RUP3	T17	HDR_G32
IO, DIFFIO_R49p	R17	
IO, DIFFIO_R43p	V21	HDR_G26
IO, DIFFIO_R48p	M16	
IO, DIFFIO_R46n, (DQ3R)/(DQ3R)/(DQ1R)	W22	
IO, DIFFIO_R46p	W21	HDR_G29
IO, DIFFIO_R45n, (DQ3R)/(DQ3R)/(DQ1R)	T20	
IO, DIFFIO_R45p, (DQ3R)/(DQ3R)/(DQ1R)	T19	
IO, DIFFIO_R43n, (DQ3R)/(DQ3R)/(DQ1R)	V22	
IO, DIFFIO_R48n, (DQ3R)/(DQ3R)/(DQ1R)	U20	HDR_G27
IO, DIFFIO_R40p	R19	HDR_G22
IO, DIFFIO_R41p	U21	
IO, DIFFIO_R41n, (DQ1R)/(DQ3R)/(DQ1R)	U22	
IO, DIFFIO_R38p	R21	HDR_G21
IO, DIFFIO_R42n, (DM1R/BWS#1R)/(DM3R/BWS#3R)/(DM1R/BWS#1R)	R20	
IO, DIFFIO_R38n, (DQ1R)/(DQ3R)/(DQ1R)	R22	
IO, VREFB5N1	P20	
IO, DIFFIO_R33n	N20	
IO, DIFFIO_R36p	P21	HDR_G20
IO, DIFFIO_R36n	P22	HDR_G19
IO, VREFB5N0	N19	
IO, DIFFIO_R28n, (DQ1R)/(DQ3R)/(DQ1R)	M22	HDR_G18
IO, DIFFIO_R29n, (DEV_OE)	N22	
IO, DIFFIO_R29p, (DEV_CLRn)	N21	
IO, DIFFIO_R30p, (DQS1R/CQ1R#,DPCLK6)/(DQS1R/CQ1R#,DPCLK6)/(DQS1R/CQ1R#,DPCLK6)	N18	
IO, DIFFIO_R27p, (_)/(DQ1R)/(DQ1R)	M19	
IO, DIFFIO_R28p	M21	HDR_G17
IO, DIFFIO_R27n, (DM0R)/(DM1R/BWS#1R)/(DM1R/BWS#1R)	M20	HDR_G16

EP4CE115F23C8N

BANK5 BANK5

HDR_H30 HDR_H27 HDR_H25 HDR_H24 HDR_H23 HDR_H22 HDR_H21 HDR_H19 HDR_H16 HDR_H15

0SPI_CLK

HDR_H[31..27] → HDR_H[31..27] 2[4D], 4[5D]

HDR_H[25..21] → HDR_H[25..21] 2[4D]

BANK5

RSTn_Pushbutton 11[3C]

HDR_H[19..15] → HDR_H[19..15] 2[4C], 4[5D]

HDR_G[32..3] → HDR_G[32..3] 2[1D], 4[5C]

+3.3V

R23
10.0K

Allows configuration of a device tristate (drive low to tristate all FPGA pins).

BANK VOLTAGE 3.3V

U8F

BANK 6

IO, DIFFIO_R24n, (INIT_DONE)	L22	
IO, DIFFIO_R24p, (CRC_ERROR)	L21	
IO, VREFB6N2	K19	
IO, DIFFIO_R23n, (nCEO)	K22	
IO, DIFFIO_R23p, (CLKUSR)	K21	
IO, DIFFIO_R22p	J21	
IO, DIFFIO_R22n, (DQS0R/CQ1R,DPCLK7)/(DQS0R/CQ1R,DPCLK7)/(DQS0R/CQ1R,DPCLK7)	J22	HDR_G14
IO, DIFFIO_R21p, (DQ0R)/(DQ1R)/(DQ1R)	H21	
IO, DIFFIO_R18p	F21	
IO, DIFFIO_R20n, (DQ0R)/(DQ1R)/(DQ1R)	K18	HDR_G15
IO, DIFFIO_R20p	J18	
IO, DIFFIO_R18n, (DQ0R)/(DQ1R)/(DQ1R)	F22	
IO, DIFFIO_R14p	D21	
IO, DIFFIO_R17n, (DQ0R)/(DQ1R)/(DQ1R)	J20	
IO, DIFFIO_R21n, (DQ0R)/(DQ1R)/(DQ1R)	H22	HDR_G13
IO, DIFFIO_R16n	H20	HDR_G12
IO, DIFFIO_R15p, (nOE), (DQ2R)/(DQ1R)/(DQ1R)	E21	
IO, DIFFIO_R16p, (_)/(DQ1R)/(DQ1R)	H19	HDR_G8
IO, VREFB6N1	H18	
IO, DIFFIO_R9n, (PADD22)	B22	
IO, DIFFIO_R10n	C22	HDR_G7
IO, DIFFIO_R13n, (nAVD), (DQ2R)/(DQ1R)/(DQ1R)	F20	
IO, DIFFIO_R14n, (DQ2R)/(DQ1R)/(DQ1R)	D22	HDR_G10
IO, DIFFIO_R15n, (nWE), (DQ2R)/(DQ1R)/(DQ1R)	E22	HDR_G11
IO, DIFFIO_R9p, (PADD21), (DQ2R)/(DQ1R)/(DQ1R)	B21	
IO, DIFFIO_R10p, (DQ2R)/(DQ1R)/(DQ1R)	C21	HDR_G6
IO, DIFFIO_R8n, (PADD20), (DQS2R/CQ3R,CDPCLK5)/(DQS2R/CQ3R,CDPCLK5)/(DQS2R/CQ3R,CDPCLK5)	C20	HDR_G3
IO, DIFFIO_R2n	F17	HDR_G4
IO, DIFFIO_R12n, (PADD23), (DQ2R)/(DQ1R)/(DQ1R)	G18	HDR_G5
IO, VREFB6N0	D20	
IO, DIFFIO_R13p	F19	HDR_G9

EP4CE115F23C8N

HDR_H13 HDR_H12 HDR_H11 HDR_H9 HDR_H10

HDR_H[13..9] → HDR_H[13..9] 2[4C]

HDR_H[7..4] → HDR_H[7..4] 2[4C]

LTC3616_PGOOD 11[5A]

BANK6

HDR_H6 HDR_H5 HDR_H4

BANK6 BANK6 BANK6

GND

Title	*Cardstac Cnt., Std. Size, Altera 4CE115*		
Size: B	Number:CMC1003	Revision:B	
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FPGA 4

BANK VOLTAGE 1.8V

U8G

BANK 7

IO, DIFFIO_T49p, (DQ4T)/(DQ5T)/(DQ5T)	B16
IO, DIFFIO_T35n, (PADD11), (_)/(DQ5T)/(DQ5T)	A13
IO, DIFFIO_T59p, (DQS0T/CQ1T,CDPCLK6)/(DQS0T/CQ1T,CDPCLK6)/(DQS0T/CQ1T,CDPCLK6)	F14
IO, DIFFIO_T58n	C18
IO, DIFFIO_T58p, (DQ0T)/(_)/(_)	D18
IO, VREFB7N0	D17
IO, DIFFIO_T45n, (PADD5), (DQ4T)/(DQ5T)/(DQ5T)	A15
IO, DIFFIO_T46n, (PADD3), (DQ4T)/(DQ5T)/(DQ5T)	E14
IO, PLL2_CLKOUTp	B20
IO, PLL2_CLKOUTn	A20
IO, DIFFIO_T45p, (PADD6), (DQ4T)/(DQ5T)/(DQ5T)	B15
IO, RUP4	B19
IO, RDN4	A19
IO, DIFFIO_T53n, (DQ2T)/(DQ5T)/(DQ5T)	A18
IO, DIFFIO_T53p, (PADD0)	B18
IO, DIFFIO_T52n, (DQ2T)/(DQ5T)/(DQ5T)	D15
IO, DIFFIO_T60n, (DQ0T)/(_)/(_)	E16
IO, DIFFIO_T44p, (PADD8), (DQ4T)/(DQ5T)/(DQ5T)	D13
IO, DIFFIO_T50p, (PADD2)	B17
IO, DIFFIO_T49n, (DM2T)/(DM5T/BWS#5T)/(DM5T/BWS#5T)	A16
IO, DIFFIO_T52p, (DQ2T)/(DQ5T)/(DQ5T)	E15
IO, VREFB7N1	C15
IO, DIFFIO_T56n, (DQ0T)/(_)/(_)	C19
IO, DIFFIO_T46p, (PADD4), (DQS2T/CQ3T,DPCLK8)/(DQS2T/CQ3T,DPCLK8)/(DQS2T/CQ3T,DPCLK8)	F13
IO, DIFFIO_T36p, (PADD10)	B14
IO, DIFFIO_T36n, (PADD9), (DQ4T)/(DQ5T)/(DQ5T)	A14
IO, DIFFIO_T44n, (PADD7)	C13
IO, DIFFIO_T50n, (PADD1), (_)/(DQ5T)/(DQ5T)	A17
IO, VREFB7N2	E13
IO, DIFFIO_T60p, (DQ0T)/(_)/(_)	F15
IO, DIFFIO_T56p, (DM0T)/(_)/(_)	D19
IO, DIFFIO_T54p, (DQ2T)/(DQ5T)/(DQ5T)	C17
IO, DIFFIO_T35p, (PADD12), (DQS4T/CQ5T,DPCLK9)/(DQS4T/CQ5T,DPCLK9)/(DQS4T/CQ5T,DPCLK9)	B13
IO, DIFFIO_T33p, (DM4T)/(DM5T/BWS#5T)/(DM5T/BWS#5T)	E12
IO, DIFFIO_T32n, (PADD13)	E11
IO, DIFFIO_T32p, (PADD14), (DQ5T)/(DQ3T)/(DQ5T)	F11

EP4CE115F23C8N

DDR2_DQ15
DDR2_DQ12
DDR2_DQ9
DDR2_DQ8
DDR2_DQ14
DDR2_DQ1
DDR2_DQ0
DDR2_DQ11
DDR2_DQ2
DDR2_DQ6
DDR2_DQ13
DDR2_DQ10
DDR2_DQ3
DDR2_DQ5
DDR2_DQ4
DDR2_DQ7

BANK7

DDR2_RAS- 9[2B]

R18 49.9
R17 49.9
+1.8V
GND

DDR2_WE- 9[2B]
DDR2_LDM 9[3B]
DDR2_LDQS 9[3B]
DDR2_UDQS 9[3C]
DDR2_ODT 9[3B]
DDR2_UDM 9[3C]

C45 0.1UF
C96 0.1UF
C68 0.1UF
GND
PWR
DDR2_VREF 11[3A], 9[3C]

DDR2_DQ[15..0]
DDR2_DQ[15..0] 9[5B]

DDR2_A[13..0]
DDR2_A[13..0] 9[1A]

BANK VOLTAGE 1.8V

U8H

BANK 8

IO, DIFFIO_T31n, (DQ5T)/(DQ3T)/(DQ5T)	D10
IO, DIFFIO_T30n, (DQ5T)/(DQ3T)/(DQ5T)	A10
IO, DIFFIO_T30p, (PADD15)	B10
IO, DIFFIO_T29n, (PADD16), (DQ5T)/(DQ3T)/(DQ5T)	A9
IO, DIFFIO_T29p, (PADD17), (DQS5T/CQ5T#,DPCLK10)/(DQS5T/CQ5T#,DPCLK10)/(DQS5T/CQ5T#,DPCLK10)	B9
IO, VREFB8N0	C10
IO, DIFFIO_T25n, (DATA2), (DQ5T)/(DQ3T)/(DQ5T)	A8
IO, DIFFIO_T25p, (DATA3), (DQ5T)/(DQ3T)/(DQ5T)	B8
IO, DIFFIO_T14n, (DQ3T)/(DQ3T)/(DQ5T)	A4
IO, DIFFIO_T23p, (DATA4), (DM5T/BWS#5T)/(DM3T/BWS#3T)/(DM5T/BWS#5T)	B7
IO, DIFFIO_T15n, (DATA7), (DQ3T)/(DQ3T)/(DQ5T)	C6
IO, DIFFIO_T4n, (DQ1T)/(_)/(_)	C3
IO, DIFFIO_T21n, (DQ3T)/(DQ3T)/(DQ5T)	E9
IO, DIFFIO_T14p, (DATA8)	B4
IO, DIFFIO_T18p, (DATA5), (DQ3T)/(DQ3T)/(DQ5T)	A5
IO, DIFFIO_T19n, (DQ3T)/(DQ3T)/(DQ5T)	D8
IO, DIFFIO_T19p	E8
IO, DIFFIO_T22p, (DATA15), (DQ3T)/(DQ3T)/(DQ5T)	B6
IO, VREFB8N1	B5
IO, DIFFIO_T17p, (DATA6), (DQ3T)/(DQ3T)/(DQ5T)	F10
IO, DIFFIO_T9p, (DATA11)	B3
IO, DIFFIO_T15p	D7
IO, DIFFIO_T22n, (PADD19)	A6
IO, DIFFIO_T23n, (PADD18)	A7
IO, DIFFIO_T11n, (DATA9), (DM3T/BWS#3T)/(DM3T/BWS#3T)/(DM5T/BWS#5T)	F8
IO, DIFFIO_T20n, (DATA14), (DQS3T/CQ3T#,DPCLK11)/(DQS3T/CQ3T#,DPCLK11)/(DQS3T/CQ3T#,DPCLK11)	C8
IO, DIFFIO_T20p, (DATA13)	C7
IO, VREFB8N2	D6
IO, DIFFIO_T7n	E7
IO, DIFFIO_T3n	F7
IO, DIFFIO_T4p, (DATA12), (DQS1T/CQ1T#,CDPCLK7)/(DQS1T/CQ1T#,CDPCLK7)/(DQS1T/CQ1T#,CDPCLK7)	C4
IO, DIFFIO_T9n, (DATA10), (DQ1T)/(_)/(_)	A3
IO, (DQ1T)/(_)/(_)	F9
IO, PLL3_CLKOUTp	E5
IO, PLL3_CLKOUTn	E6

EP4CE115F23C8N

DDR2_A9
DDR2_A10
DDR2_A6
DDR2_A7
DDR2_A13
DDR2_A11
DDR2_A5
DDR2_A8
DDR2_A3
DDR2_A4
DDR2_A0
DDR2_A1
DDR2_A2
DDR2_A12

BANK8

DDR2_CK_N 9[3B]
DDR2_CK_P 9[3B]
DDR2_CAS- 9[2B]
DDR2_BA2 9[2B]
DDR2_BA0 9[2B]
DDR2_BA1 9[2B]
DDR2_CS- 9[2B]
DDR2_CKE 9[3B]

BANK8

Title	*Cardstac Cnt., Std. Size, Altera 4CE115*		
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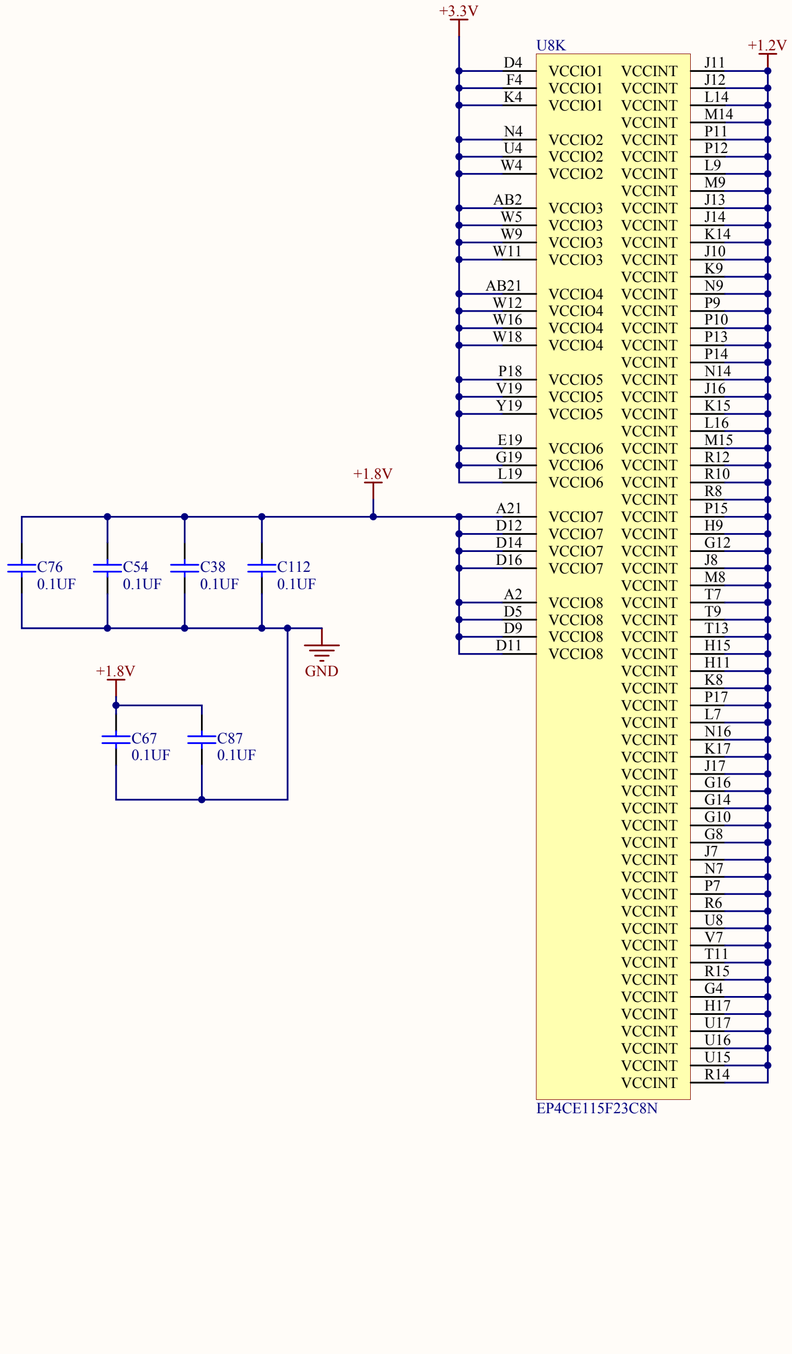
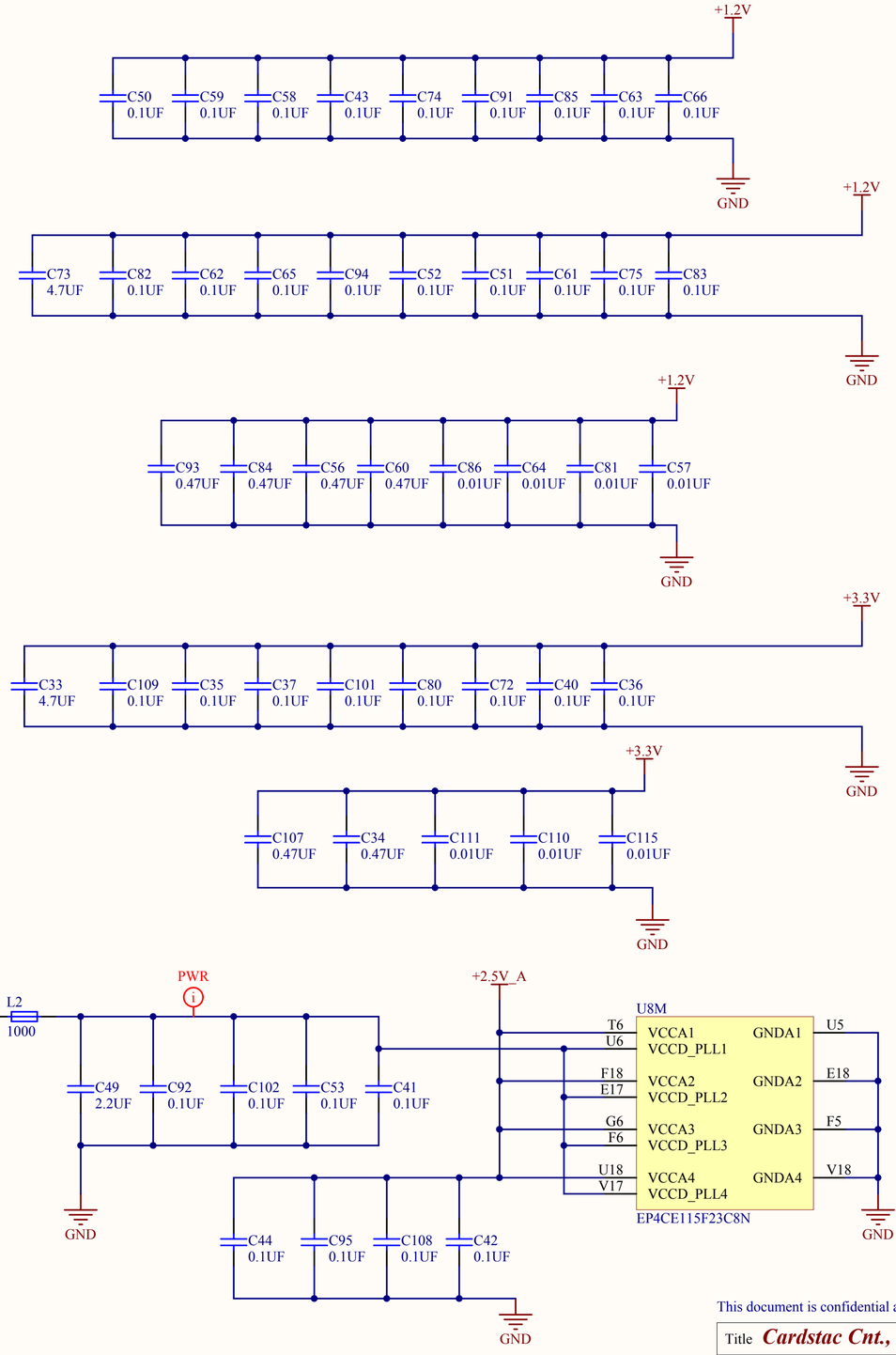
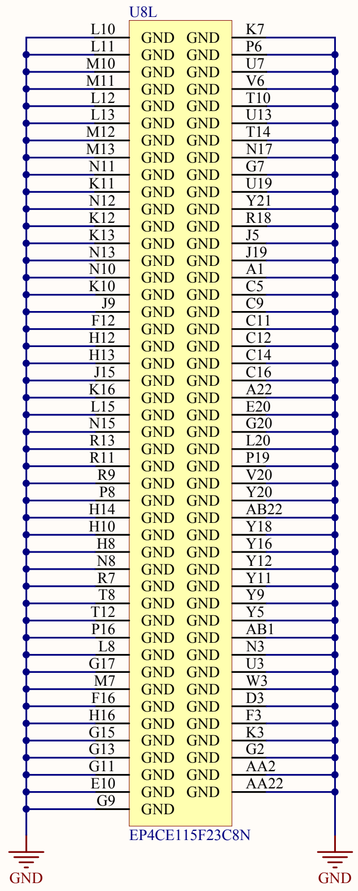
FPGA 5







Title	*Cardstac Cnt., Std. Size, Altera 4CE115*		
Size: B	Number:CMC1003	Revision:B	
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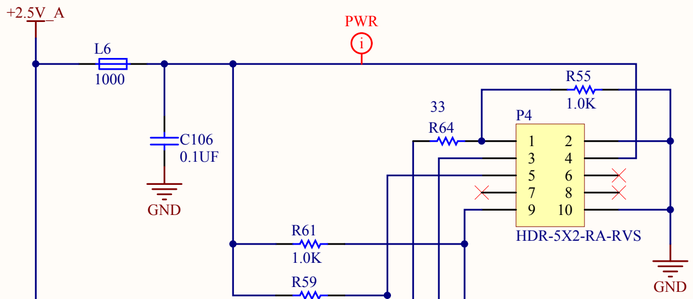
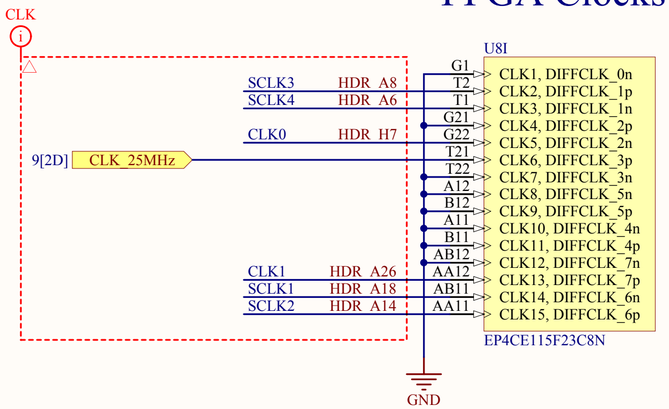
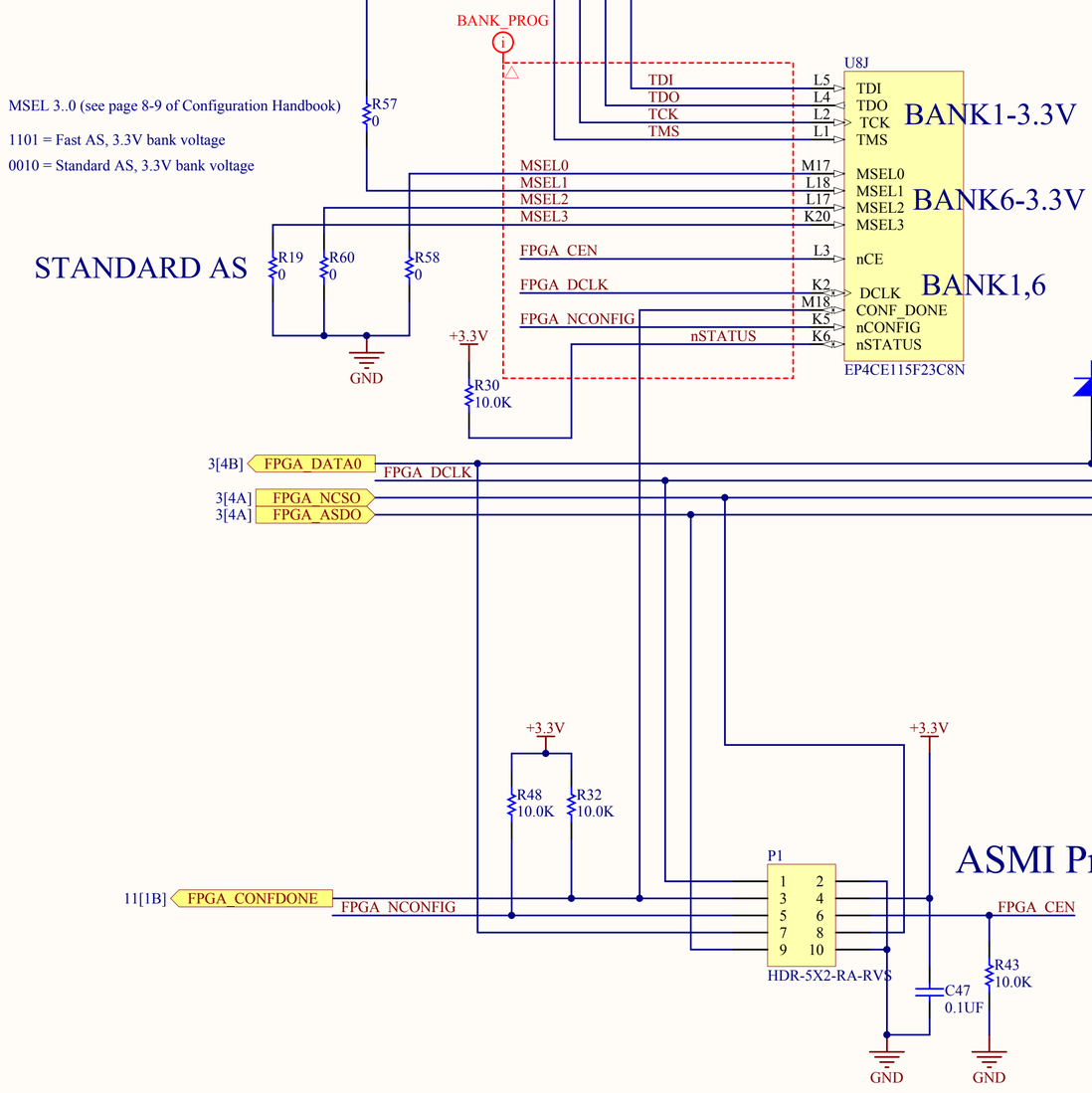
FPGA 6

JTAG Configuration Header



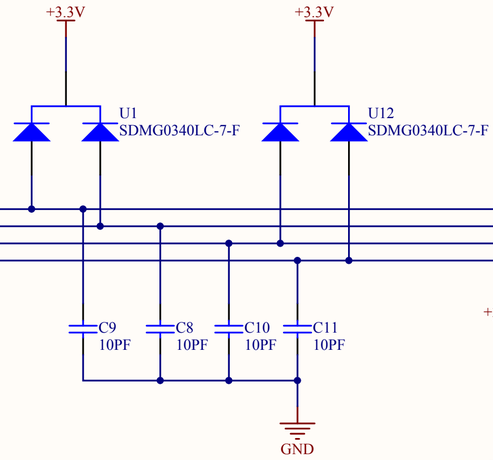
FPGA Clocks





New for Cyclone III, IV to limit ringing. Source series temination is a possible simple alternative.

Locate these devices near FPGA.



FLASH 64Mbit

EP4CE115 requires 28,571,696 bit for configuration (uncompressed).

ASMI Programming Header

Title	*Cardstac Cnt., Std. Size, Altera 4CE115*		Dallas Logic Corporation 801 E. Plano Parkway Suite 158 Plano TX 75074 USA
Size: B	Number:CMC1003	Revision:B	
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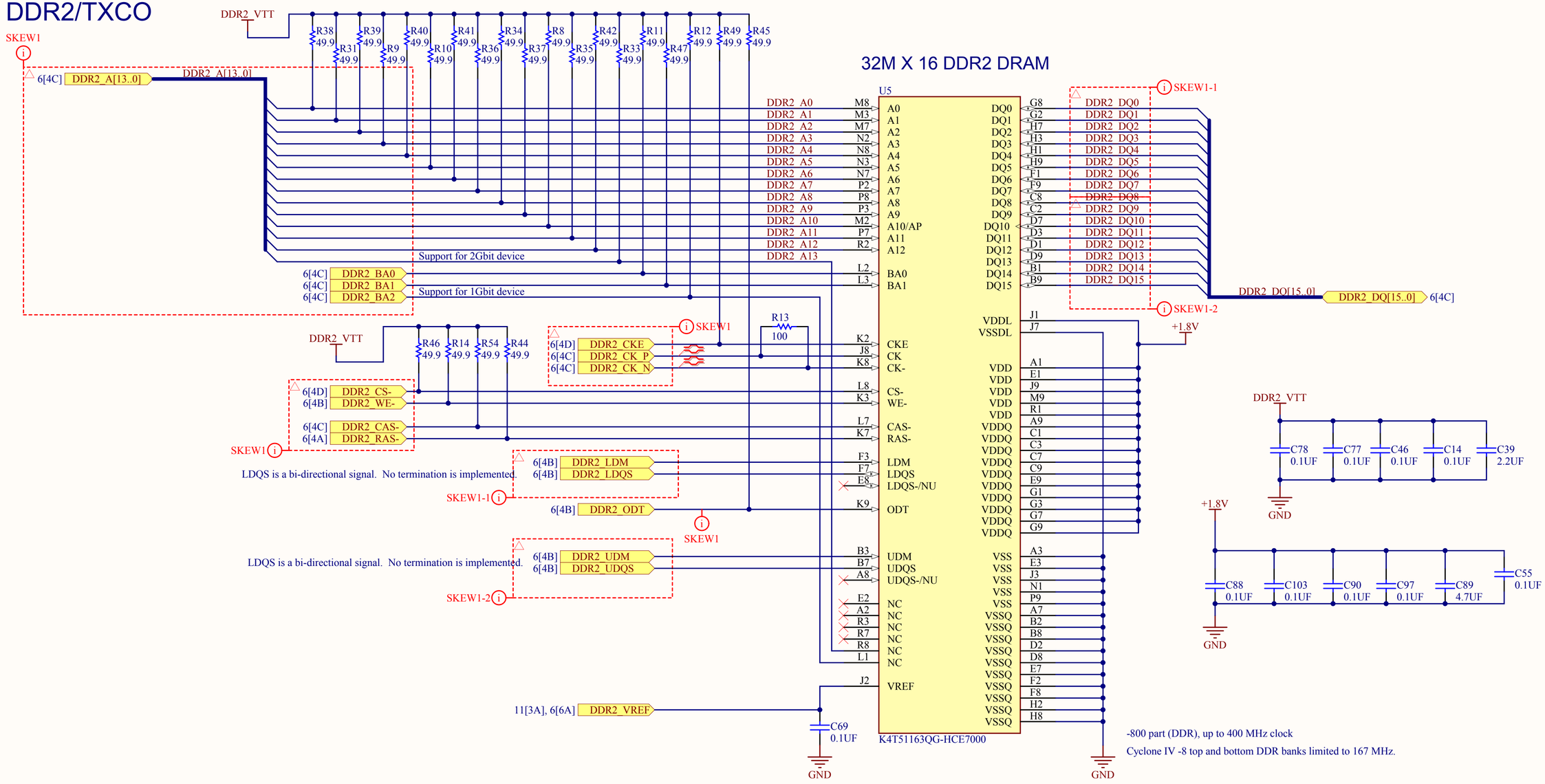
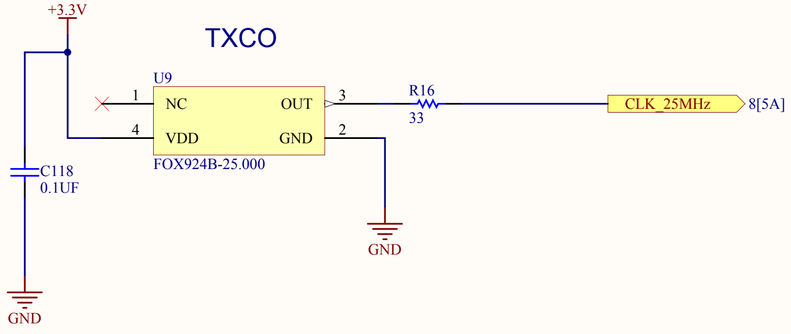
DDR2/TXCO

32M X 16 DDR2 DRAM



TXCO



DQ, UDQS, UDM, LDQS, LDM make up the bidirectional data bus group and have ODT (These are the DDR signals).
CK - differential clock group
A, BA, WE, CAS, RAS, CKE, ODT, CS are in the address/command/control group, no ODT.
DDR2 trace lengths of 62.5mm or less should not require termination.

Match _P to _N differential legs for CK signal to within 10mil.
Match skew group 1-1 to 50 mil (and route on same layer). Match group 1-2 to 50 mil (and route on same layer).
Match skew group 1 to 250 mil.
Skew matching on terminated lines should not include stub to 49.9 Ohm termination resistor.
The CK signal should be equal to the longest address/control group signal or up to 100 mil longer.

See Altera External Memory Interface Handbook Vol. 2, page 1-59 and 1-60 for PCB guidelines.
Good Reference: Micron TN-47-20 DDR2 Package Sizes and Layout Basics.
Good Reference: Freescale AN2910 Hardware and Layout Design Considerations for DDR2 SDRAM Memory Interfaces.

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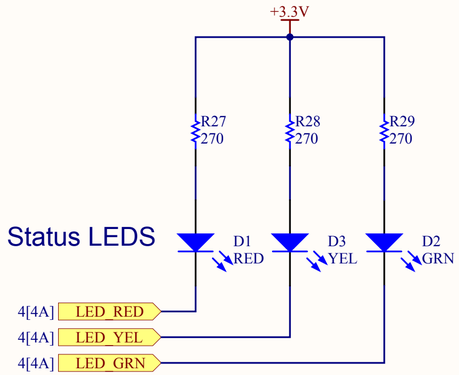
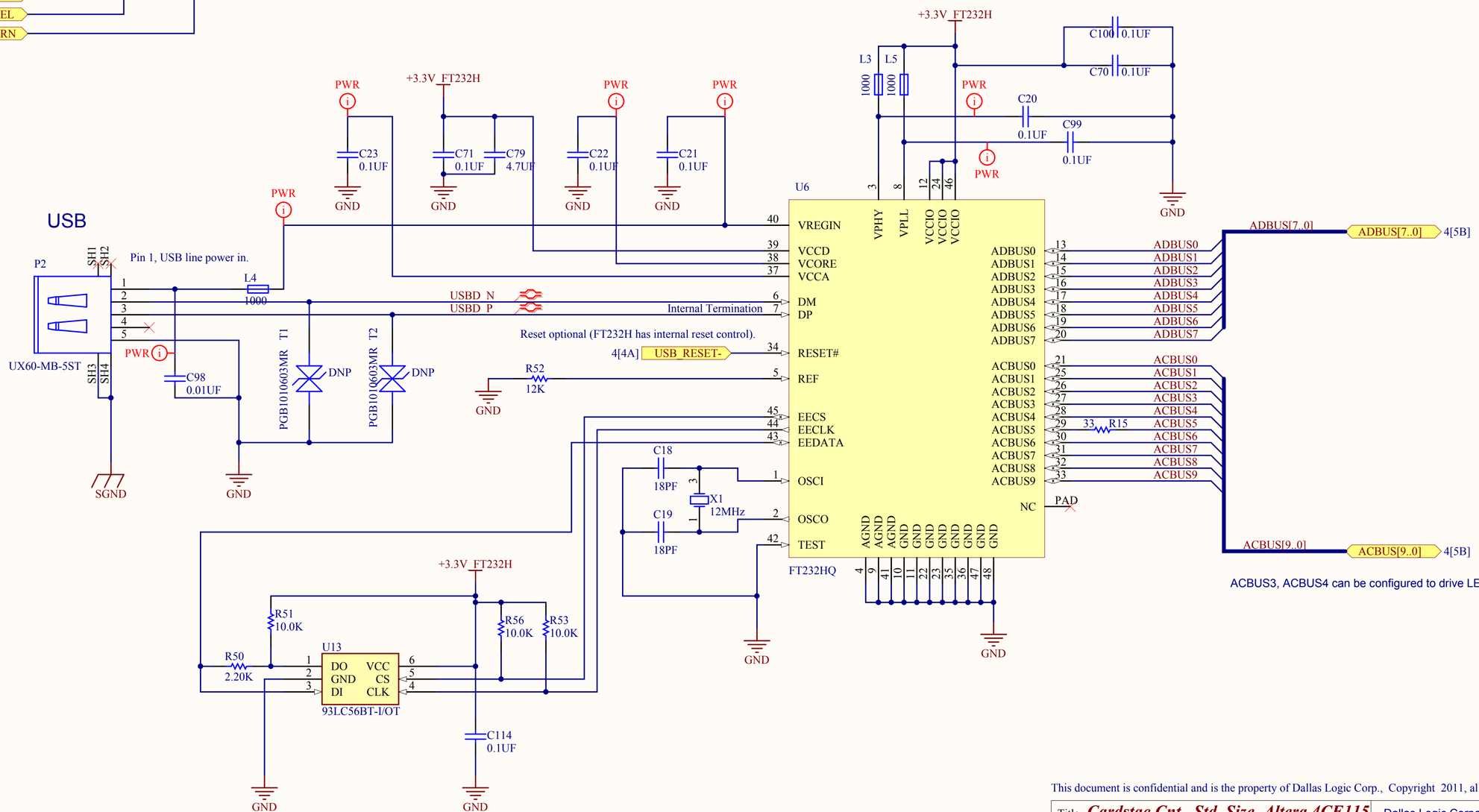
MISC.

Status LEDS



FT232H USB TO UART/FIFO SERIAL ADAPTOR - USB LINE POWERED



Title	*Cardstac Cnt., Std. Size, Altera 4CE115*		
Size: B	Number:CMC1003	Revision:B	
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801 E. Plano Parkway
Suite 158
Plano TX 75074 USA

POWER SUPPLY

+3.3V
C117 0.1UF
GND
VDDQ= INPUT FOR VREF CIRCUIT
U10
PVIN
AVIN
VDDQ
SD-
GND
VREF
VSENSE
VTT
PGND/THERM
PAD
LP2997MR
Specified at +/- 30uA: buffered, but low current
DDR2_VREF 6[6A], 9[3C]
C119 0.1UF
GND
DDR2 0.9V Termination - 900mA peak
DDR2_VTT
C116 0.1UF
C28 47UF
GND
+1.8V
C29 4.7UF
C25 0.1UF
GND
+3.3V
R24 2.20K
4[4C] DDR2_PWR_OFF-
R62 33
ENABLE SLOW SLEW RATE/SERIES TERM FOR DDR2_POWER_OFF- SIGNAL SWITCHING.

C1 4.7UF
C2 47UF
C5 47UF
C15 4.7UF
C16 0.1UF
GND
+3.3V
U3
PVIN
PVIN
PVIN
PVIN
SVIN
ITH
RT/SYNC
RUN
TRACK/SS
MODE
SRLIM/DDR
SGND
PGOOD
VFB
SW
NC
PGND/PAD
LTC3616EUDD#PBF
ITH- AVP (Active Voltage Positioning) mode selected, internal compensation
RT/SYNC- Set 2.25MHz +/- 20% operation
TRACK/SS- Internal soft start, output voltage ramp within 1 ms
MODE- Burst mode operation, internal clamp
SRLIM- Switch slew rate adjust, efficiency -vs- EMI
RUN- FPGA core power enabled at power up (no shutdown)
+3.3V
R1 10.0K
LTC3616_PGOOD 5[5C]
VFB
R6 294K
C12 18PF
R5 294K
L1 0.33UH
FPGA CORE - 6A MAX.
+1.2V
R7 43.0K
25 High current GND
GND
C7 47UF
C17 47UF
C6 47UF
C3 4.7UF
C13 0.1UF
GND
VOUT= 0.6V (1+Rtop/Rbot)
Inductor = Vishay IHLP2525CZERR33M01, 20.0A Max. Operating, 30A Saturation.
Keep SGND (signal ground) and PGND (high current) returns separated, except at connect point near IC.

VOLTAGE MONITOR / RESET

This signal insures that FPGA logic is reset following configuration (and power up).
8[2D] FPGA_CONFDONE
NT1
S1
KMR211GLFS
GND
SGND
+3.3V
Internal 30K PU
U4
MR-
VCC
GND
GND
RST-
TPS3802K33DCKR
RSTn_Pushbutton 5[5B]
C48 0.1UF
GND

POWER INPUT

DC JACK
INPUT: +3.3V, 2.5A Max.
0.65 mm center pin positive, 2.8 mm outer diameter.
P5
PJ-031H-SMT
PWR
F2 2.5A
T3 3.3V-0.1J
C113 0.1UF
GND
+3.3V
F1 4A
C30 0.1UF
3.3V_PIN_A32_B31 2[1B]
F3 4A
C120 0.1UF
3.3V_PIN_G2_H1 2[1C]
Current out limit per set of two pins is 4A. DC Jack fuse will blow before these will.
May also pull current in from 3.3V header pins (local power from external source).

+3.3V
C31 2.2UF
U11
VIN
SHDN-
VSS
VOUT
NC
MCP1802T-2502I-OT
300 mA Max.
+2.5V_A
C32 2.2UF
GND

+3.3V
C24 4.7UF
C104 0.1UF
U7
VIN
VIN
EN
GND
PAD
VOUT
SNS
LP38692SD-1.8
DDR2 DRAM - 1A MAX.
+1.8V
C26 4.7UF
C27 4.7UF
C105 0.1UF
GND

SGND (Shield GND or guard ring) connected to ground power pins at two corners of module.
R26 0
R63 0
SGND
GND

Title	Cardstac Cnt., Std. Size, Altera 4CE115		
Size: B	Number:CMC1003	Revision:B	
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