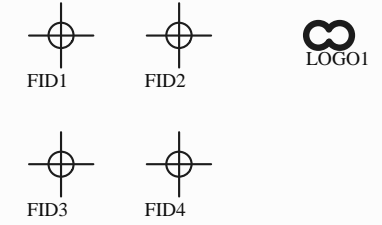


## Design Notes

- 1) CMC5001 is configured as a Cardstac master card.
- 2) CPLD Bank 3 is fixed 3.3V I/O
- 3) Dev OE pin is used as IO, not as reset
- 4) RST\_OUT\_n is reset signal from CPLD
- 5) CPLD\_RST\_n is the CPLD reset from Power Supply



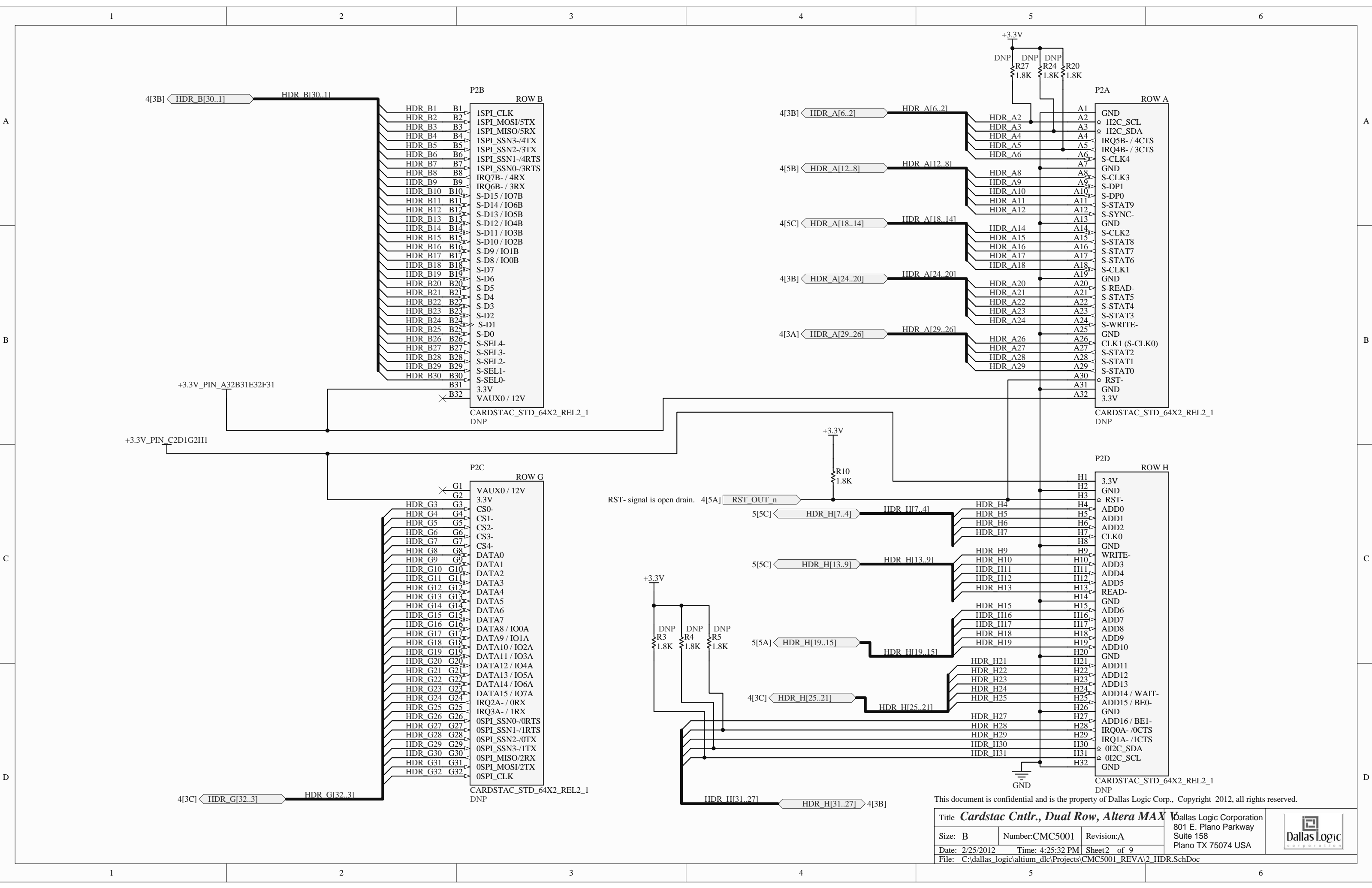
### TABLE OF CONTENTS:

- 1- Cover Sheet
- 2- Header Connectors (Cardstac)
- 3 - Header Connectors 2 (Cardstac)
- 4- CPLD page 1 (MAX V)
- 5- CPLD page 2 (MAX V)
- 6- CPLD Power (MAX V)
- 7- CPLD Misc (MAX V)
- 8- Miscellaneous devices, LED, Switches
- 9- Power Supply Input

REVISION TABLE			
02-25-12	A	ET	Initial release of the schematic.

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Title <b>Cardstac Cntrl., Dual Row, Altera MAX</b>		Dallas Logic Corporation 801 E. Plano Parkway Suite 158 Plano TX 75074 USA		
Size: <b>B</b>	Number: CMC5001	Revision: A		
Date: 2/25/2012	Time: 4:25:31 PM	Sheet 1 of 9		
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Date: 2/25/2012	Time: 4:25:32 PM	Sheet 2 of 9			
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A

B

C

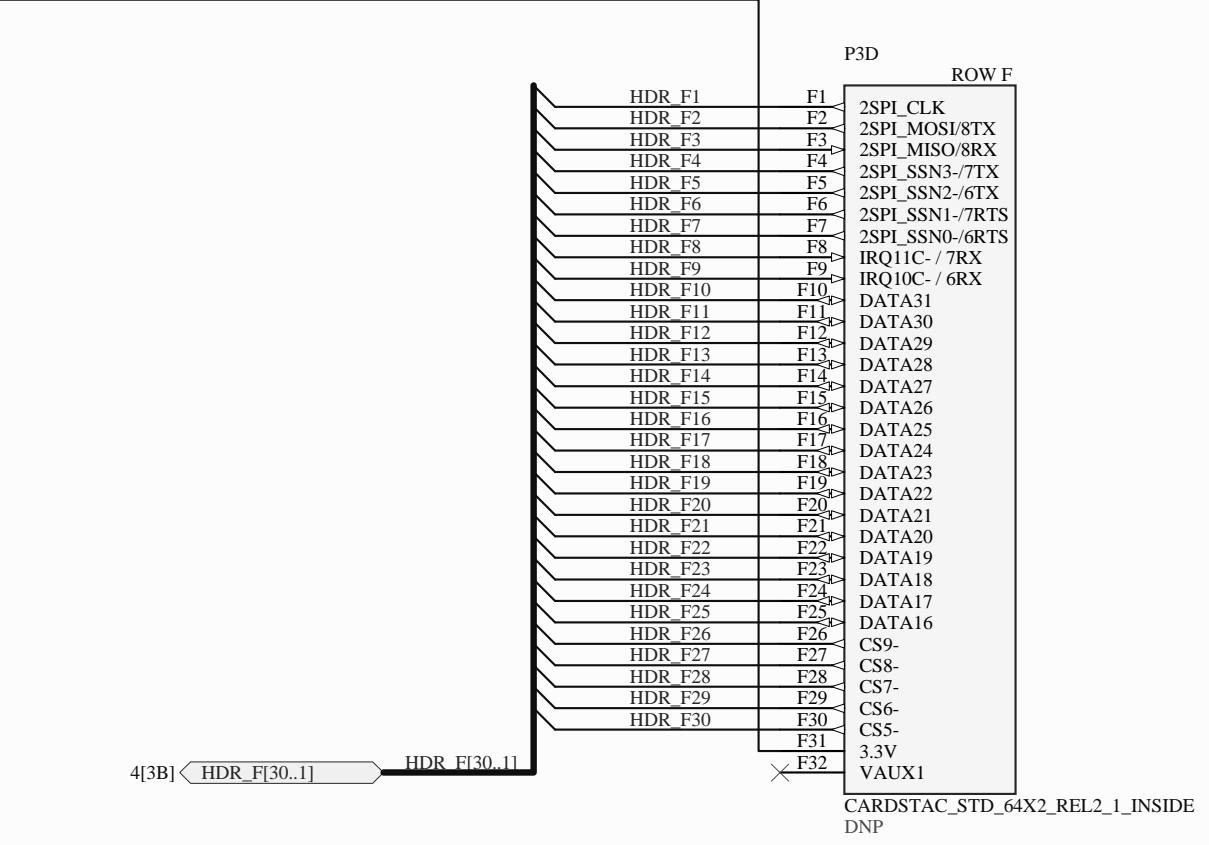
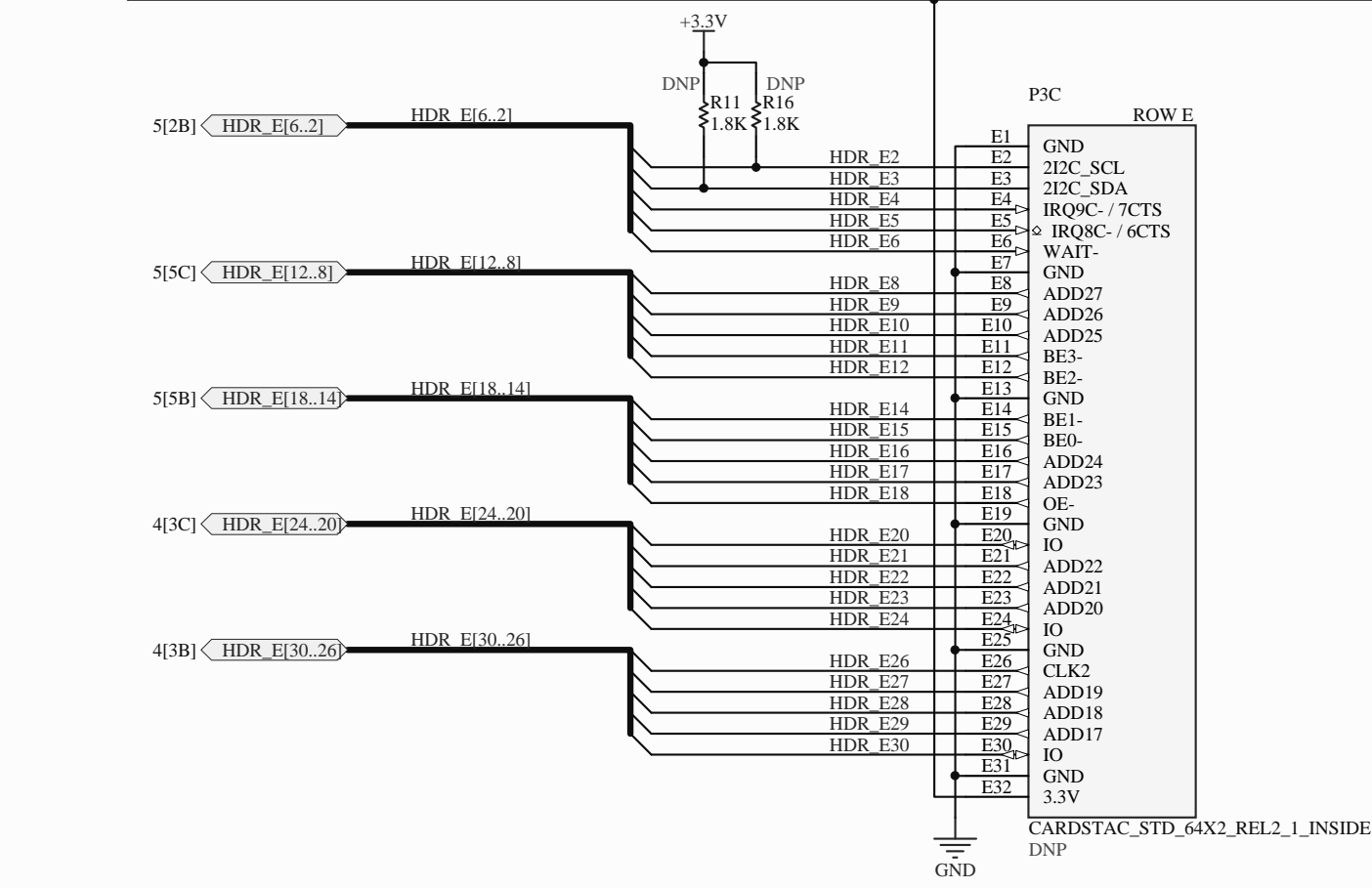
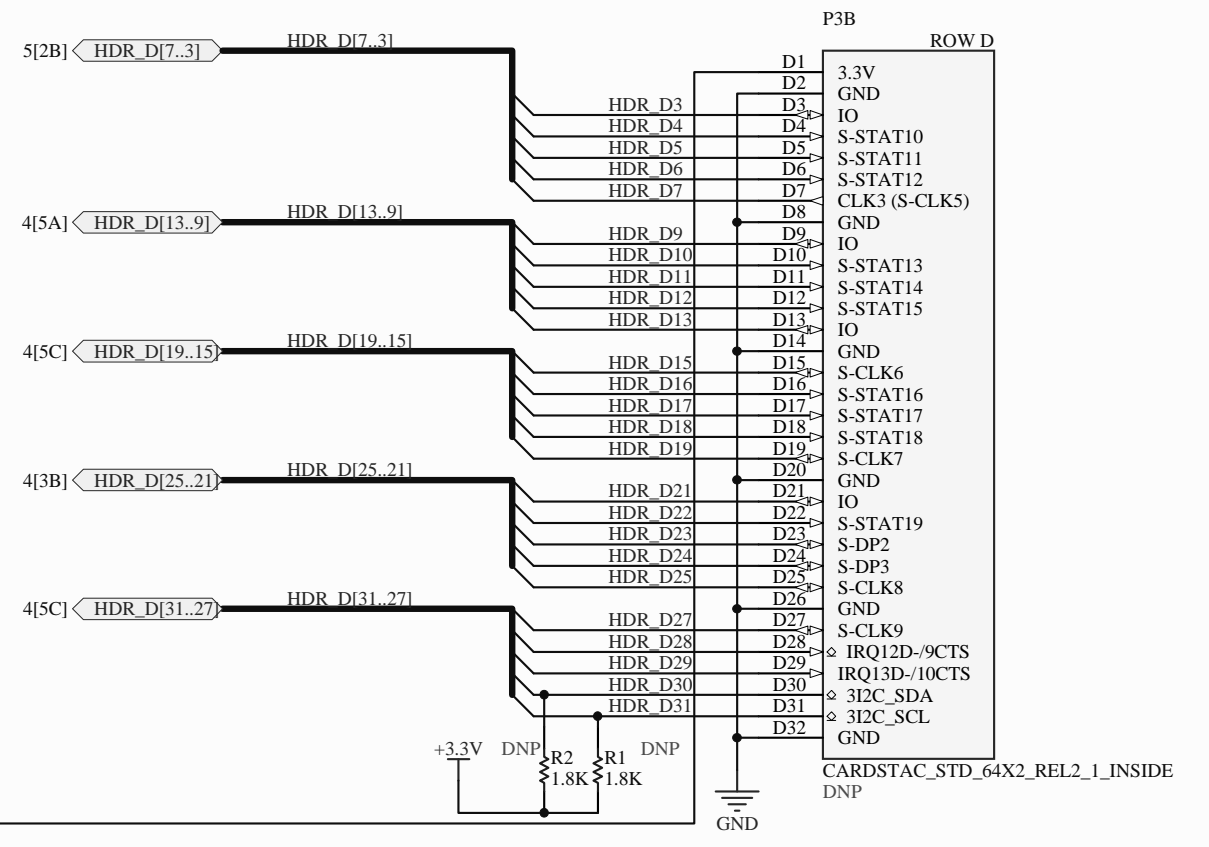
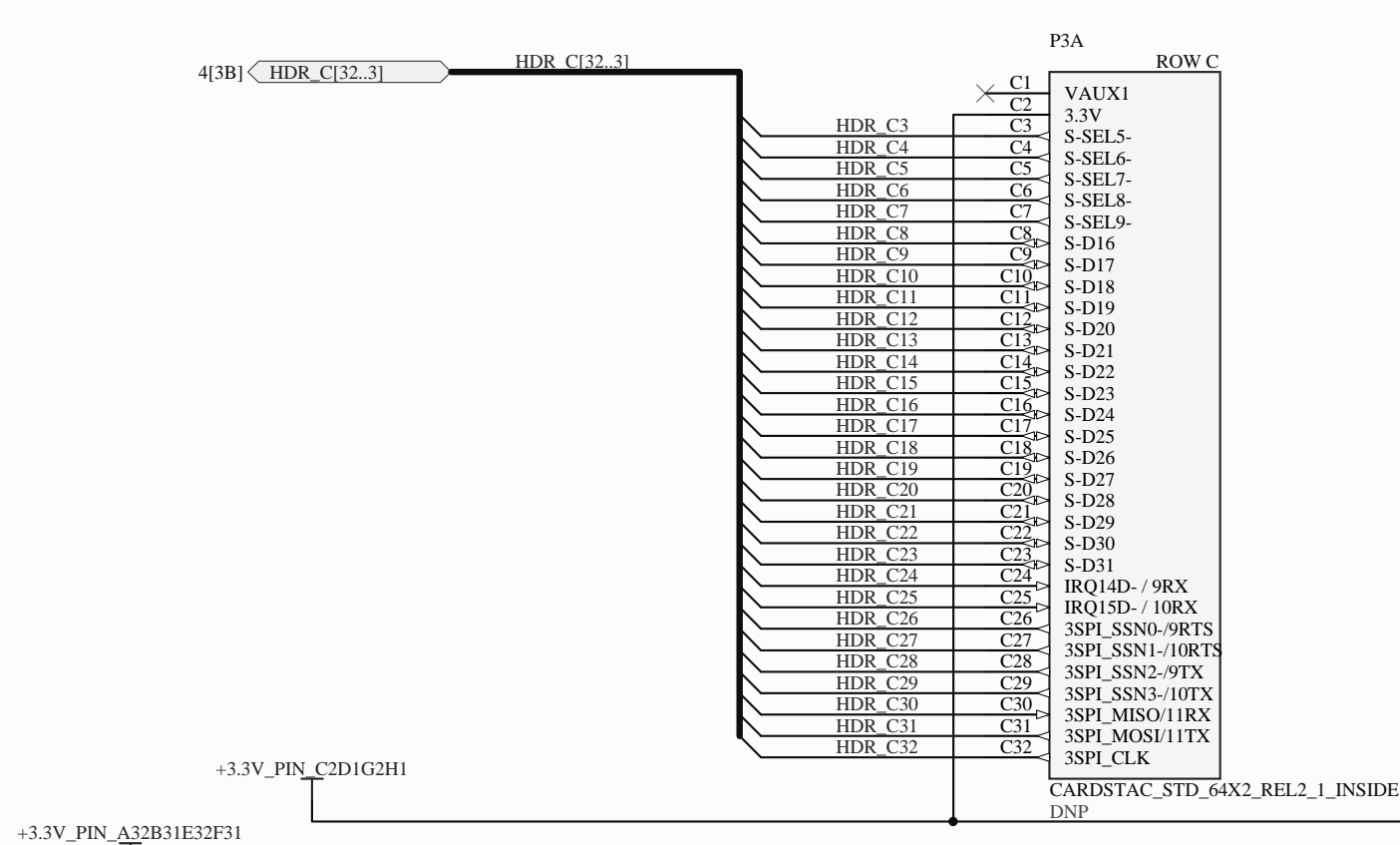
D

A

B

C

D

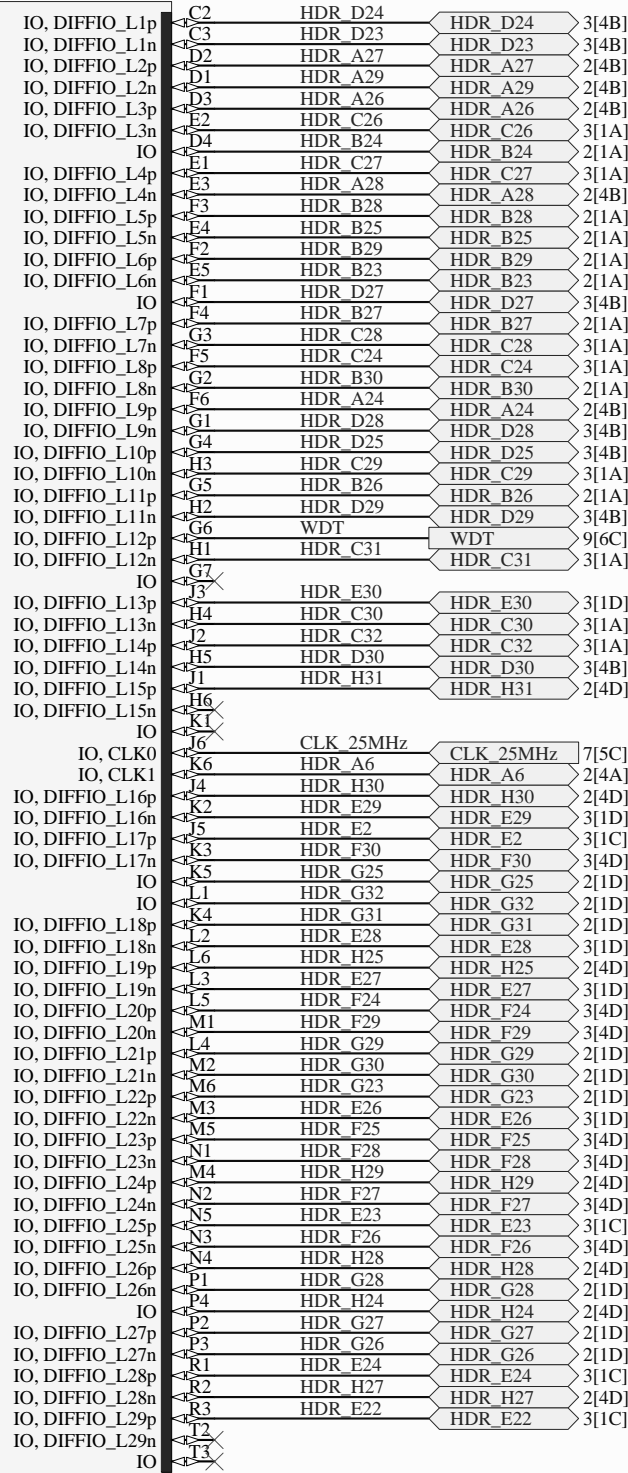


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Size: B	Number: CMC5001	Revision: A		
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U4A

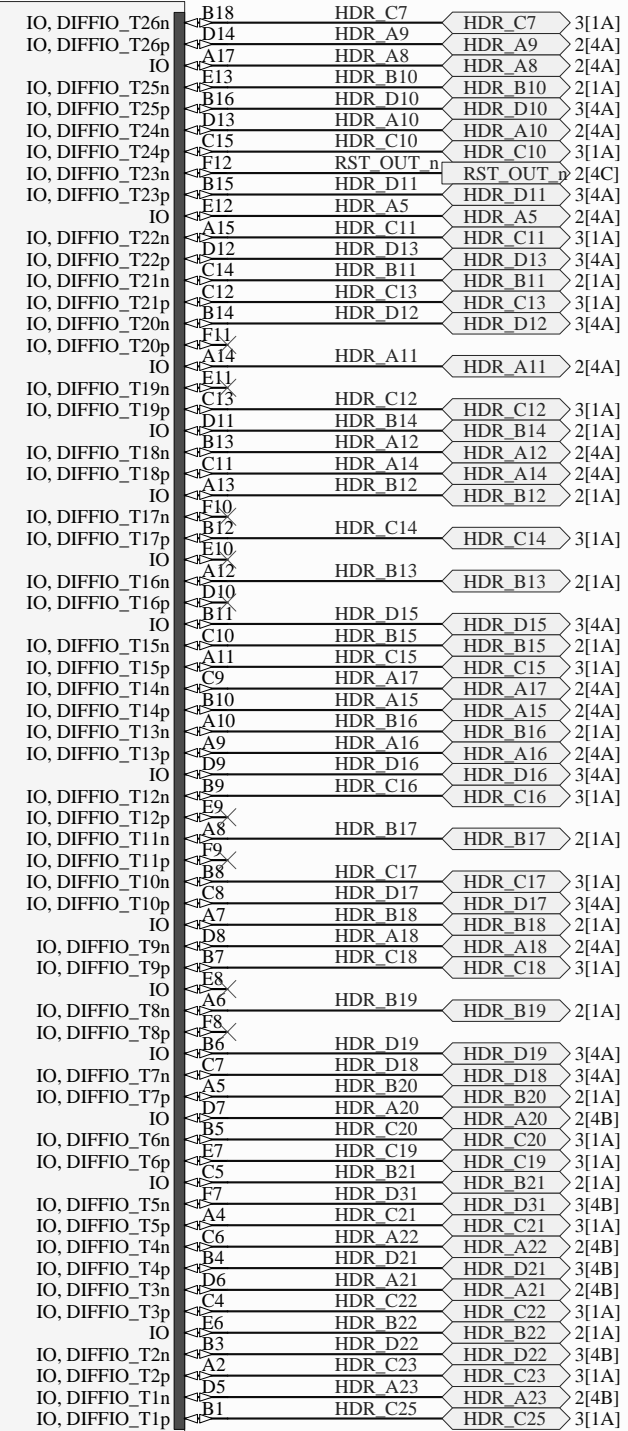
BANK 1



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BANK 2



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Date: 2/25/2012	Time: 4:25:32 PM	Sheet 4 of 9		
File: C:\dallas_logic\altium_dlc\Projects\CMC5001_REVA\4_CPLD1.SchDoc				

U4C

**BANK 3**

IO, DIFFIO_R32n	T17	EEPROM3_WP_N	EEPROM3_WP_N	7[1C]
IO, DIFFIO_R32p	R15	EEPROM3_CLK	EEPROM3_CLK	7[1C]
IO, DIFFIO_R31n	T16	EEPROM3_HOLD	EEPROM3_HOLD_N	7[1D]
IO, DIFFIO_R31p	R16	EEPROM3_SO	EEPROM3_SO	7[2C]
IO, DIFFIO_R30n	P15	EEPROM1_HOLD	EEPROM1_HOLD_N	7[1A]
IO, DIFFIO_R30p	R17	EEPROM3_CS_N	EEPROM3_CS_N	7[1C]
IO, DIFFIO_R29n	P14	LED_YEL	LED_YEL	8[1C]
IO, DIFFIO_R29p	R18	EEPROM3_SI	EEPROM3_SI	7[1C]
IO, DIFFIO_R28n	N15	SW1	SW1	8[4A]
IO, DIFFIO_R28p	P16	EEPROM1_WP_N	EEPROM1_WP_N	7[1A]
IO, DIFFIO_R27n	N14	LED_GRN	LED_GRN	8[1C]
IO, DIFFIO_R27p	P17	EEPROM1_SO	EEPROM1_SO	7[2A]
IO, DIFFIO_R26n	N13	TEMP_CLK	TEMP_CLK	8[4A]
IO, DIFFIO_R26p	P18	EEPROM1_CS_N	EEPROM1_CS_N	7[1A]
IO, DIFFIO_R25n	M15	EEPROM2_SO	EEPROM2_SO	7[2B]
IO, DIFFIO_R25p	N16	EEPROM2_CS_N	EEPROM2_CS_N	7[1B]
IO, DIFFIO_R24n	M14	EEPROM2_HOLD	EEPROM2_HOLD_N	7[1B]
IO, DIFFIO_R24p	N17	EEPROM1_CLK	EEPROM1_CLK	7[1A]
IO, DIFFIO_R23n	M13	TEMP_CSN	TEMP_CSN	8[4A]
IO, DIFFIO_R23p	N18	SW2	SW2	8[4B]
IO, DIFFIO_R22n	M12	LED_RED	LED_RED	8[1C]
IO, DIFFIO_R22p	M16	EEPROM2_CLK	EEPROM2_CLK	7[1B]
IO, DIFFIO_R21n	L16	SW3	SW3	8[4C]
IO, DIFFIO_R21p	M17	EEPROM2_WP_N	EEPROM2_WP_N	7[1B]
IO, DIFFIO_R20n	L15	EEPROM2_SI	EEPROM2_SI	7[1B]
IO, DIFFIO_R20p	M18	EEPROM1_SI	EEPROM1_SI	7[1A]
IO, DIFFIO_R19n	L14	TEMP_SIO	TEMP_SIO	8[4A]
IO, DIFFIO_R19p	L17	HDR_G4	HDR_G4	2[1D]
IO, DIFFIO_R18n	L13	HDR_E8	HDR_E8	3[1C]
IO, DIFFIO_R18p	L18	HDR_F4	HDR_F4	3[4D]
IO, DIFFIO_R17n	K16	HDR_F5	HDR_F5	3[4D]
IO, DIFFIO_R17p	K17	HDR_F3	HDR_F3	3[4D]
IO, DIFFIO_R16n	K15	HDR_E3	HDR_E3	3[1C]
IO, DIFFIO_R16p	K18	HDR_E5	HDR_E5	3[1C]
IO, DIFFIO_R15n	K14	HDR_F6	HDR_F6	3[4D]
IO, DIFFIO_R15p	K13	HDR_D7	HDR_D7	3[4A]
IO, DIFFIO_R14n	J13	HDR_E6	HDR_E6	3[1C]
IO, DIFFIO_R14p	J18	HDR_F1	HDR_F1	3[4D]
IO, DIFFIO_R13n	J14	HDR_G3	HDR_G3	2[1D]
IO, DIFFIO_R13p	J17	HDR_E4	HDR_E4	3[1C]
IO, DIFFIO_R12n	J15			
IO, DIFFIO_R12p	J18	HDR_F2	HDR_F2	3[4D]
IO, DIFFIO_R11n	J16			
IO, DIFFIO_R11p	J17	HDR_D3	HDR_D3	3[4A]
IO, DIFFIO_R10n	J13	HDR_D3	HDR_D3	3[4A]
IO, DIFFIO_R10p	J18	HDR_B1	HDR_B1	2[1A]
IO, DIFFIO_R9n	G17	HDR_C3	HDR_C3	3[1A]
IO, DIFFIO_R9p	H15	HDR_D5	HDR_D5	3[4A]
IO, DIFFIO_R8n	G16	HDR_C4	HDR_C4	3[1A]
IO, DIFFIO_R8p	H16	HDR_D4	HDR_D4	3[4A]
IO, DIFFIO_R7n	F18	HDR_B2	HDR_B2	2[1A]
IO, DIFFIO_R7p	G12	HDR_B3	HDR_B3	2[1A]
IO, DIFFIO_R6n	F17	HDR_B3	HDR_B3	2[1A]
IO, DIFFIO_R6p	G13			
IO, DIFFIO_R5n	F16	HDR_D6	HDR_D6	3[4A]
IO, DIFFIO_R5p	G14			
IO, DIFFIO_R4n	E18			
IO, DIFFIO_R4p	E15	HDR_B5	HDR_B5	2[1A]
IO, DIFFIO_R3n	E17	HDR_C5	HDR_C5	3[1A]
IO, DIFFIO_R3p	F13	HDR_A2	HDR_A2	2[4A]
IO, DIFFIO_R2n	D18	HDR_B4	HDR_B4	2[1A]
IO, DIFFIO_R2p	F14	HDR_D9	HDR_D9	3[4A]
IO, DIFFIO_R1n	E16	HDR_C6	HDR_C6	3[1A]
IO, DIFFIO_R1p	F15	HDR_B9	HDR_B9	2[1A]
	D17	HDR_B6	HDR_B6	2[1A]
	E14	HDR_A3	HDR_A3	2[4A]
	D16	HDR_C8	HDR_C8	3[1A]
	C16	HDR_B8	HDR_B8	2[1A]
	E15	HDR_A4	HDR_A4	2[4A]
	C17	HDR_B7	HDR_B7	2[1A]
	D15	HDR_C9	HDR_C9	3[1A]

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U4D

**BANK 4**

IO, DIFFIO_B1p	U1	HDR_G24	HDR_G24	2[1D]
IO, DIFFIO_B1n	V2	HDR_E21	HDR_E21	3[1C]
IO, DIFFIO_B2p	R5	HDR_F22	HDR_F22	3[4D]
IO, DIFFIO_B2n	U3	HDR_H23	HDR_H23	2[4D]
IO, DIFFIO_B3p	P6	HDR_F21	HDR_F21	3[4D]
IO, DIFFIO_B3n	T4	HDR_G22	HDR_G22	2[1D]
IO, DIFFIO_B4p	R6	HDR_G21	HDR_G21	2[1D]
IO, DIFFIO_B4n	U4	HDR_E20	HDR_E20	3[1C]
IO, DIFFIO_B5p	T6	HDR_F19	HDR_F19	3[4D]
IO, DIFFIO_B5n	V4	HDR_H22	HDR_H22	2[4D]
IO, DIFFIO_B6p	N7	HDR_F23	HDR_F23	3[4D]
IO, DIFFIO_B6n	T5	HDR_H21	HDR_H21	2[4D]
IO, DIFFIO_B7p	F7	HDR_H19	HDR_H19	2[4C]
IO, DIFFIO_B7n	U5	HDR_F20	HDR_F20	3[4D]
IO, DIFFIO_B8p	R7	HDR_F18	HDR_F18	3[4D]
IO, DIFFIO_B8n	V5	HDR_G20	HDR_G20	2[1D]
IO, DIFFIO_B9p	T7	HDR_G18	HDR_G18	2[1D]
IO, DIFFIO_B9n	U6	HDR_G19	HDR_G19	2[1D]
IO, DIFFIO_B10p	P8	HDR_E17	HDR_E17	3[1C]
IO, DIFFIO_B10n	T7	HDR_H18	HDR_H18	2[4C]
IO, DIFFIO_B11p	R8	HDR_F17	HDR_F17	3[4D]
IO, DIFFIO_B11n	T8	HDR_H16	HDR_H16	2[4C]
IO, DIFFIO_B12p	U8	HDR_G17	HDR_G17	2[1D]
IO, DIFFIO_B12n	V8	HDR_H17	HDR_H17	2[4C]
IO, DIFFIO_B13p	R9	HDR_G15	HDR_G15	2[1D]
IO, DIFFIO_B13n	U9	HDR_E16	HDR_E16	3[1C]
IO, DIFFIO_B14p	V9	HDR_H15	HDR_H15	2[4C]
IO, DIFFIO_B14n	U10	HDR_E15	HDR_E15	3[1C]
IO, DIFFIO_B15p	V10	HDR_F15	HDR_F15	3[4D]
IO, DIFFIO_B15n	P10	HDR_H11	HDR_H11	2[4C]
IO, DEV_OE, DIFFIO_B16p	U11	HDR_H12	HDR_H12	2[4C]
IO, DEV_OE, DIFFIO_B16n	N9	HDR_E14	HDR_E14	3[1C]
IO, DIFFIO_B17p	V10	CPLD_RST_n	CPLD_RST_n	9[6C]
IO, DIFFIO_B17n	R10	HDR_H13	HDR_H13	2[4C]
IO, DIFFIO_B18p	V11	HDR_F14	HDR_F14	3[4D]
IO, DIFFIO_B18n	T10	HDR_G14	HDR_G14	2[1D]
IO, DIFFIO_B19p	U12	HDR_F12	HDR_F12	3[4D]
IO, DIFFIO_B19n	N11	HDR_E9	HDR_E9	3[1C]
IO, DIFFIO_B20p	V12	HDR_F13	HDR_F13	3[4D]
IO, DIFFIO_B20n	P11	HDR_G8	HDR_G8	2[1D]
IO, DIFFIO_B21p	U13	HDR_E12	HDR_E12	3[1C]
IO, DIFFIO_B21n	R11	HDR_G9	HDR_G9	2[1D]
IO, DIFFIO_B22p	V13	HDR_G11	HDR_G11	2[1D]
IO, DIFFIO_B22n	T11	HDR_G12	HDR_G12	2[1D]
IO, DIFFIO_B23p	T14	HDR_E10	HDR_E10	3[1C]
IO, DIFFIO_B23n	N12	HDR_G5	HDR_G5	2[1D]
IO, DIFFIO_B24p	U14	HDR_G10	HDR_G10	2[1D]
IO, DIFFIO_B24n	P12	HDR_F10	HDR_F10	3[4D]
IO, DIFFIO_B25p	V14	HDR_F11	HDR_F11	3[4D]
IO, DIFFIO_B25n	R12	HDR_H7	HDR_H7	2[4C]
IO, DIFFIO_B26p	T15	HDR_H5	HDR_H5	2[4C]
IO, DIFFIO_B26n	T12	HDR_H10	HDR_H10	2[4C]
IO, DIFFIO_B27p	U15	HDR_F9	HDR_F9	3[4D]
IO, DIFFIO_B27n	P13	HDR_F7	HDR_F7	3[4D]
IO, DIFFIO_B28p	V15	HDR_H9	HDR_H9	2[4C]
IO, DIFFIO_B28n	R13	HDR_H6	HDR_H6	2[4C]
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IO, DIFFIO_B29n	T13	HDR_E11	HDR_E11	3[1C]
IO, DIFFIO_B30p	V17	HDR_G7	HDR_G7	2[1D]
IO, DIFFIO_B30n	U18	HDR_H4	HDR_H4	2[4C]
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IO, DIFFIO_B31n				

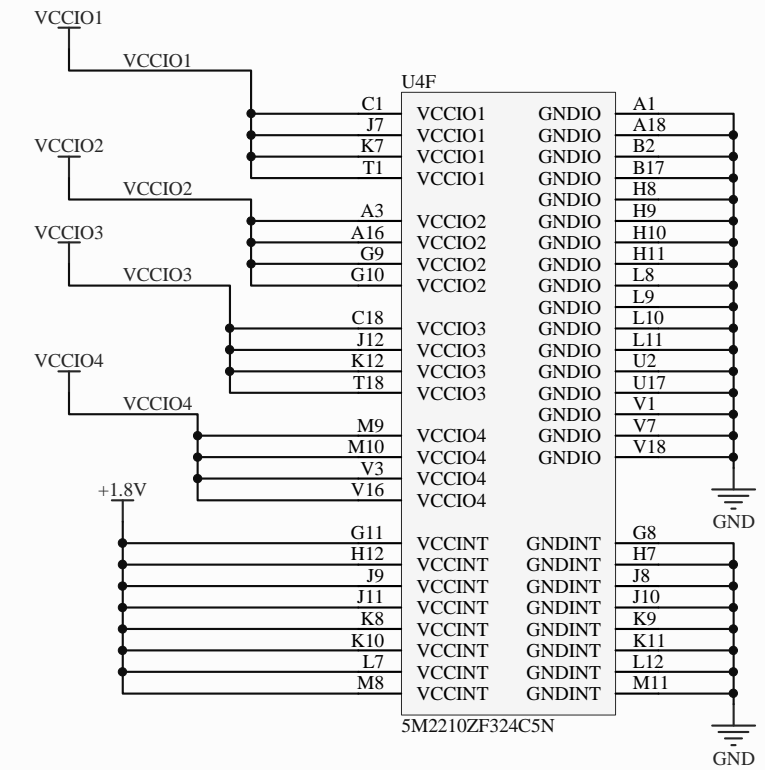
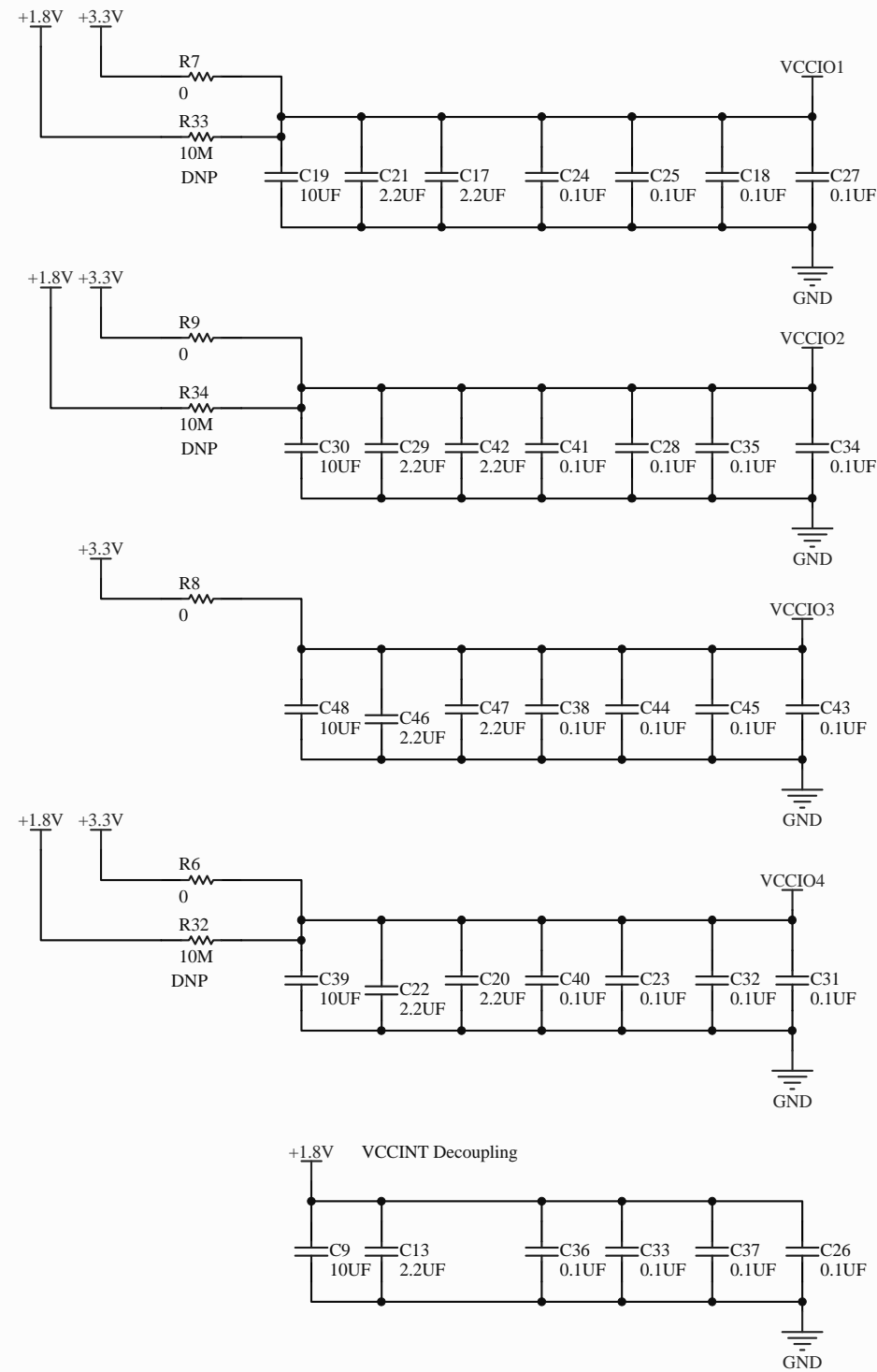
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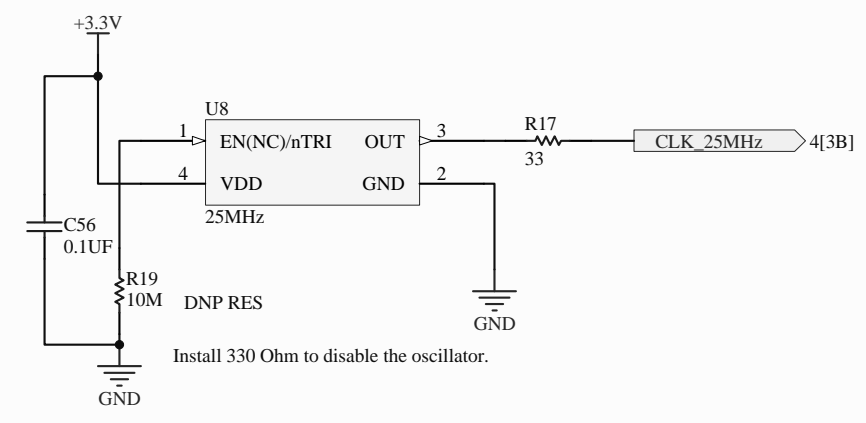
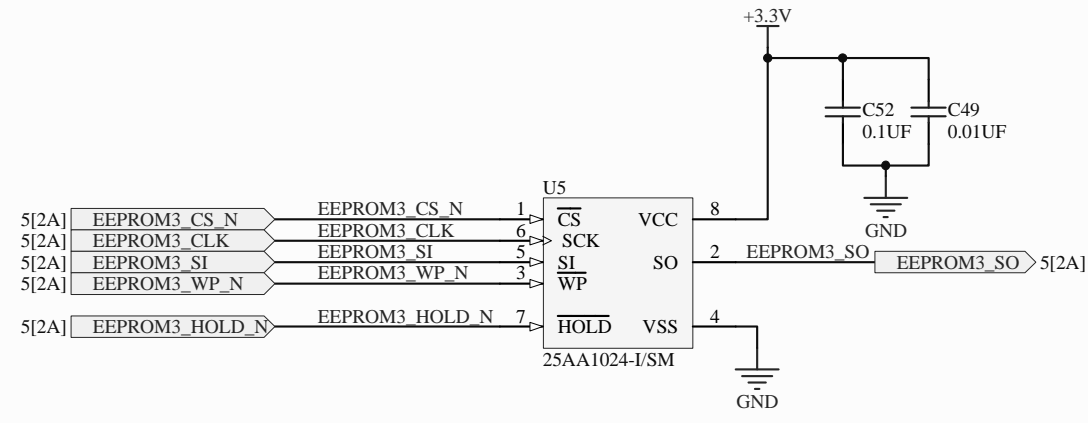
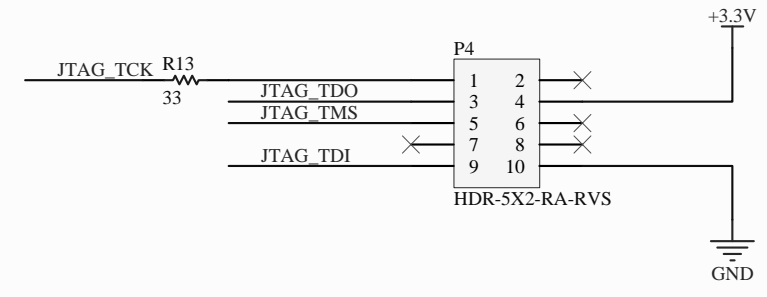
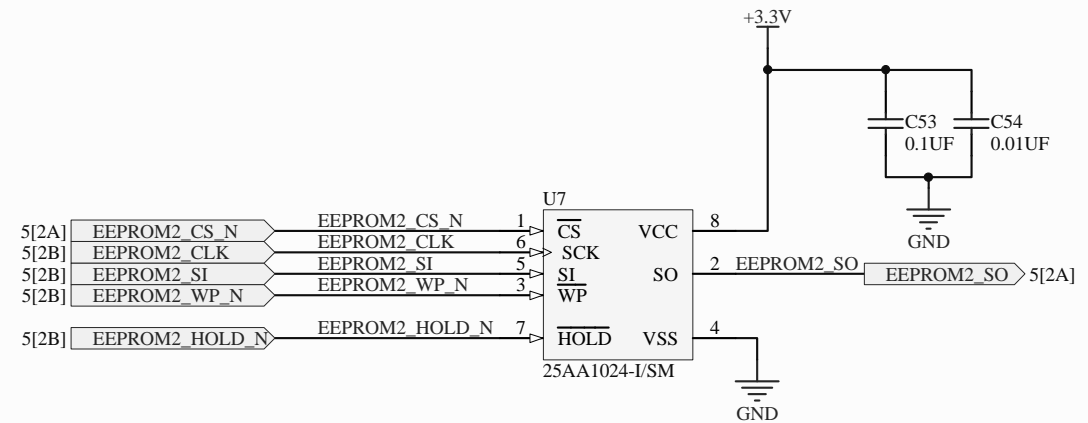
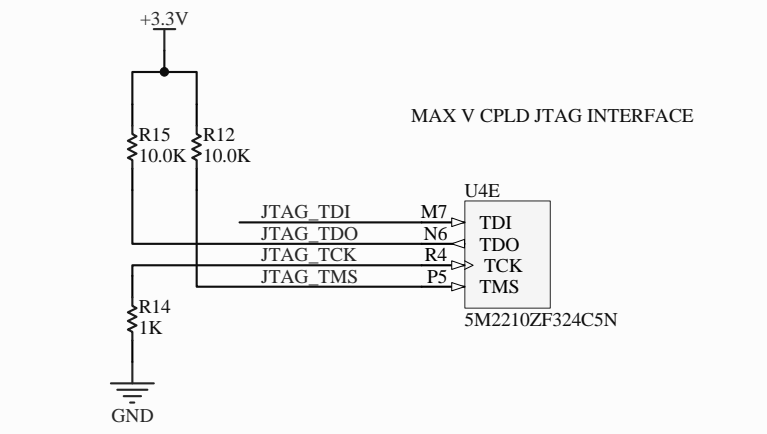
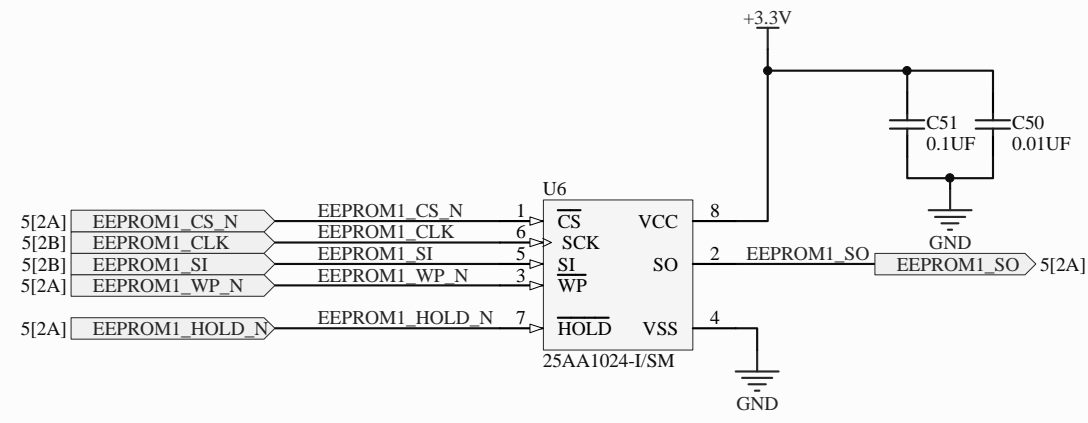
Default power configuration is 3.3V IO.

Remove top-side resistor and install bottom side resistor to support 1.8V IO.



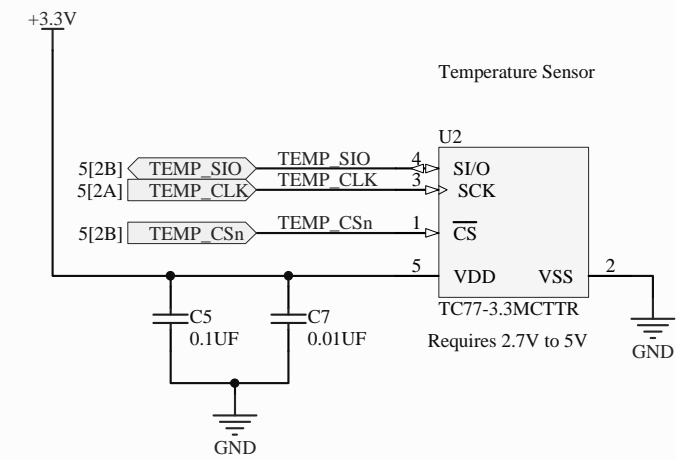
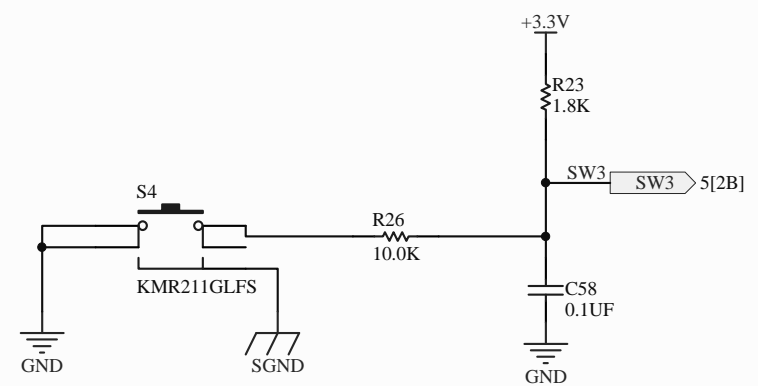
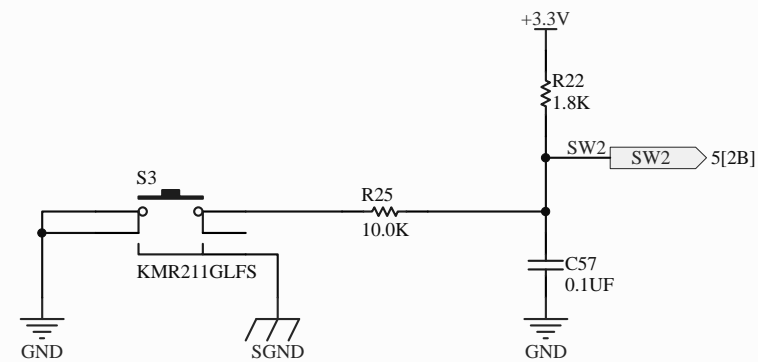
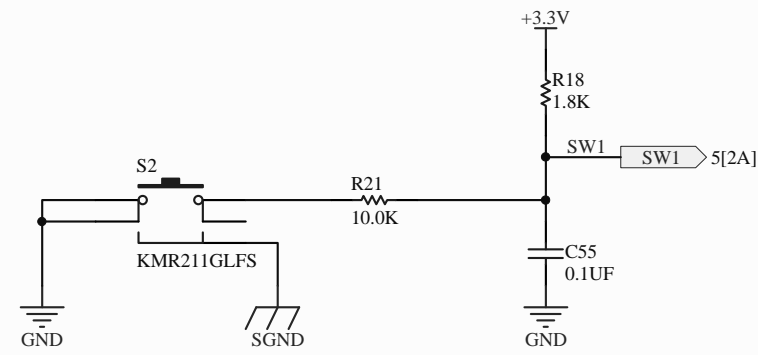
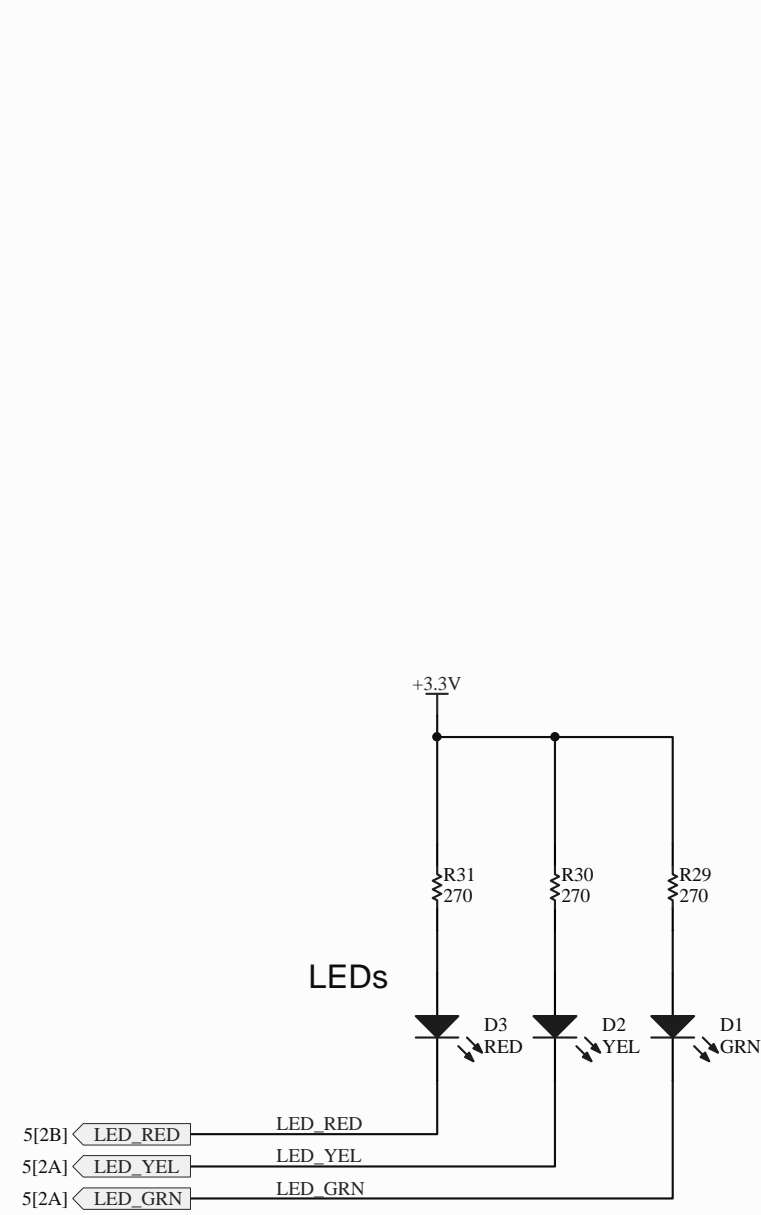
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Size: B	Number: CMC5001	Revision: A		
Date: 2/25/2012	Time: 4:25:33 PM	Sheet 6 of 9		
File: C:\dallas_logic\altium_dlc\Projects\CMC5001_REVA\6_CPLD_PWR.SchDoc				



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Size: B	Number: CMC5001	Revision: A		
Date: 2/25/2012	Time: 4:25:33 PM	Sheet 7 of 9		
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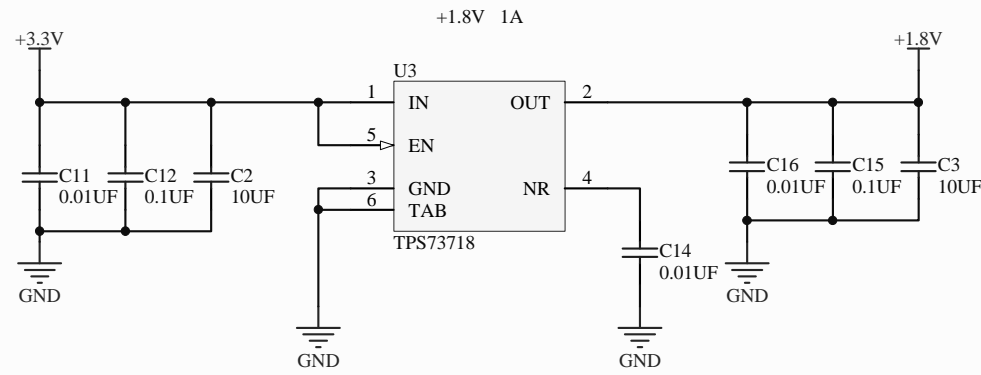


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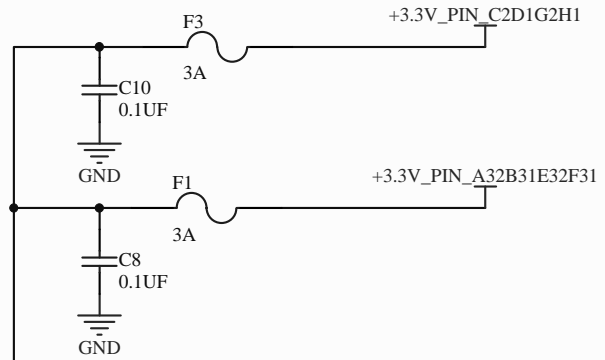
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Date: 2/25/2012	Time: 4:25:33 PM	Sheet 8 of 9	
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# POWER SUPPLY

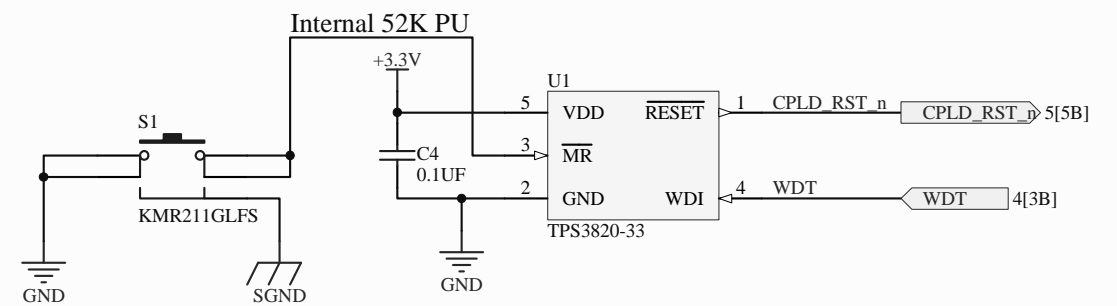
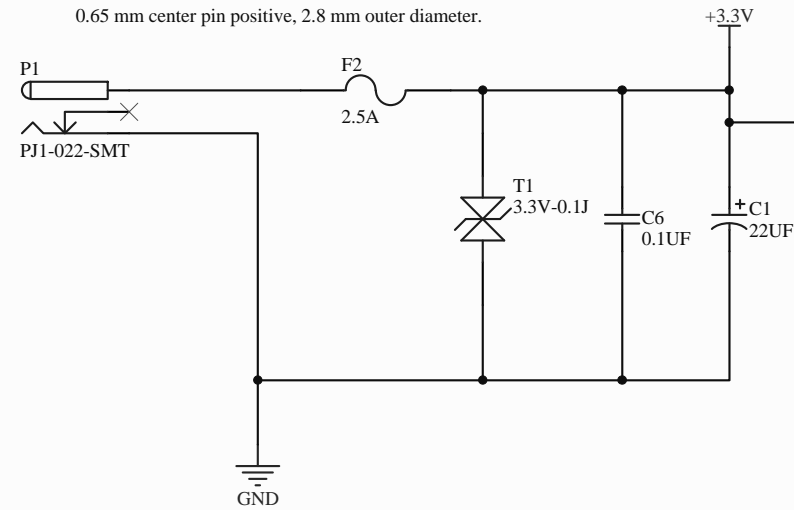


Remove fuses if other card in stack sources 3.3V power rail and local DCJACK is attached and powered (should not do this).  
CMC5001 may also pull current in from 3.3V pin (local power from external source via header pins).

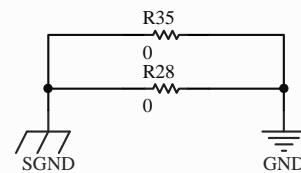


Design limit per set of four pins is 3A. DC Jack fuse will blow before these will.

DC JACK  
INPUT: +3.3V, 2.5A Max.  
0.65 mm center pin positive, 2.8 mm outer diameter.



SGND (Shield GND or guard ring) connected to ground power pins at two corners of module.



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File: C:\dallas_logic\altium_dlc\Projects\CMC5001_REVA\9_PS.SchDoc				