Design Notes

1) CMC5001 is configured as a Cardstac master card.
2) CPLD Bank 3 is fixed 3.3V I/O
3) Dev OE pin is used as IO, not as reset
4) RST_OUT_n is reset signal from CPLD
5) CPLD_RST_n is the CPLD reset from Power Supply

FID1 FID2 FID3 FID4 LOGO1

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REVISION TABLE

02-25-12	A	ET	Initial release of the schematic.

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File: C:\dallas_logic\altium_dlc\Projects\CMC5001_REVA\1_TOC.SchDoc			

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Title: ***Cardstac Cntlr., Dual Row, Altera MAX V***		Dallas Logic Corporation 801 E. Plano Parkway Suite 158 Plano TX 75074 USA
Size: B	Number: CMC5001	Revision: A
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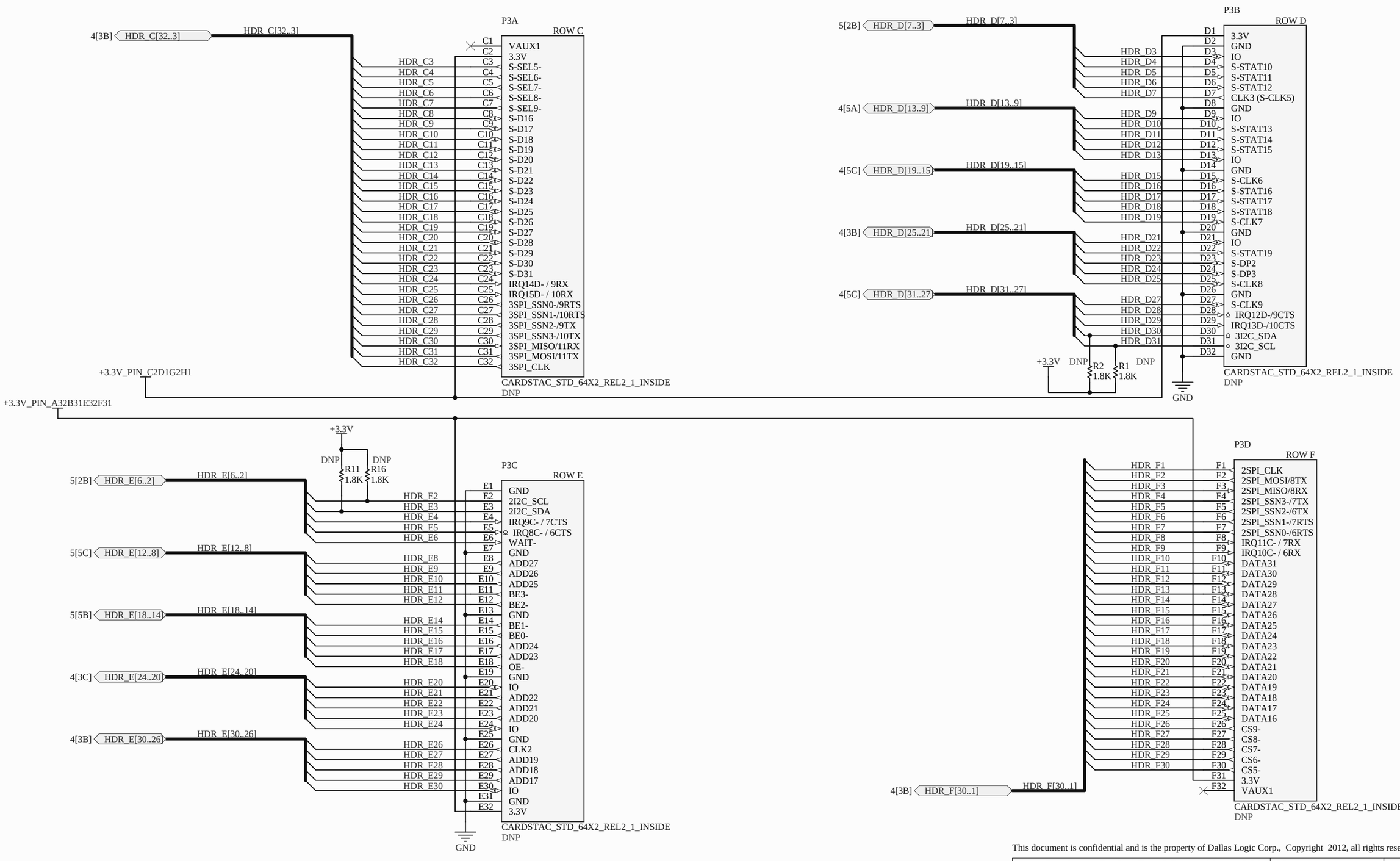

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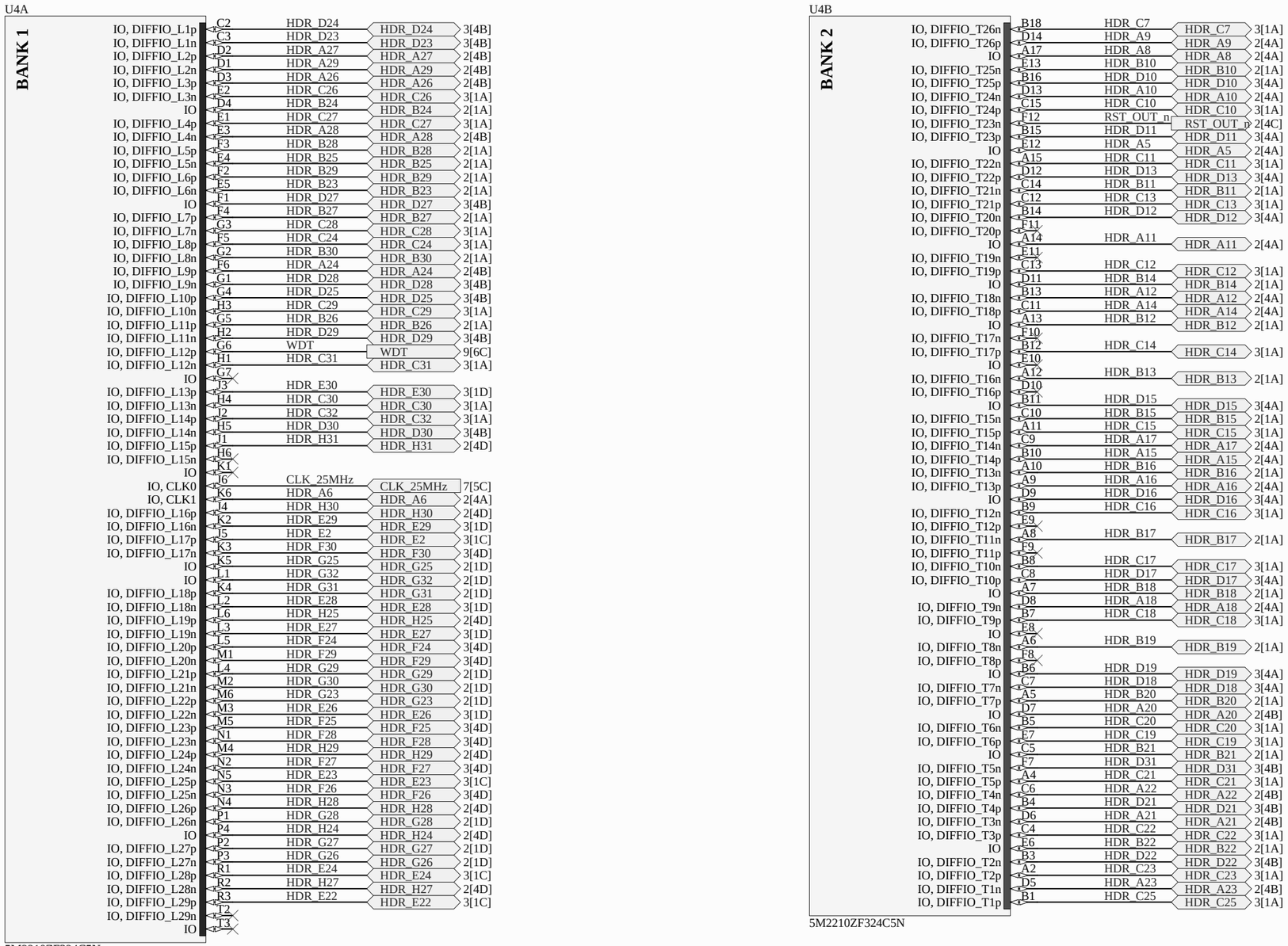

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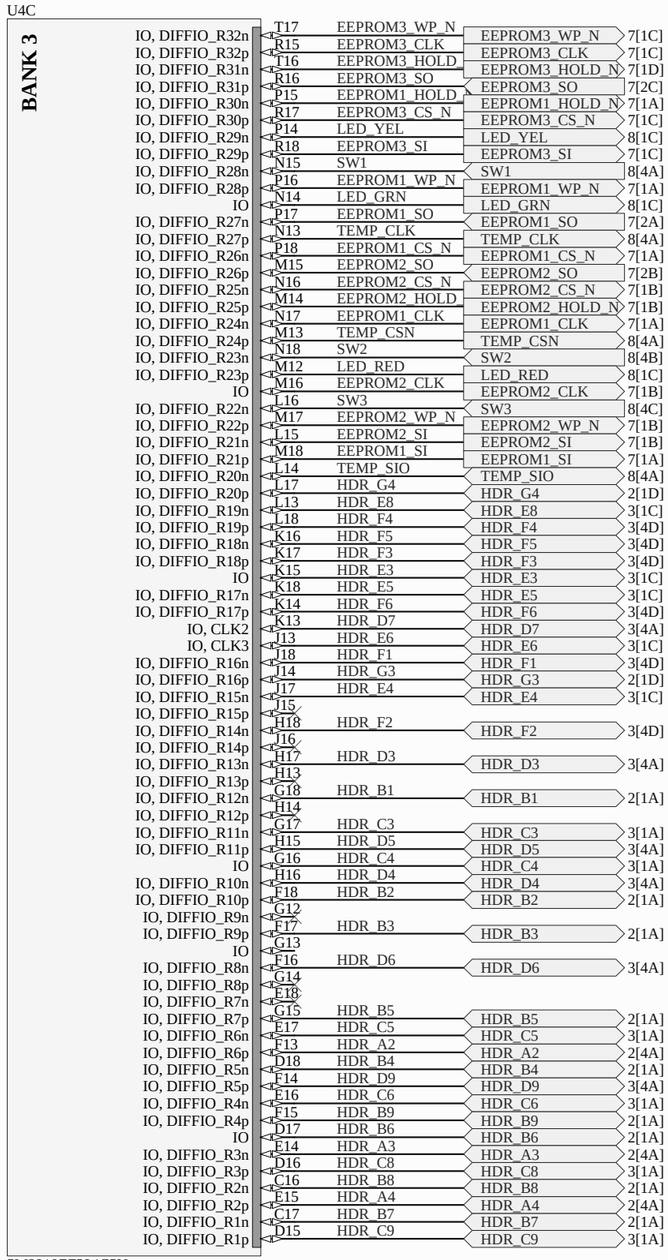

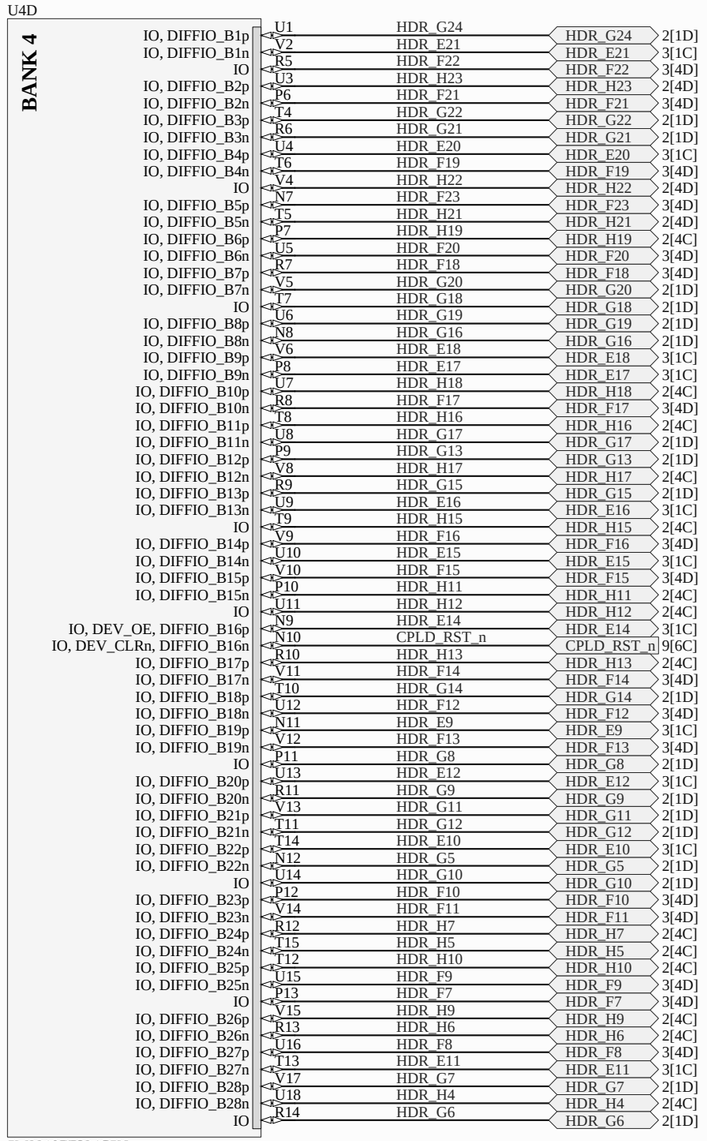

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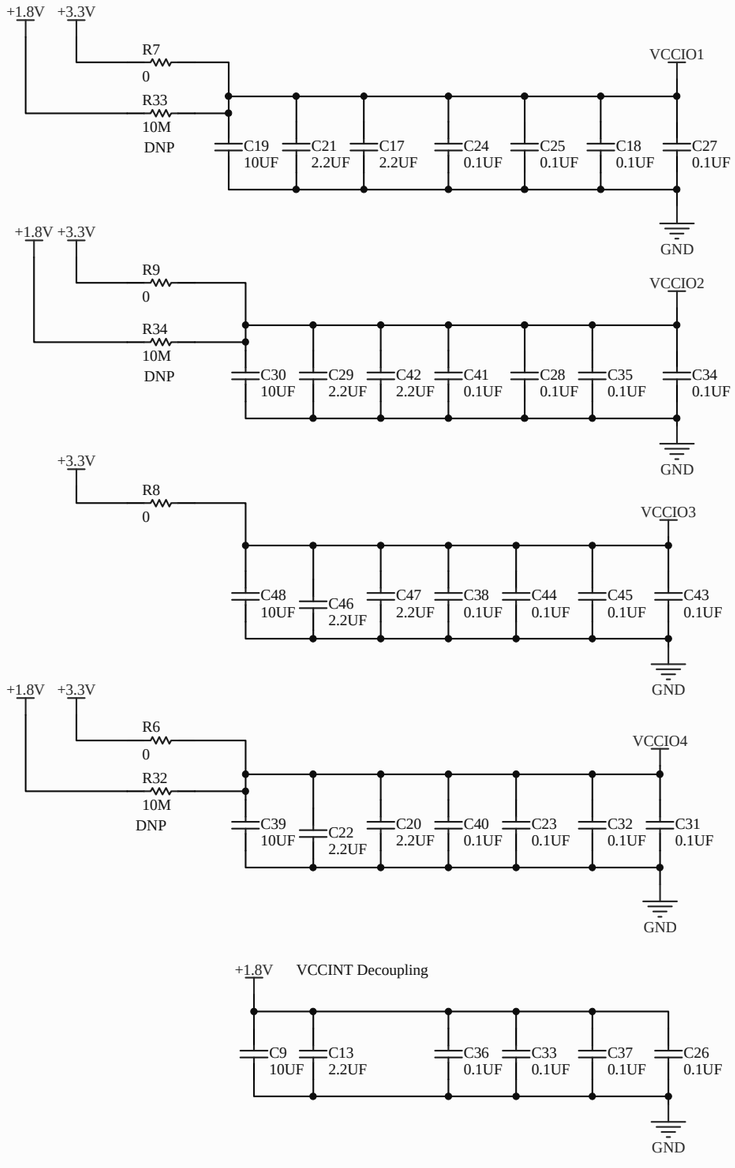
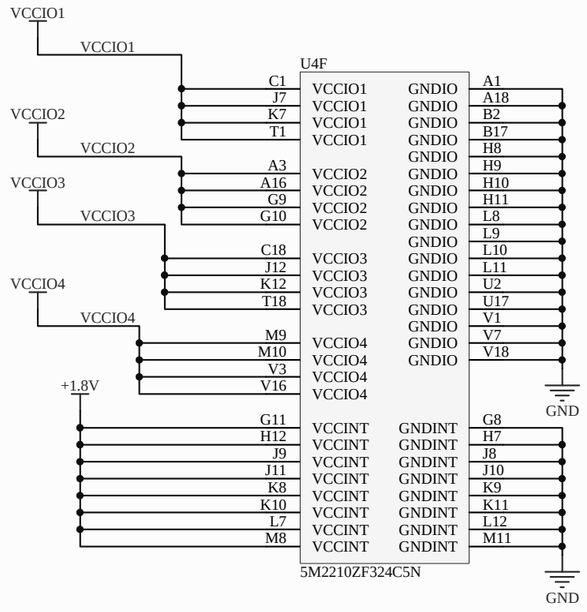
Default power configuration is 3.3V IO.

Remove top-side resistor and install bottom side resistor to support 1.8V IO.





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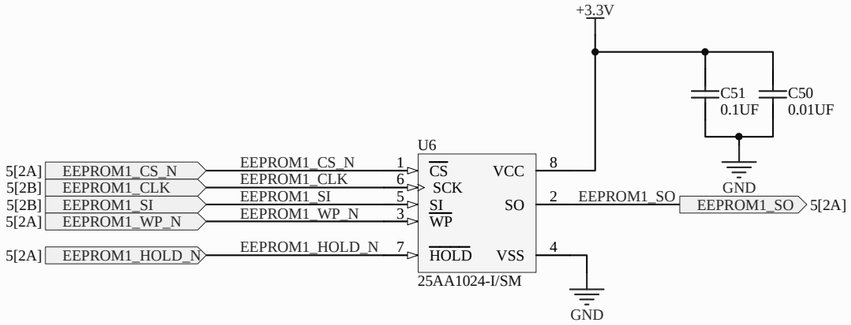

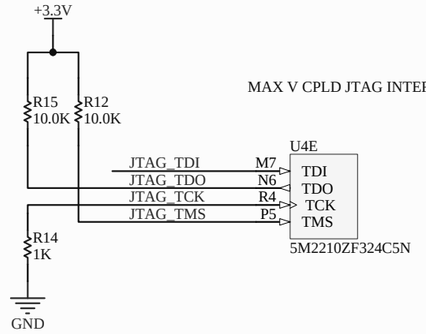

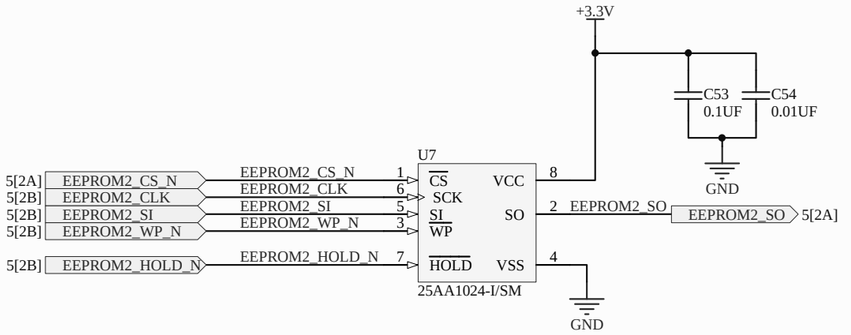

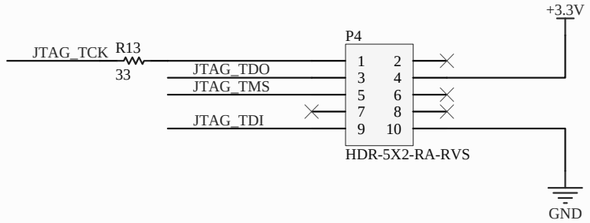

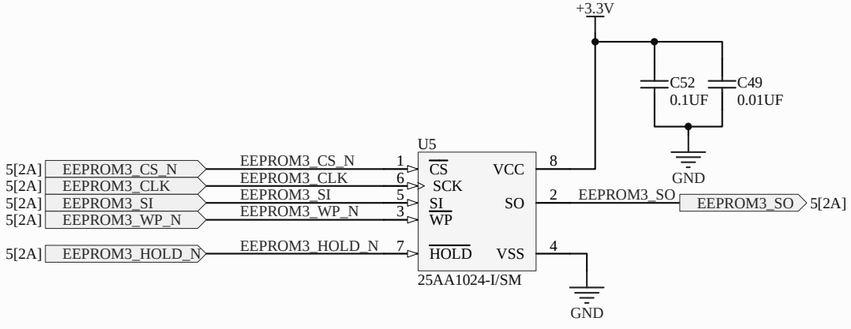

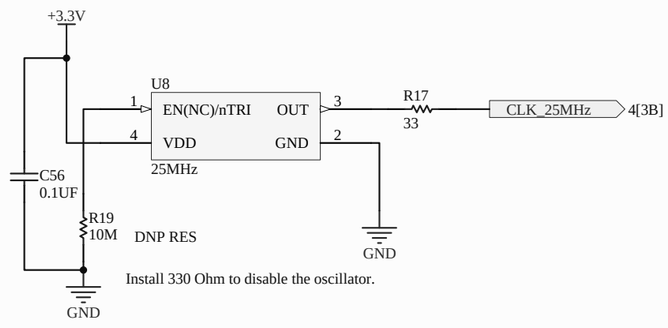

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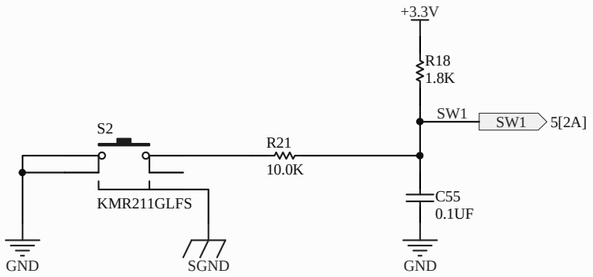

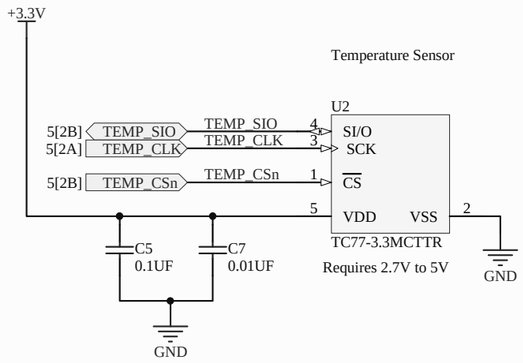

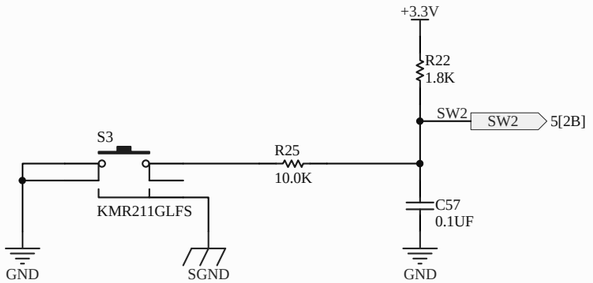

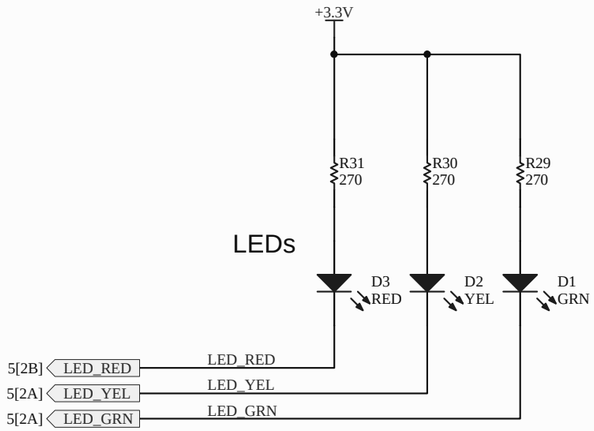

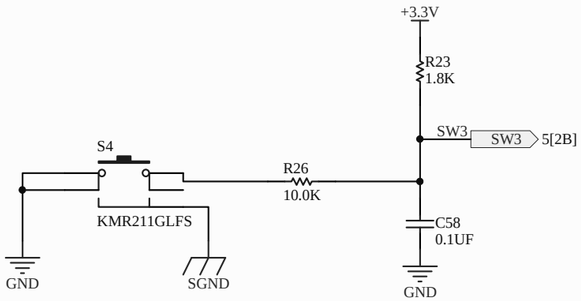

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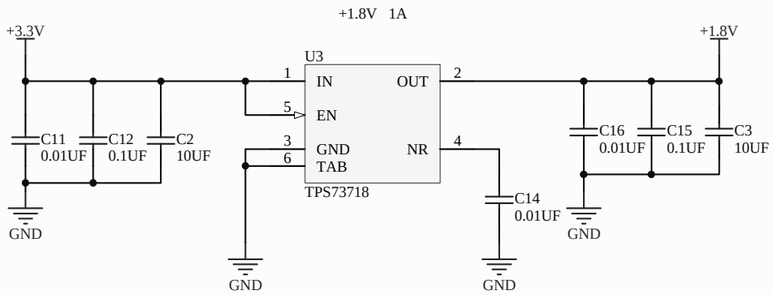
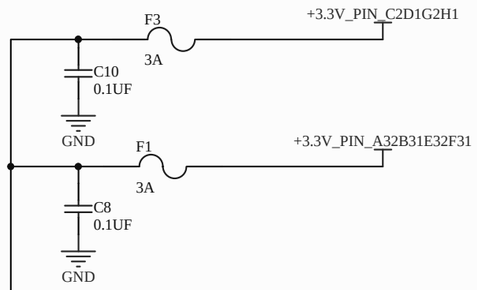
POWER SUPPLY



Remove fuses if other card in stack sources 3.3V power rail and local DCJACK is attached and powered (should not do this).
CMC5001 may also pull current in from 3.3V pin (local power from external source via header pins).

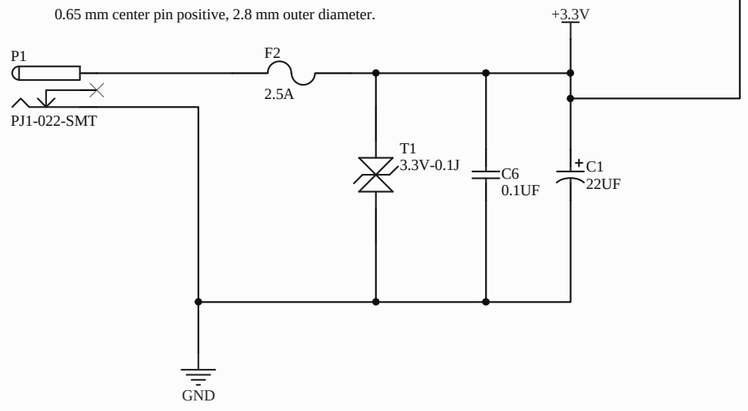


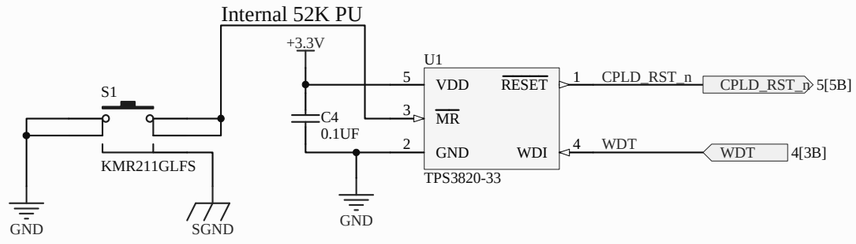
Design limit per set of four pins is 3A. DC Jack fuse will blow before these will.

DC JACK

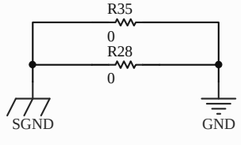
INPUT: +3.3V, 2.5A Max.

0.65 mm center pin positive, 2.8 mm outer diameter.





SGND (Shield GND or guard ring) connected to ground power pins at two corners of module.



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