REV.	DATE	NOTES	BY	APPROVED
X1	04-10-06	First draft release.	E.T.	
A	05-19-06	First manufacturing release.	E.T.	
B	10-23-06	Move of JTAG/ASMI connectors for more space.	E.T.	

DESIGN NOTES

1) Cyclone FPGA ports have no ESD or buffer protection. Use ESD precautions when handling Niomite PCB assembly.

2) Design provides for extra VCCINT/GND pin requirements of EP2C8 FPGA (can populate with C5 or C8 FPGA).

- For C5 FPGA devices, IO pins 26, 27, 80, 81 are dedicated to C8 Power connections and are not available.

3) Cardstac connector IO pins A11, A12, A14, A15, B13, B14, B15 are input only on the FPGA device.

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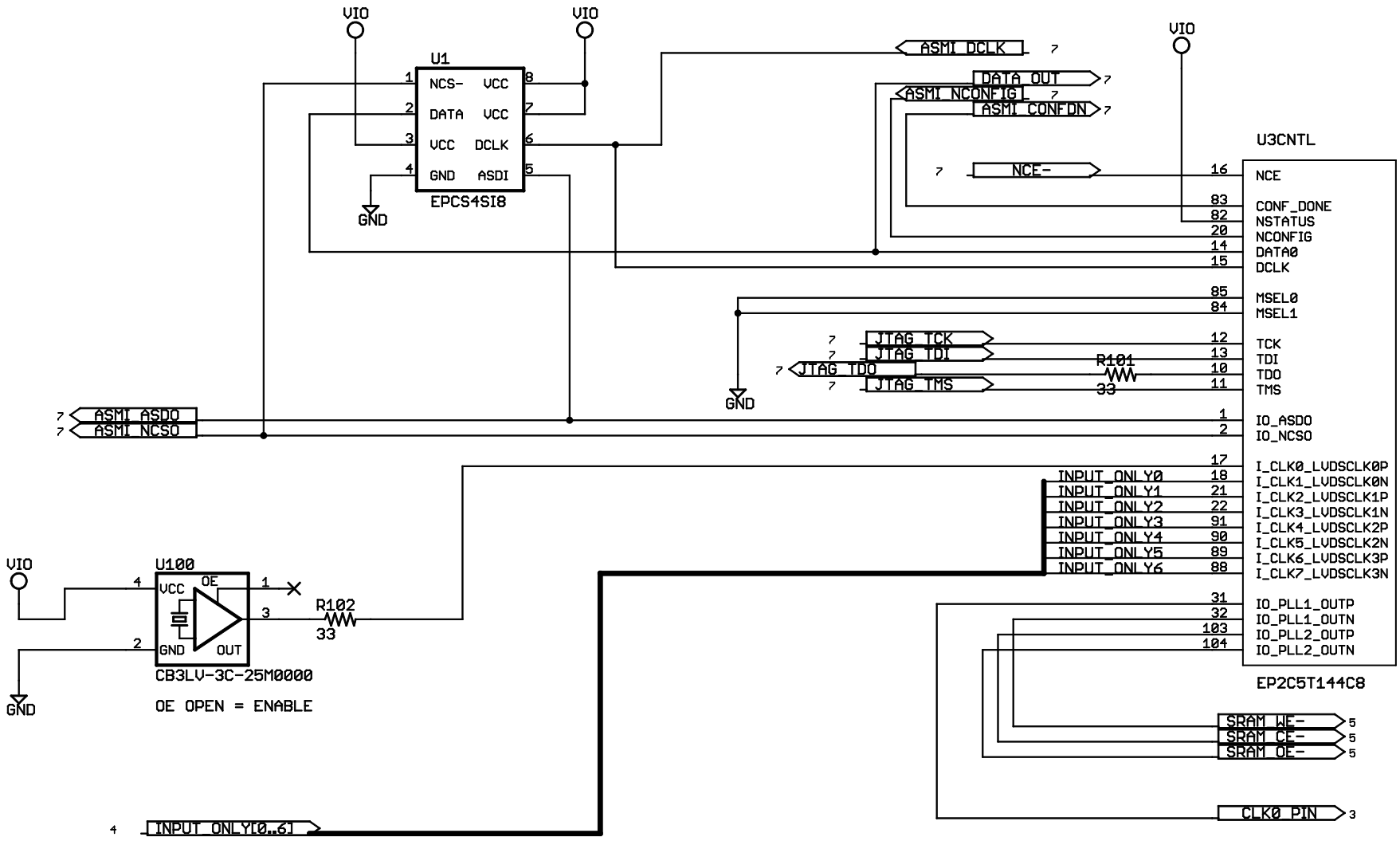

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FPGA CONTROL, EPCS LOADER, CLOCKS

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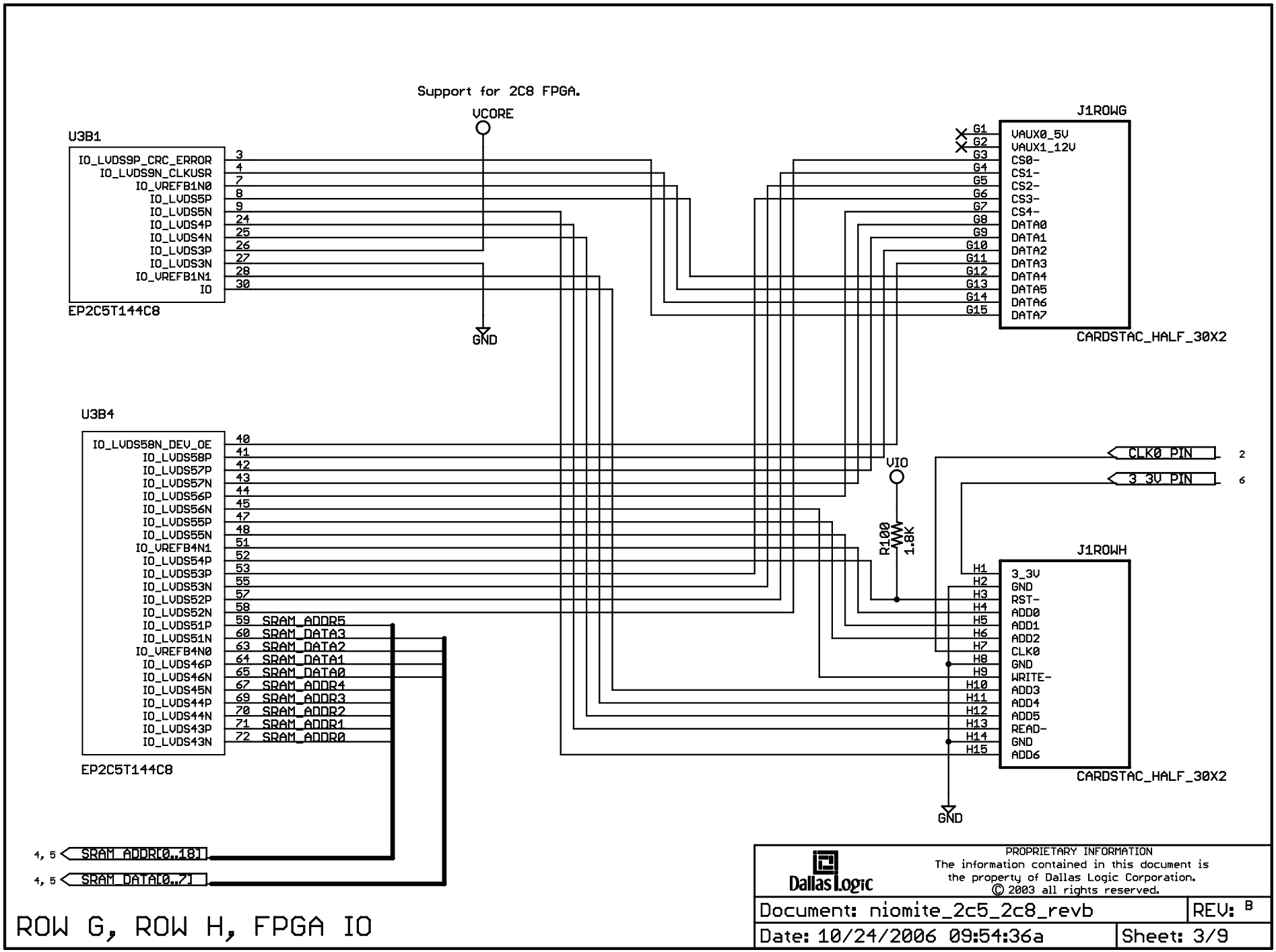
Support for 2C8 FPGA.
VCORE
U3B1
IO_LVDS9P_CRC_ERROR 3
IO_LVDS9N_CLKUSR 4
IO_VREFB1N0 7
IO_LVDS5P 8
IO_LVDS5N 9
IO_LVDS4P 24
IO_LVDS4N 25
IO_LVDS3P 26
IO_LVDS3N 27
IO_VREFB1N1 28
IO 30
EP2C5T144C8
GND
J1ROWG
G1 VAUX0_5V
G2 VAUX1_12V
G3 CS0-
G4 CS1-
G5 CS2-
G6 CS3-
G7 CS4-
G8 DATA0
G9 DATA1
G10 DATA2
G11 DATA3
G12 DATA4
G13 DATA5
G14 DATA6
G15 DATA7
CARDSTAC_HALF_30X2
U3B4
IO_LVDS58N_DEV_OE 40
IO_LVDS58P 41
IO_LVDS57P 42
IO_LVDS57N 43
IO_LVDS56P 44
IO_LVDS56N 45
IO_LVDS55P 47
IO_LVDS55N 48
IO_VREFB4N1 51
IO_LVDS54P 52
IO_LVDS53P 53
IO_LVDS53N 55
IO_LVDS52P 57
IO_LVDS52N 58
IO_LVDS51P 59 SRAM_ADDR5
IO_LVDS51N 60 SRAM_DATA3
IO_VREFB4N0 63 SRAM_DATA2
IO_LVDS46P 64 SRAM_DATA1
IO_LVDS46N 65 SRAM_DATA0
IO_LVDS45N 67 SRAM_ADDR4
IO_LVDS44P 69 SRAM_ADDR3
IO_LVDS44N 70 SRAM_ADDR2
IO_LVDS43P 71 SRAM_ADDR1
IO_LVDS43N 72 SRAM_ADDR0
EP2C5T144C8
VIO
R100 1.8K
CLK0 PIN 2
3_3V PIN 6
J1ROWH
H1 3_3V
H2 GND
H3 RST-
H4 ADD0
H5 ADD1
H6 ADD2
H7 CLK0
H8 GND
H9 WRITE-
H10 ADD3
H11 ADD4
H12 ADD5
H13 READ-
H14 GND
H15 ADD6
CARDSTAC_HALF_30X2
GND
4, 5 SRAM_ADDR[0..18]
4, 5 SRAM_DATA[0..7]
ROW G, ROW H, FPGA IO
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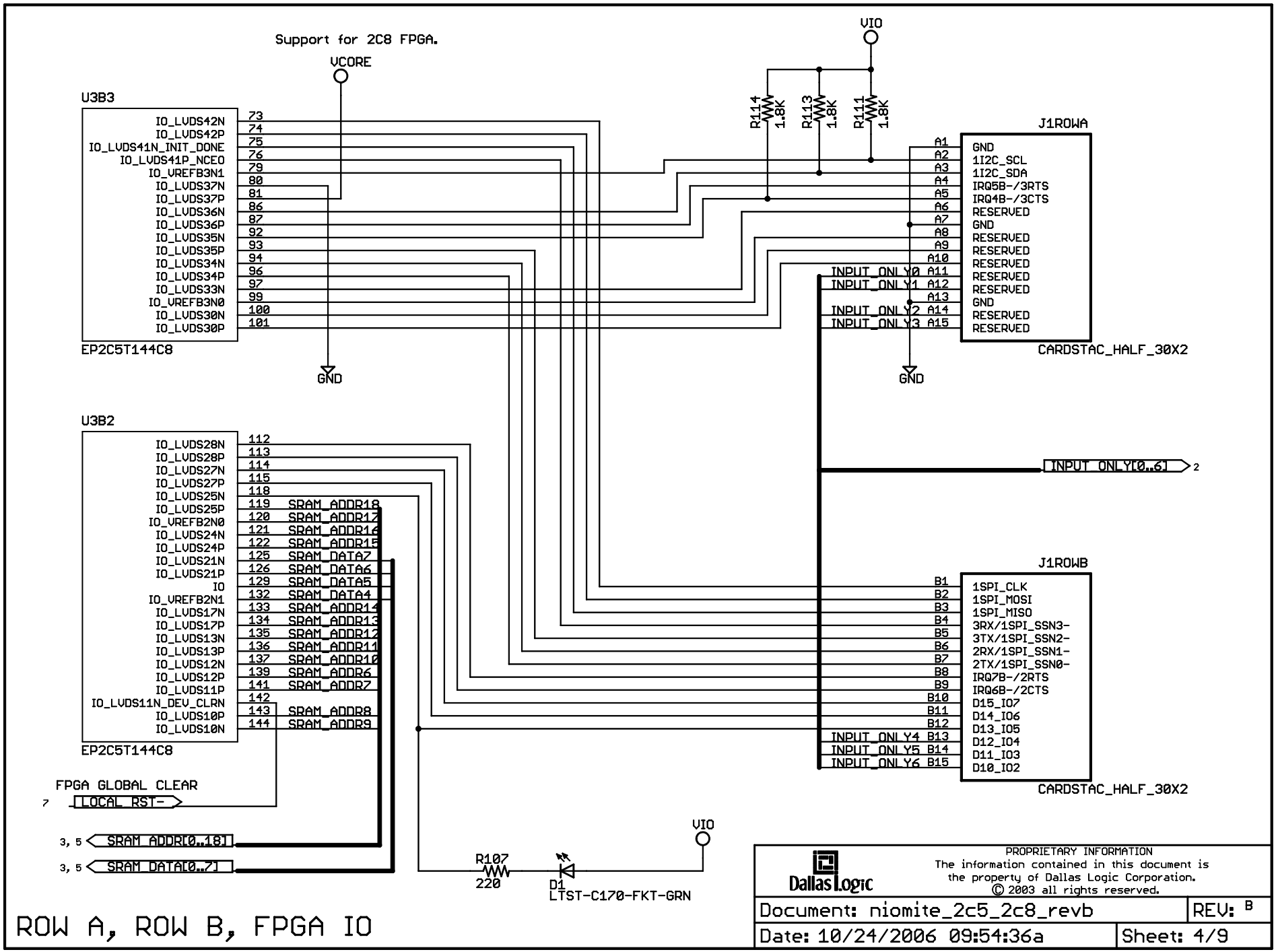
Support for 2C8 FPGA.
VCORE
VIO
U3B3
IO_LVDS42N 73
IO_LVDS42P 74
IO_LVDS41N_INIT_DONE 75
IO_LVDS41P_NCEO 76
IO_VREFB3N1 79
IO_LVDS37N 80
IO_LVDS37P 81
IO_LVDS36N 86
IO_LVDS36P 87
IO_LVDS35N 92
IO_LVDS35P 93
IO_LVDS34N 94
IO_LVDS34P 96
IO_LVDS33N 97
IO_VREFB3N0 99
IO_LVDS30N 100
IO_LVDS30P 101
EP2C5T144C8
GND
R114 1.8K
R113 1.8K
R111 1.8K
J1ROWA
A1 GND
A2 1I2C_SCL
A3 1I2C_SDA
A4 IRQ5B-/3RTS
A5 IRQ4B-/3CTS
A6 RESERVED
A7 GND
A8 RESERVED
A9 RESERVED
A10 RESERVED
INPUT_ONLY0 A11 RESERVED
INPUT_ONLY1 A12 RESERVED
A13 GND
INPUT_ONLY2 A14 RESERVED
INPUT_ONLY3 A15 RESERVED
CARDSTAC_HALF_30X2
GND
U3B2
IO_LVDS28N 112
IO_LVDS28P 113
IO_LVDS27N 114
IO_LVDS27P 115
IO_LVDS25N 118
IO_LVDS25P 119 SRAM_ADDR18
IO_VREFB2N0 120 SRAM_ADDR17
IO_LVDS24N 121 SRAM_ADDR16
IO_LVDS24P 122 SRAM_ADDR15
IO_LVDS21N 125 SRAM_DATA7
IO_LVDS21P 126 SRAM_DATA6
IO 129 SRAM_DATA5
IO_VREFB2N1 132 SRAM_DATA4
IO_LVDS17N 133 SRAM_ADDR14
IO_LVDS17P 134 SRAM_ADDR13
IO_LVDS13N 135 SRAM_ADDR12
IO_LVDS13P 136 SRAM_ADDR11
IO_LVDS12N 137 SRAM_ADDR10
IO_LVDS12P 139 SRAM_ADDR6
IO_LVDS11P 141 SRAM_ADDR7
IO_LVDS11N_DEV_CLRN 142
IO_LVDS10P 143 SRAM_ADDR8
IO_LVDS10N 144 SRAM_ADDR9
EP2C5T144C8
INPUT_ONLY[0..6] 2
J1ROWB
B1 1SPI_CLK
B2 1SPI_MOSI
B3 1SPI_MISO
B4 3RX/1SPI_SSN3-
B5 3TX/1SPI_SSN2-
B6 2RX/1SPI_SSN1-
B7 2TX/1SPI_SSN0-
B8 IRQ7B-/2RTS
B9 IRQ6B-/2CTS
B10 D15_IO7
B11 D14_IO6
B12 D13_IO5
INPUT_ONLY4 B13 D12_IO4
INPUT_ONLY5 B14 D11_IO3
INPUT_ONLY6 B15 D10_IO2
CARDSTAC_HALF_30X2
FPGA GLOBAL CLEAR
7 LOCAL_RST-
3, 5 SRAM_ADDR[0..18]
3, 5 SRAM_DATA[0..7]
VIO
R107 220
D1 LTST-C170-FKT-GRN
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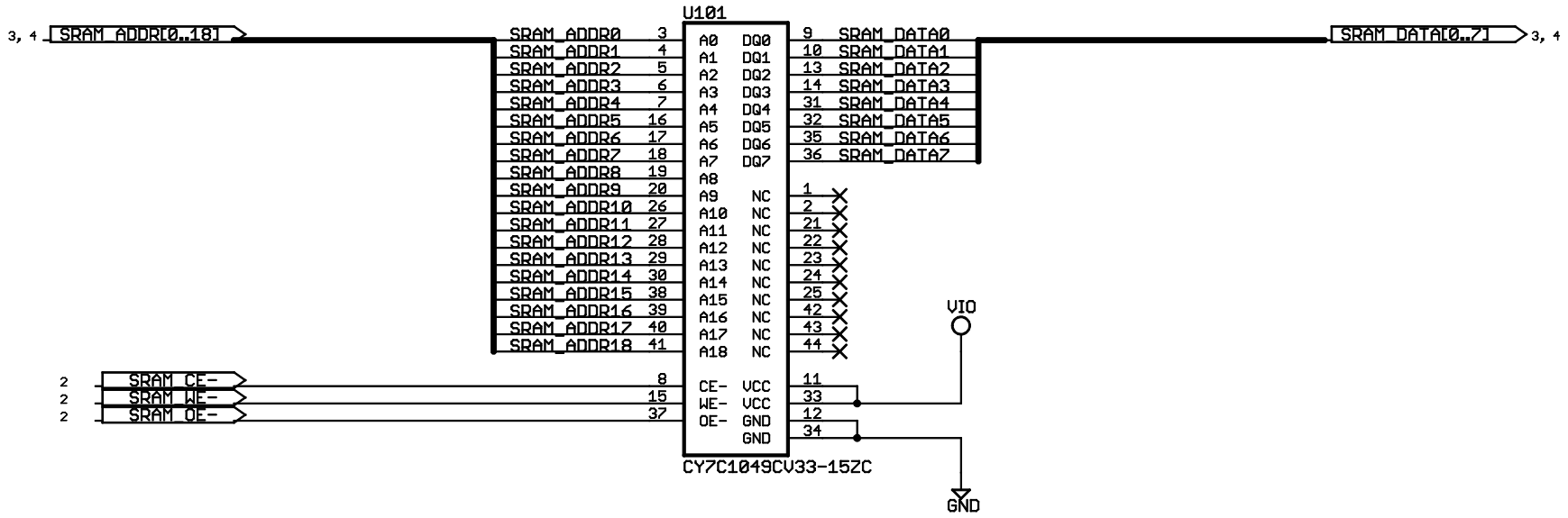
ROW A, ROW B, FPGA IO

512K X 8



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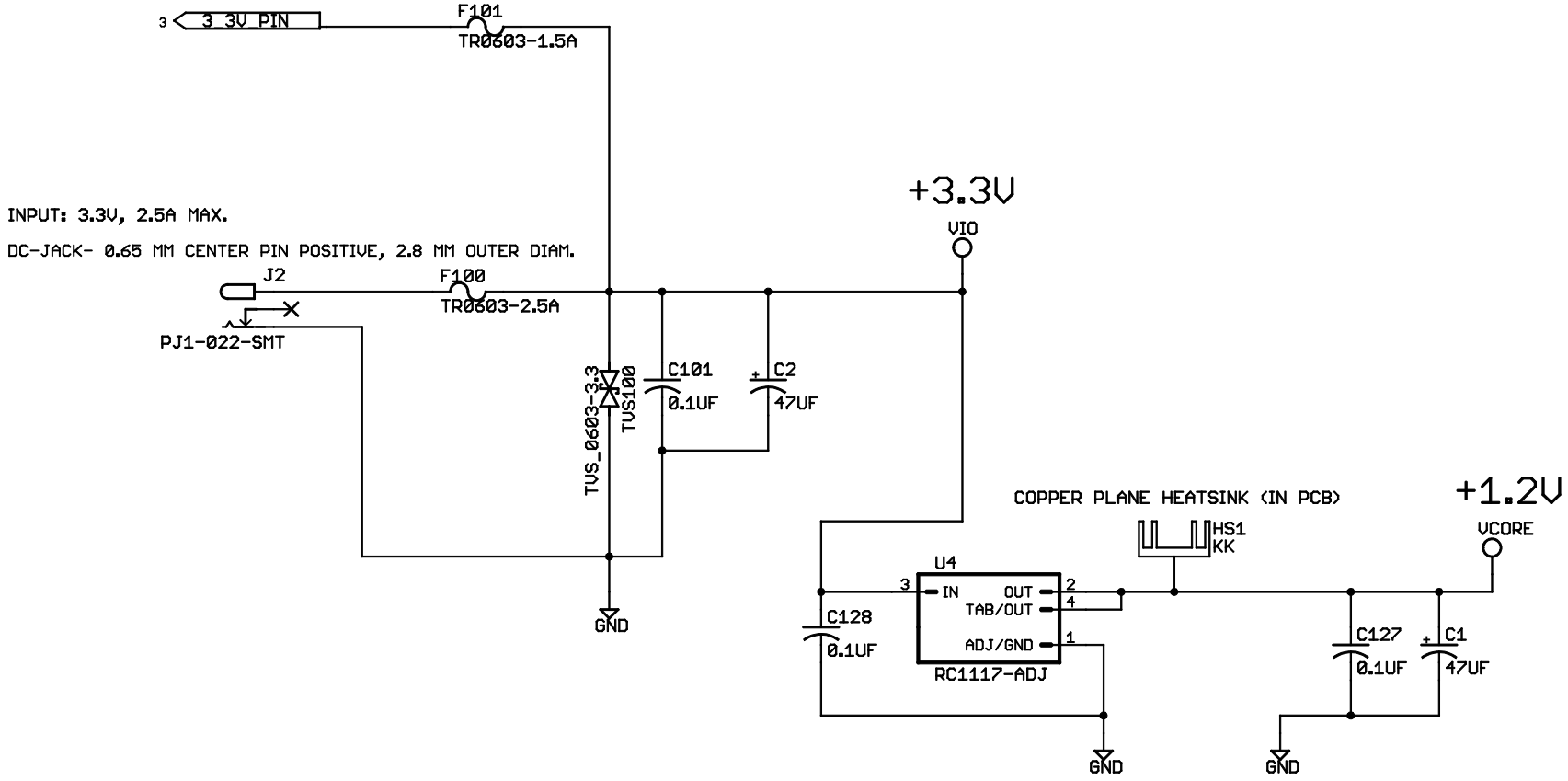
512K X 8 SRAM

MAY ALSO PULL CURRENT IN FROM 3_3V PIN (LOCAL POWER FROM EXTERNAL SOURCE).

REMOVE FUSE IF OTHER CARD SOURCES 3.3V POWER RAIL AND LOCAL DCJACK IS ATTACHED.



RC1117 Adjustable has a ref voltage of 1.25V.

No divider on pin 1 gives an output of 1.25V.

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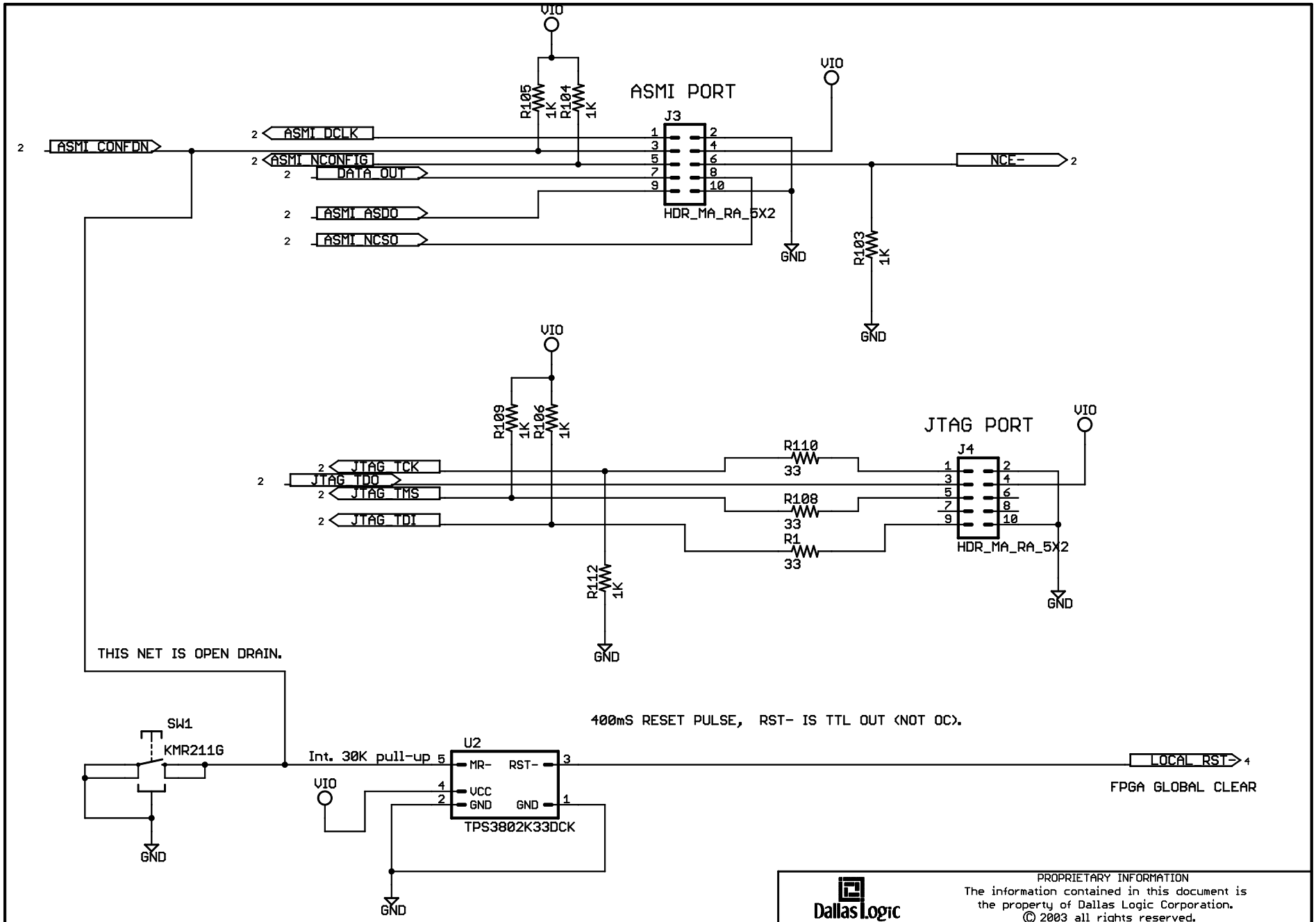
POWER SUPPLY



BYTE BLASTER PORTS, RESET/VMON

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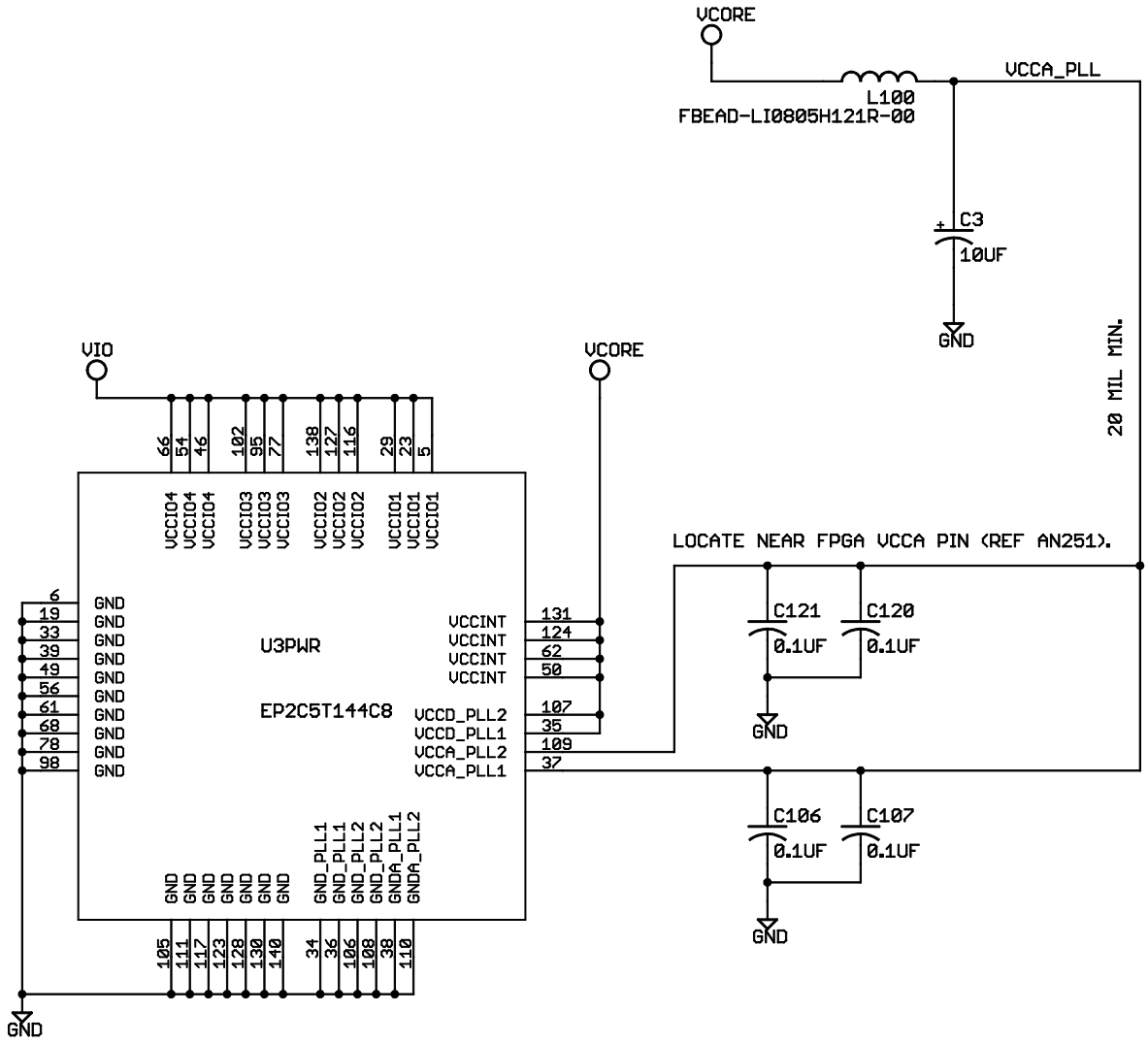

FPGA POWER

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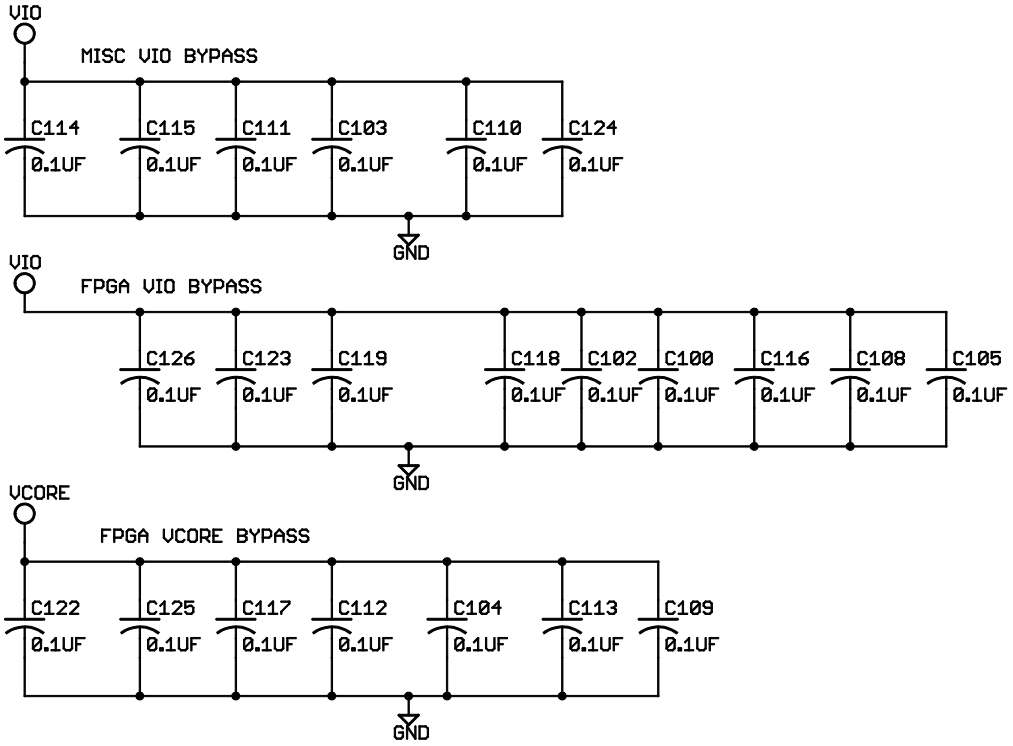

BYPASS CAPS

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