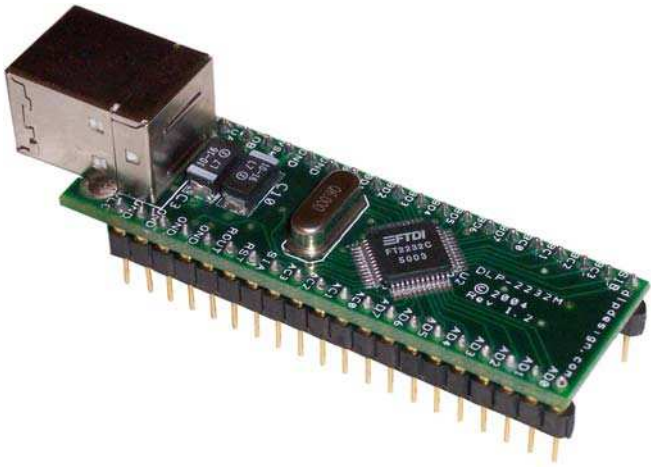
DLP Design

# DLP-2232M-G MODULE / EVALUATION KIT

*LEAD-FREE*



## 1.0 Introduction

The DLP-2232M-G utilizes FTDI's third-generation USB UART/FIFO I.C., the FT2232D. This low-cost development tool features two Multi-Purpose UART/FIFO controllers that can be configured individually in several different modes. In addition to the UART interface, FIFO interface, and Bit-Bang IO modes of the second-generation FT232BM and FT245BM devices, the FT2232D offers a variety of additional modes of operation including a Multi-Protocol Synchronous Serial Engine interface designed specifically for synchronous serial protocols such as JTAG and SPI bus.

The DLP-2232M-G features a quality four-layer printed circuit board with a solid ground plane, an integral 93C56 EEPROM on board for easy OEM customization and a standard 40-pin, 0.6in wide footprint. Integral power control and on-board MOSFET power switch make the DLP-2232M-G a perfect choice for USB bus-powered, high-power designs as well as self- and low-powered products.

## 1.1 Features Summary

- Single board, USB Dual Channel Serial / Parallel Ports with a variety of configurations
- Entire USB protocol handled on-board. No USB-specific firmware programming required
- DLP-USB232M-style UART interface option with full Handshaking & Modem interface signals
- UART Interface supports 7/8 bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity
- Transfer Data Rate 300 to 1 Mega Baud (RS232)
- Transfer Data Rate 300 to 3 Mega Baud (TTL and RS422 / RS485)
- Auto Transmit Enable control for RS485 serial applications using TXDEN pin
- DLP-USB245M-style FIFO interface option with bi-directional data bus and simple 4-wire handshake interface
- Transfer Data Rate up to 1 MegaByte / Second
- Enhanced Bit-Bang Mode interface option
- New Synchronous Bit-Bang Mode interface option
- New CPU-Style FIFO Interface Mode option
- New Multi-Protocol Synchronous Serial Engine (MPSSE) interface option
- New MCU Host Bus Emulation Mode option
- New Fast Opto-Isolated Serial Interface Mode option
- Interface mode and USB Description strings configurable in on-board EEPROM
- EEPROM Configurable in-circuit via USB
- Support for USB Suspend and Resume conditions via PWREN#, and SI/WUx pins
- Support for bus powered, self powered, and high-power bus powered USB configurations
- Integrated Power-On-Reset circuit, with optional Reset input and Reset Output pins
- 5V and 3.3V logic IO Interfacing with independent level conversion on each channel
- USB Bulk or Isochronous data transfer modes
- 4.35V to 5.25V single supply operating voltage range
- UHCI / OHCI / EHCI host controller compatible
- USB 2.0 Full Speed (12 Mbits/ Second) compatible
- Standard 40-pin, 0.6in wide footprint

VIRTUAL COM PORT (VCP) DRIVERS

- Windows 98 / 98 SE / 2000 / ME / XP
- Windows CE **
- MAC OS-8 and OS-9**
- MAC OS-X**
- Linux 2.40 and greater**

[ ** = In planning or under development ]

D2XX (Direct Drivers + DLL S/W

- Windows 98 / 98 SE / 2000 / ME / XP

APPLICATION AREAS

- USB Dual Port RS232 Converters
- USB Dual Port RS422 / RS485
- Upgrading Legacy Peripheral Designs
- USB Instrumentation
- USB JTAG Programming
- USB to SPI Bus Interfaces
- USB Industrial Control
- Field Upgradeable USB Products
- Galvanically Isolated Products With USB Interface

## 1.2 General Description

The DLP-2232M-G module is a USB interface that incorporates the functionality of two DLP-USB2xxM modules into a single 40-pin module. A single downstream USB port is converted to two IO channels that can each be individually configured as a DLP-USB232M-style UART interface, or a DLP-USB245M-style FIFO interface, without the need to add a USB hub.

There are also several new modes which can be enabled in the external EEPROM, or by using DLL driver commands. These include Synchronous Bit-Bang Mode, a CPU-Style FIFO Interface Mode, a Multi-Protocol Synchronous Serial Engine Interface Mode, MCU Host Bus Emulation Mode, and Fast Opto-Isolated Serial Interface Mode. Additionally, a new high output drive level option means that the device UART / FIFO IO pins will drive out at around three times the normal power level, allowing the data bus to be shared by several devices.

Classic BM-style Asynchronous Bit-Bang Mode is also supported, but has been enhanced to give the user access to the device's internal RD# and WR# strobes.

FTDI provides a royalty free Virtual Com Port (VCP) driver that makes the peripheral ports look like a standard COM port to the PC. Most existing software applications should be able interface with the Virtual Com Port simply by reconfiguring them to use the new ports created by the driver. Using the VCP drivers, an application programmer would communicate with the device in exactly the same way as they would a regular PC COM port - using the Windows VCOMM API calls or a COM port library.

The FT2232D driver also incorporates the functions defined for FTDI's D2XX drivers, allowing applications programmers to interface software directly to the device using a Windows DLL.

## 2.0 Features and Enhancements

The DLP-2232M-G incorporates all of the enhancements introduced for the second generation DLP-USB232M and DLP-USB245M modules, summarized here:

- Two Individually Configurable IO Channels

Each of the DLP-2232M-G's Channels (A and B) can be individually configured as a DLP-USB232M-style UART interface, or as a DL-USB245M-style FIFO interface. Additionally, these channels can be configured in a number of special IO modes.

- Integrated Power-On-Reset (POR) circuit

The module incorporates an internal POR function. A RESET# pin is available to allow external logic to reset the module where required, however for most applications this pin can simply be left disconnected as the RESET input to the FT2232D is pulled to VCC through a 47K resistor. A RSTOUT# pin is provided in order to allow the new POR circuit to provide a stable reset to external MCU and other devices.

- Integrated level converter on UART /FIFO interface and control signals

Each channel of the DLP-2232M-G has its own independent VCCIO pin that can be supplied by between 3V to 5V. This allows each channel's output voltage drive level to be individually configured. Thus allowing, for example, 3.3V logic to be interfaced to the device without the need for external level converter I.C.'s.

- Improved power management control for high-power USB Bus Powered devices

The PWREN# pin of the FT2232D directly drives a P-Channel MOSFET for applications where power switching of external circuitry is required. The BM pull down enable feature (configured in the external EEPROM) is also retained. This will make the module gently pull down on the FIFO / UART IO lines when the power is shut off (PWREN# is high). In this mode, any residual voltage on external circuitry is bled to GND when power is removed, thus ensuring that external circuitry controlled by PWREN# resets reliably when power is restored.

- Support for Isochronous USB Transfers

Whilst USB Bulk transfer is usually the best choice for data transfer, the scheduling time of the data is not guaranteed. For applications where scheduling latency takes priority over data integrity such as transferring audio and low bandwidth video data, the DLP-2232M-G offers the option of USB Isochronous transfer via configuration of bit in the EEPROM.

- Send Immediate / Wake Up Signal Pin on each channel

There is a Send Immediate / Wake Up (SI/WU) signal pin on each of the two channels. These combine two functions on one pin. If USB is in suspend mode (and remote wakeup is enabled in the EEPROM), strobing this pin low will cause the device to request a resume from suspend (WakeUp) on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation, if this pin is strobed low any data in the device RX buffer will be sent out over USB on the next Bulk-IN request from the

drivers regardless of the packet size. This can be used to optimize USB transfer speed for applications that send small packets of data to the host PC.

- Programmable Receive Buffer Timeout

The TX buffer timeout is programmable over USB in 1ms increments from 1ms to 255ms, thus allowing the module to be better optimized for protocols requiring faster response times from short data packets.

- Baud Rate Pre-Scaler Divisors

The DLP-2232M-G (UART mode) baud rate pre-scaler supports division by (n+0), (n+0.125), (n+0.25), (n+0.375), (n+0.5), (n+0.625), (n+0.75) and (n+0.875) where n is an integer between 2 and 16,384.

- USB 2.0 (full speed option)

An EEPROM based option allows the DLP-2232M-G to return a USB 2.0 device descriptor as opposed to USB 1.1. Note: The device would be a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).
For more details on these features please see the FT232BM and FT245BM datasheets and application notes.

In addition to the DLP-USB2xxM module features, the DLP-2232M-G incorporates the following new features and interface modes:

- Enhanced Asynchronous Bit-Bang Interface

The DLP-2232M-G supports FTDI's BM chip Bit Bang mode. In Bit Bang mode, the eight FIFO data lines can be switched between FIFO interface mode and an 8-bit Parallel IO port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal timer (equivalent to the baud rate prescaler). With the DLP-2232M-G module, this mode has been enhanced so that the internal RD# and WR# strobes are now brought out of the device which can be used to allow external logic to be clocked by accesses to the Bit-Bang IO bus.

- Synchronous Bit-Bang Interface

With Synchronous Bit-Bang Mode, the device is only read when it is written to, as opposed to asynchronously by the data rate generator. This makes it easier for the controlling program to measure the response to an output stimulus, as the data returned is synchronous to the output data.

- High Output Drive Level Capability

The IO interface pins can be made to drive out at 12 mA, instead of the normal 4 mA allowing multiple devices to be interfaced to the bus.

• CPU-Style FIFO Interface

The CPU style FIFO interface is essentially the same function as the classic FT245 interface, however the bus signals have been redefined to make them easier to interface to a CPU bus.

• Multi-Protocol Synchronous Serial Engine Interface (M.P.S.S.E.)

The Multi-Protocol Synchronous Serial Engine (MPSSE) interface is a new option designed to interface efficiently with synchronous serial protocols such as JTAG and SPI Bus. It is very flexible in that it can be configured for different industry standards, or proprietary bus protocols. For instance, it is possible to connect one of the DLP-2232M-G's channels to an SRAM configurable FPGA as supplied by vendors such as Altera and Xilinx. The FPGA device would normally be un-configured (i.e. have no defined function) at power-up. Application software on the PC could use the MPSSE to download configuration data to the FPGA over USB. This data would define the hardware's function and then, after the FPGA device is configured, the DLP-2232M-G can switch back into FIFO interface mode to allow the programmed FPGA device to communicate with the PC over USB. The other DLP-2232M-G channel would also be available for other devices.

This approach would allow a customer to create a "generic" USB peripheral; who's hardware function can be defined under control of the application software. The FPGA based hardware could be easily upgraded or totally changed simply by changing the FPGA configuration data file. (See the FTDI MORPH-IC or DLP-Design DLP-2232PB and DLP-2232SY development modules for practical examples)

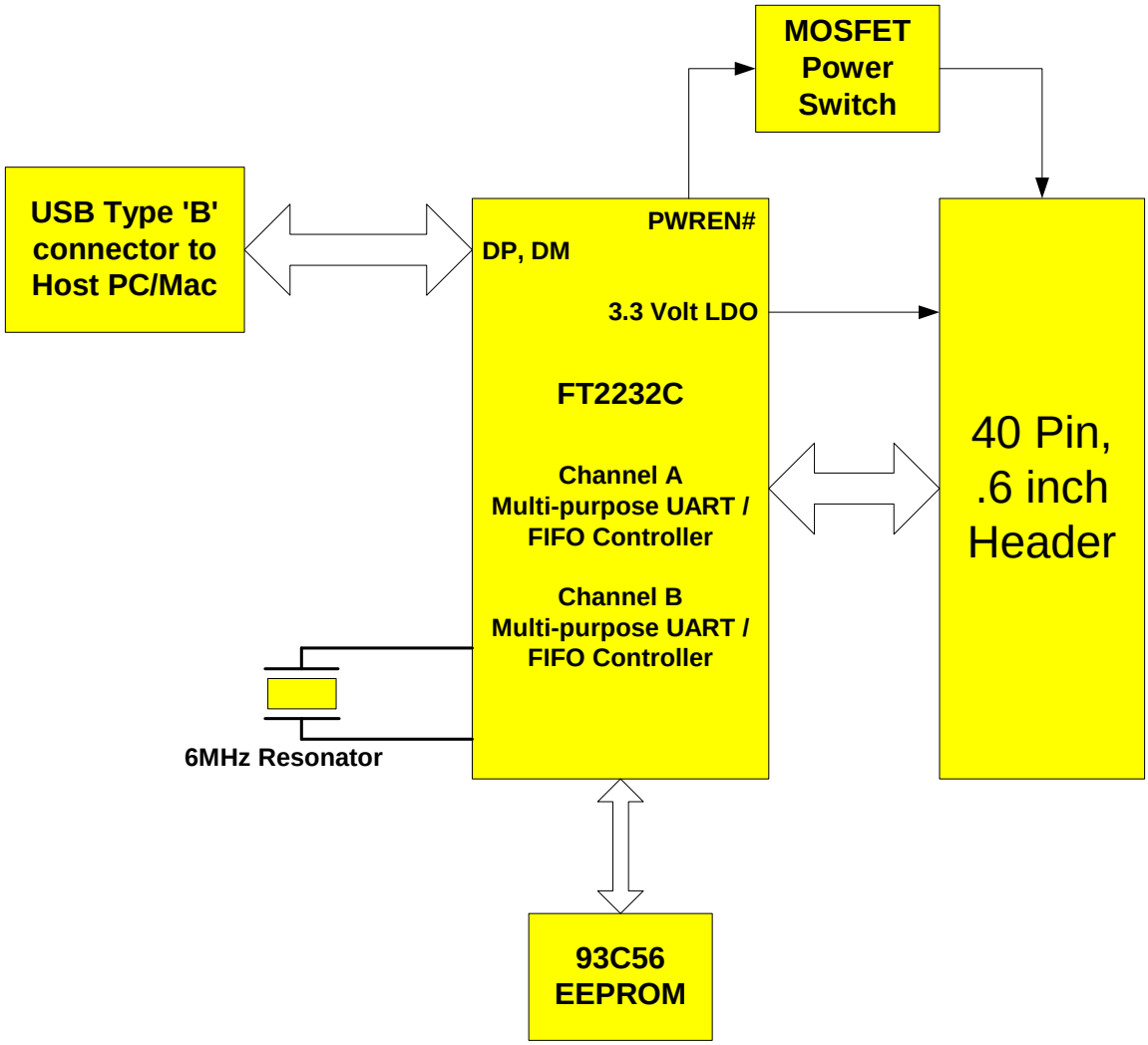
• MCU Host Bus Emulation

This new mode combines the 'A' and 'B' bus interface to make the DLP-2232M-G interface emulate a standard 8048 / 8051 style MCU bus. This allows peripheral devices for these MCU families to be directly attached to the DLP-2232M-G with IO being performed over USB with the help of MPSSE interface technology.

• Fast Opto-Isolated Serial Interface

A new proprietary FTDI protocol is designed to allow galvanically isolated devices to communicate synchronously with the DLP-2232M-G using just 4 wires (two dual opto-isolators). The peripheral circuitry controls the data transfer rate in both directions, whilst maintaining full data integrity. Maximum USB full speed data rates can be achieved. Both 'A' and 'B' channels can communicate over the same 4-wire interface if desired.

## 3.0 DLP-2232M-G Module Simplified Block Diagram




## 3.1 Functional Block Descriptions

• 6MHz Oscillator

The 6MHz Oscillator cell generates a 6MHz reference clock input to the x8 Clock multiplier from an external 6MHz ceramic resonator.

• Multi-Purpose UART / FIFO Controllers

The Multi-purpose UART / FIFO controllers handle the transfer of data between the Dual Port RX and TX buffers and the UART / FIFO transmit and receive registers. When configured as a UART it performs asynchronous 7/8 bit parallel to serial and serial to parallel conversion of the data on the RS232 (RS422 and RS485) interface. Control signals supported by UART mode include RTS, CTS, DSR, DTR, DCD and RI. There are also transmitter enable control signal pins (TXDEN) provided to assist with interfacing to RS485 transceivers. RTS/CTS, DSR/DTR and X-On/X-Off handshaking options are also supported. Handshaking, where required, is handled in hardware to

ensure fast response times. The UARTs also support the RS232 BREAK setting and detection conditions.

- EEPROM Interface

The on-board 93C56 EEPROM allows each of the DLP-2232M-G module's channels to be independently configured as a serial UART (232 mode), or a parallel FIFO (245 mode). The EEPROM is used to enable the CPU-style FIFO interface, and Fast Opto-Isolated Serial interface modes. The driver type selection (VCP or D2XX) is also stored in the EEPROM.

The EEPROM can also be used to customize the USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the DLP-2232M-G for OEM applications. Other parameters controlled by the EEPROM include Remote Wake Up, Isochronous Transfer Mode, Soft Pull Down on Power-Off and USB 2.0 descriptor modes.

The EEPROM is programmable in-circuit via USB using the MPROG utility program available from both www.dlpdesign.com and FTDI's web site (www.ftdichip.com).

## 4.0 Module Pin-Out

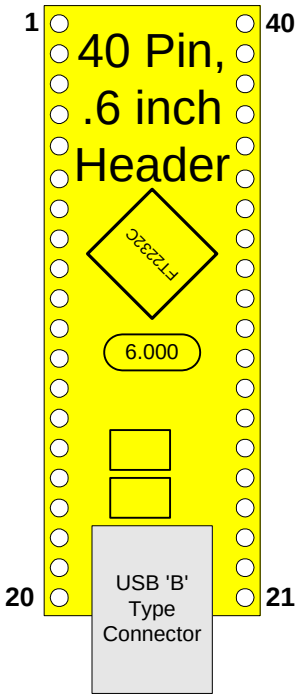



Figure 2. Pin-Out (40 Pin DIP Header )

## 4.1 Pin Definitions

This section describes the operation of the DLP-2232M-G pins. Common pins are defined in the first section and the I/O pins are defined by chip mode. More detailed descriptions of the operation of the I/O pins are provided in section x. (was 9)

## 4.2 Common Pins

The operation of the following DLP-2232M-G pins stay the same, regardless of the operating mode.

| Pin# | Signal | Type | Description |
|---|---|---|---|
| 27 | RSTIN# | Input | Can be used by an external device to reset the FT2232D. If not required, can be left disconnected. |
| 26 | RSTOUT# | Output | Output of the internal Reset Generator. Stays high impedance for ~5ms after VCC > 3.5V and the internal clock starts up, then clamps it's output to the 3.3V output of the internal regulator. Taking RESET# low will also force RSTOUT# to drive low. RSTOUT# is NOT affected by a USB Bus Reset. |
| 19 | EXTVCC | PWR | +4.35 to +5.25 volt VCC to the device core, LDO and non- |

| | | | |
|---|---|---|---|
| | | | UART / FIFO controller interface pins.<br>Device Analog Power Supply for the internal x8 clock multiplier. |
| 18 | VCCIOA | PWR | +3.0 to +5.25 volt VCC to the UART/FIFO Channel A interface pins. When interfacing with 3.3V external logic connect VCCIO to the 3.3V supply of the external logic, otherwise connect to VCC to drive out at 5V CMOS level. |
| 17 | VCCIOB | PWR | +3.0 volt to +5.25 volt VCC to the UART/FIFO Channel B interface pins. When interfacing with 3.3V external logic connect VCCIO to the 3.3V supply of the external logic, otherwise connect to VCC to drive out at 5V CMOS level. |
| 20 | PORTVCC | PWR | Power from USB port. Connect to EXTVCC if module is to be powered by the USB port (typical configuration). 500mA maximum current available to USB adapter and target electronics if USB device is configured for high power. |
| 16 | VCCSW | PWR | Output of the MOSFET power switch, activated after enumeration. |
| 21 | VCCUSB | PWR | Filtered +3.0 volt to +5.25 volt EXTVCC from either the host USB port or user supplied external power supply. |

## 4.3 IO Pin Definitions by Chip Mode

The definition of the following pins vary according to the module's mode:

| Pin# | Generic Pin Name | Pin Definitions by Chip Mode *Note 2 | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | 232 UART Mode | 245 FIFO Mode | CPU FIFO Interface Mode | Enhanced Asynchronous and Synchronous Bit-Bang Modes | MPSSE *Note 4 | MCU Host Bus Enumeration Mode *Note 5 | Fast Opto-Isolated Serial Mode |
| 40 | ADBUS0 | TXD | D0 | D0 | D0 | TCK/SK | AD0 | *Note 3 |
| 39 | ADBUS1 | RXD | D1 | D1 | D1 | TDI/DU | AD1 | |
| 38 | ADBUS2 | RTS# | D2 | D2 | D2 | TDO/D1 | AD2 | |
| 37 | ADBUS3 | CTS# | D3 | D3 | D3 | TMS/CS | AD3 | |
| 36 | ADBUS4 | DTR# | D4 | D4 | D4 | GPIOL0 | AD4 | |
| 35 | ADBUS5 | DSR# | D5 | D5 | D5 | GPIOL1 | AD5 | |
| 34 | ADBUS6 | DCD# | D6 | D6 | D6 | GPIOL2 | AD6 | |
| 33 | ADBUS7 | RI# | D7 | D7 | D7 | GPIOL3 | AD7 | |
| 32 | ACBUS0 | TXDEN | RXF# | CS# | WR# *Note 6 | GPIOH0 | I/O0 | |
| 31 | ACBUS1 | SLEEP# | TXE# | A0 | RD# *Note 6 | GPIOH1 | I/O1 | |
| 30 | ACBUS2 | RXLED# | RD# | RD# | WR# *Note 7 | GPIOH2 | IORDY# | |
| 29 | ACBUS3 | TXLED# | WR | WR# | RD# *Note 7 | GPIOH3 | OSC | |
| 28 | SI/WUA | ??? | SI/WUA | SI/WUA | | SI/WUA | | |

| Pin# | Generic Pin Name | Pin Definitions by Chip Mode *Note 2 | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | 232 UART Mode | 245 FIFO Mode | CPU FIFO Interface Mode | Enhanced Asynchronous and Synchronous Bit-Bang Modes | MPSSE *Note 4 | MCU Host Bus Enumeration Mode *Note 5 | Fast Opto-Isolated Serial Mode |
| 13 | BDBUS0 | TXD | D0 | D0 | D0 | | AD8 | FSDI |
| 12 | BDBUS1 | RXD | D1 | D1 | D1 | | AD9 | FSCLK |
| 11 | BDBUS2 | RTS# | D2 | D2 | D2 | | AD10 | FSDO |
| 10 | BDBUS3 | CTS# | D3 | D3 | D3 | | AD11 | FSCTS |
| 9 | BDBUS4 | DTR# | D4 | D4 | D4 | | AD12 | *Note 3 |
| 8 | BDBUS5 | DSR# | D5 | D5 | D5 | | AD13 | |
| 7 | BDBUS6 | DCD# | D6 | D6 | D6 | | AD14 | |
| 6 | BDBUS7 | RI# | D7 | D7 | D7 | | AD15 | |
| 5 | BCBUS0 | TXDEN | RXF# | CS# | WR# *Note 8 | | CS# | |
| 4 | BCBUS1 | SLEEP# | TXE# | A0 | RD# *Note 8 | | ALE | |
| 3 | BCBUS2 | RXLED# | RD# | RD# | WR# *Note 7 | | RD# | |
| 2 | BCBUS3 | TXLED# | WR | WR# | RD# *Note 7 | | WR# | |
| 1 | SI/WUB | ??? | SI/WUB | SI/WUB | | | | |

*Note 2 : 232 UART, 245 FIFO, CPU FIFO Interface, and Fast Opto-Isolated modes are enabled in the external EEPROM. Enhanced Asynchronous and Synchronous Bit-Bang modes, MPSSE, and MCU Host Bus Emulation modes are enabled using driver commands.

*Note 3 : Channel A can be configured in another IO mode if channel B is in Fast Opto-Isolated Serial Mode. If both Channel A and Channel B are in Fast Opto-Isolated Serial Mode all of the IO will be on Channel B.

*Note 4 : MPSSE is Channel A only.

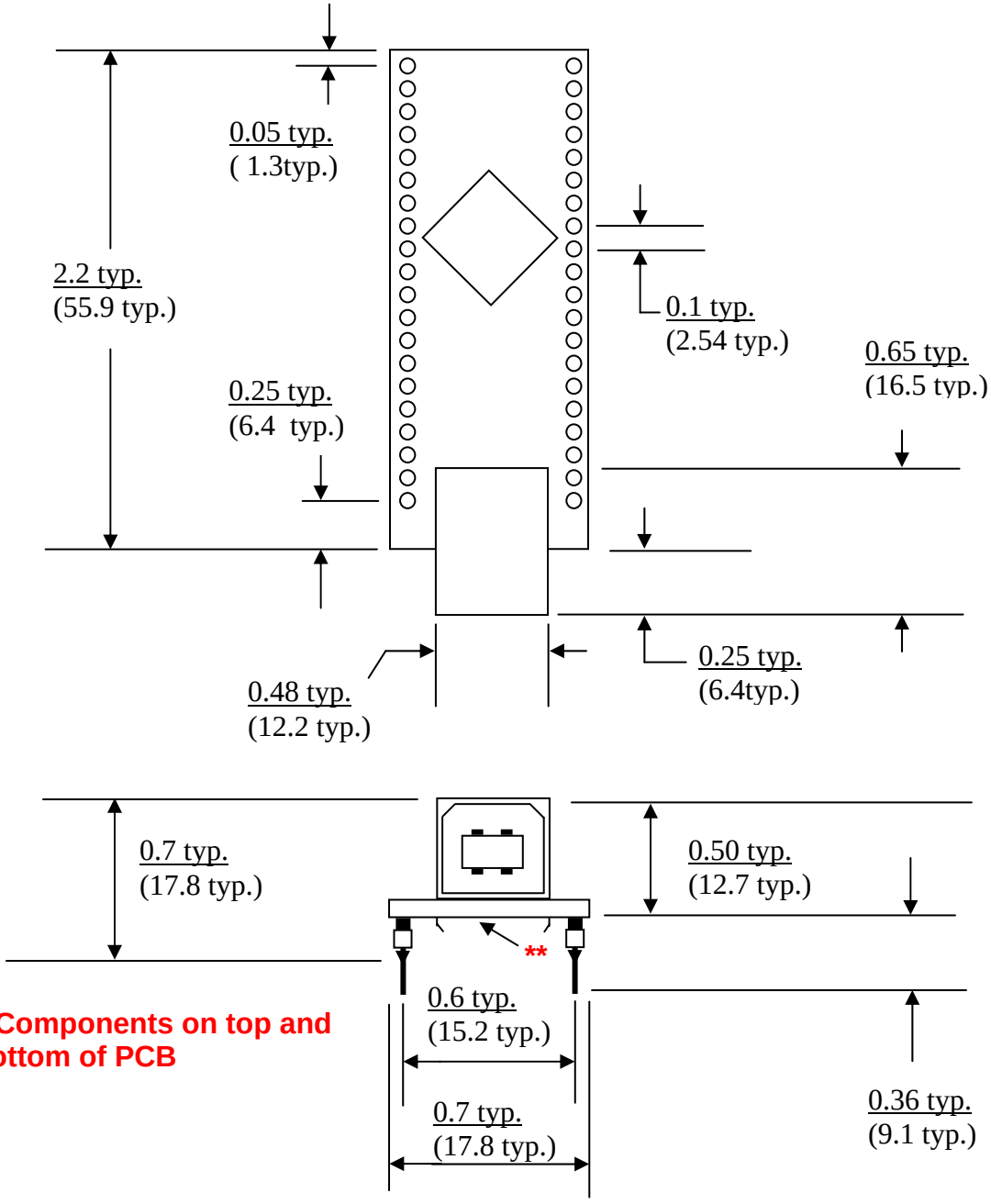
*Note 5 : MCU Host Bus Emulation requires both Channels.

*Note 6 : The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 245 FIFO, CPU FIFO interface, or Fast Opto-Isolated Serial Modes.

*Note 7 : The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 232 UART Mode.

*Note 8 : The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 245 FIFO, CPU FIFO interface. Bit-Bang mode is not available on Channel B when Fast Opto-Isolated Serial Mode is enabled.

## 5.0 Mechanical Dimensions
## Inches (mm)




****Components on top and bottom of PCB**

## 6.0 Absolute Maximum Ratings

These are the absolute maximum ratings for the FT2232D device. Exceeding these may cause permanent damage to the device.

- Storage Temperature ……..-65°C to + 150°C
- Ambient Temperature (Power Applied)…….. 0°C to 70°C
- VCC Supply Voltage ……..-0.5V to +6.00V
- DC Input Voltage - Inputs ……..-0.5V to VCC + 0.5V
- DC Input Voltage - High Impedance Bi-directional ……..-0.5V to VCC + 0.5V
- DC Output Current – Outputs……...24mA
- DC Output Current – Low Impedance Bi-directional ……24mA
- Power Dissipation (VCC = 5.25V)……..500mW
- Electrostatic Discharge Voltage (Human Body Model) (I < 1uA)…….+/- 3000V
- Latch Up Current (Vi = +/- 10V maximum, for 10 ms)……+/-200mA

## 7.0 D.C. Characteristics

### D.C. Characteristics (Ambient Temperature = 0 to 70°C)
### Operating Voltage and Current

| Parameter | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Vcc1 | VCC Operating Supply Voltage | 4.35 | 5.0 | 5.25 | V | |
| Vcc2 | VCCIO Operating Supply Voltage | 3.0 | - | 5.25 | V | |
| Icc1 | Operating Supply Current | - | 25? | - | mA | Normal Operation |
| Icc2 | Operating Supply Current | - | ?? | 200? | uA | USB Suspend *Note 11 |

*Note 11 – Supply Current excludes the 200uA nominal drawn by the pull-up resistor on USBDP

IO Pin Characteristics (VCCIOx = 5.0V) *Note 12

| Parameter | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Voh | Output Voltage High | 3.2 | 4.1 | 4.9 | V | I source = 2mA |
| Vol | Output Voltage Low | 0.3 | 0.4 | 0.6 | V | I sink = 2mA |
| Vin | Input Switching Threshold | 1.3 | 1.6 | 1.9 | V | *Note 13 |
| Vhys | Input Switching Hysteresis | 50 | 55 | 60 | mV | |

IO Pin Characteristics (VCCIOx = 3.0 – 3.6V) *Note 12

| Parameter | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Voh | Output Voltage High | 2.2 | 2.7 | 3.2 | V | I source = 1mA |
| Vol | Output Voltage Low | 0.3 | 0.4 | 0.5 | V | I sink = 2mA |
| Vin | Input Switching Threshold | 1.0 | 1.2 | 1.5 | V | *Note 13 |
| Vhys | Input Switching Hysteresis | 20 | 25 | 30 | mV | |

*Note 12 – Inputs have a 200K Ohm pull-up resistor to VCCIOx internal to the FT2232D.
*Note 13 – This is the standard output driver

RESET# and RSTOUT# Pin characteristics

| Parameter | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Vin | Input Switching Threshold | 1.3 | 1.6 | 1.9 | V | |
| VHys | Input Switching Hysteresis | 50 | 55 | 60 | mV | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Voh | Output Voltage High | 3.0 | - | 3.6 | V | I source = 2mA |
| Vol | Output Voltage Low | 0.3 | - | 0.6 | V | I sink = 2mA |

## 8.0 Standard Device Configuration Examples

### 8.1 USB Bus Powered and Self Powered Configuration

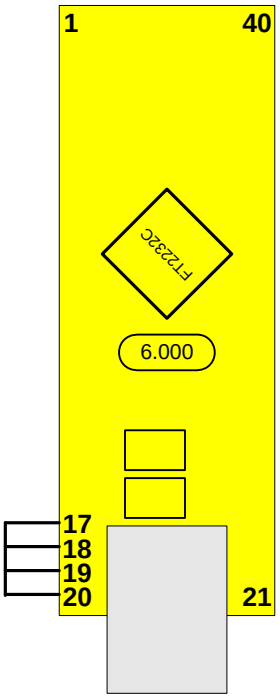



Figure 8a - USB Bus Powered Configuration

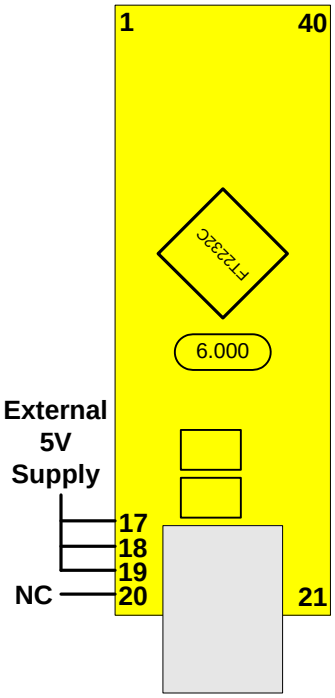



Figure 8b – Self Powered Configuration

Figure 8a illustrates the DLP-2232M-G in a typical USB bus powered configuration. A USB Bus Powered device gets its power from the USB bus. Basic rules for USB Bus power devices are as follows –
a) On plug-in, the device must draw no more than 100mA
b) On USB Suspend the device must draw no more than 500uA.
c) A High Power USB Bus Powered Device (one that draws more than 100mA) should use the on-board MOSFET to keep the current drawn by external circuitry to below ~70mA on plug-in and ~200uA on USB suspend.
d) A device that consumes more than 100mA cannot be plugged into a USB Bus Powered Hub
e) No device can draw more that 500mA from the USB Bus. The power descriptor in the EEPROM should be programmed to match the current draw required by the device.
A Ferrite Bead is connected in series with USB power to prevent noise from the device and associated circuitry (EMI) being radiated down the USB cable to the host.

Figure 8b illustrates the DLP-2232M-G in a typical USB self powered configuration. A USB Self Powered device gets its power from its own power supply and does not draw current from the USB bus. The basic rules for USB Self power devices are as follows –
a) A Self-Powered device should not force current down the USB bus when the USB Host or Hub Controller is powered down.
b) A Self-Powered device can take as much current as it likes during normal operation and USB suspend as it has its own power source.
c) A Self-Powered device can be used with any USB Host and both Bus and Self Powered USB Hubs.
The USB power descriptor option in the EEPROM should be programmed to a value of zero (self powered).

To meet requirement a) the 1.5K pull-up resistor on USBDP is connected to RSTOUT# as per the bus-power circuit. However, the USB Bus Power is used to control the RESET# Pin of the FT2232D device. When the USB Host or Hub is powered up RSTOUT# will pull the 1.5K resistor on USBDP to 3.3V, thus identifying the device as a full speed device to USB. When the USB Host or Hub power is off, RESET# will go low and the device will be held in reset. As RESET# is low, RSTOUT# will also be low, so no current will be forced down USBDP via the 1.5K pull-up resistor when the host or hub is powered down. Failure to do this may cause some USB host or hub controllers to power up erratically.

Note: When the DLP-2232M-G is in reset, the I/O interface pins all go tri-state. These pins have 200K pull-up resistors to VCCIOx internal to the FT2232D, so they will gently pull high unless driven by some external logic.

## 8.2 Interfacing to Microcontrollers

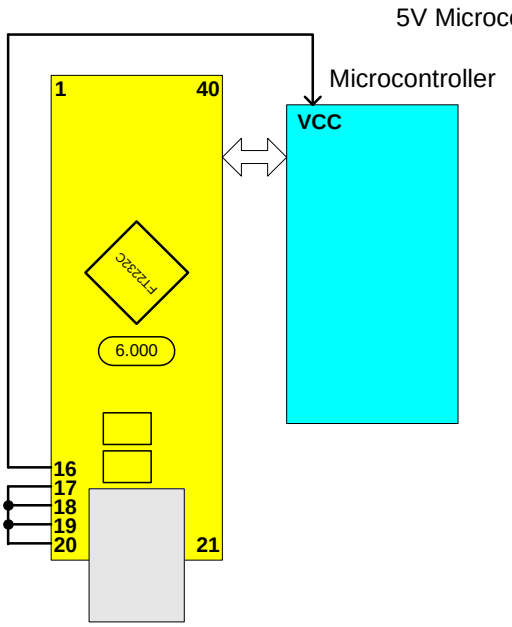



Figure 10a - Bus Powered

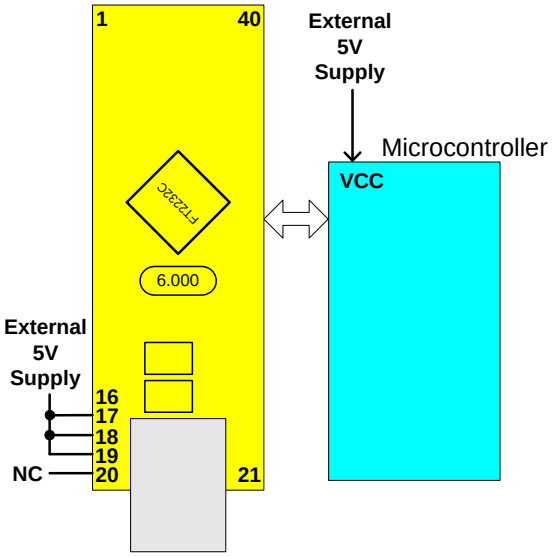



Figure 10b - Self Powered

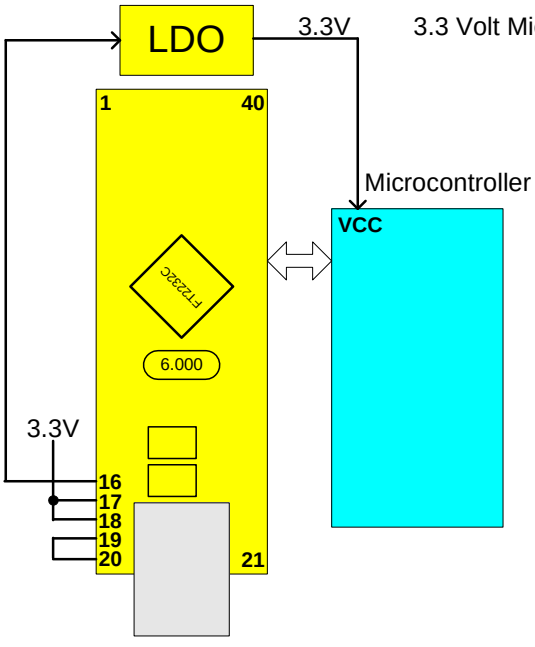



Figure 10c - Bus Powered

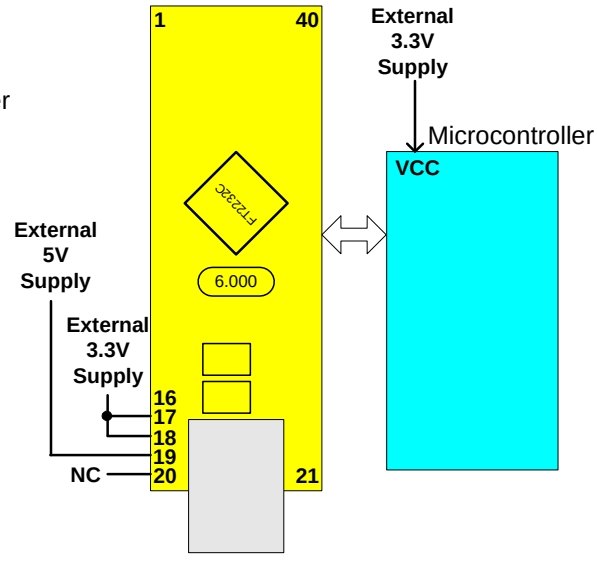



Figure 10d - Self Powered

### 8.2.1 USB Bus-Powered, 5V Systems

Figure 10a shows how to configure the DLP-2232M-G to interface with a 5V microcontroller. In this example, the USB port is the power source for VCCIOA and VCCIOB, which in turn will cause the device interface IO pins on both channels to drive out at the 5V level. In this configuration, the on-board MOSFET power switch controls power to the microcontroller. Care must be taken to ensure all microcontroller circuitry, when combined with the DLP-2232M-G circuitry, does not exceed the maximum available current from the USB port of 500mA for a high-powered USB device.

### 8.2.2 USB Self-Powered, 5V Systems

Figure 10b is an example of a DLP-2232M-G USB self-powered design with 5V interface. In this case, the VCCIOA and VCCIOB pins are supplied by an external 5V supply in order to make both of the device's IO channels drive out at 5V logic level, thus allowing them to be connected to a 5V microcontroller or other external logic.

A USB self-powered design uses its own power supplies, and does not draw any of its power from the USB bus. In such cases, no special care need be taken to meet the USB suspend current (0.5 mA) as the device does not get it's power from the USB port. Note that if the SI/WUx pins are not being used they should be pulled up to the same supply as their respective VCCIOx pin.

### 8.2.3 USB Bus-Powered, 3.3V Systems

Figure 10c shows how to configure the DLP-2232M-G to interface with a 3.3V microcontroller. In this example, a discrete 3.3V regulator is used to supply the 3.3V logic from the USB supply. VCCIOA and VCCIOB are connected to the output of the 3.3V regulator, which in turn will cause the device interface IO pins on both channels to drive out at 3.3V level. It is also possible to have one IO interface channel driving out at 5V level, and the other at 3.3V level. In this case one of the VCCIOx pins would be connected to 5V, and the other connected to 3.3V. For USB bus powered circuits, care must be taken when selecting the regulator. The regulator must be capable of sustaining its output voltage with an input voltage of 4.35 volts. A Low Drop Out (LDO) regulator must be selected. An example of a regulator family that meets these requirements is the MicroChip (Telcom) TC55 Series. These devices can supply up to 250mA current.

Note: It should be emphasized that the 3.3V supply, for VCCIOx in a bus powered design with a 3.3V logic interface, should come from an LDO that is supplied by the USB bus, not from any other source. Please also note that if the SI/WUx pins are not being used they should be pulled up to the same supply as their respective VCCIOx pin.

### 8.2.4 USB Self-Powered, 3.3V Systems

Figure 10d is an example of a DLP-2232M-G USB self-powered design with 3.3V interface. In this case, the VCCIOA and VCCIOB pins are supplied by an external 3.3V supply in order to make both of the device's IO channels drive out at 3.3V logic level,

thus allowing them to be connected to a 3.3V microcontroller or other external logic. It is also possible to have one IO interface channel driving out at 5V level, and the other at 3.3V level. In this case one of the VCCIOx pins would be connected to 5V, and the other connected to 3.3V.
A USB self-powered design uses its own power supplies, and does not draw any of its power from the USB bus. In such cases, no special care need be taken to meet the USB suspend current (0.5 mA) as the device does not get it's power from the USB port.
Note that if the SI/WUx pins are not being used they should be pulled up to the same supply as their respective VCCIOx pin.

## 9.0 Signal Descriptions By IO Mode and Interface Channel Configurations

### 9.1 232 UART Interface Mode Signal Descriptions and Interface Configurations

When either Channel A or Channel B are in 232 UART mode the IO signal lines are configured as follows:

| Pin# | | Signal | Type | Description |
|---|---|---|---|---|
| Channel A | Channel B | | | |
| 40 | 13 | TXD | OUTPUT | Transmit Asynchronous Data Output |
| 39 | 12 | RXD | INPUT | Receive Asynchronous Data Input *Note 9 |
| 38 | 11 | RTS# | OUTPUT | Request To Send Control Output / Handshake signal |
| 37 | 10 | CTS# | INPUT | Clear To Send Control Input / Handshake signal *Note 9 |
| 36 | 9 | DTR# | OUTPUT | Data Terminal Ready Control Output / Handshake signal |
| 35 | 8 | DSR# | INPUT | Data Set Ready Control Input / Handshake signal *Note 9 |
| 34 | 7 | DCD# | INPUT | Data Carrier Detect Control Input *Note 9 |
| 33 | 6 | RI# | INPUT | Ring Indicator Control Input. When the Remote Wake up option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend. *Note 9 |

*Note 9 : These pins are pulled to up VCCIO via 200K resistors in the FT2232D during Reset and USB Suspend mode. These can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting this option in the EEPROM.

## 9.2 245 FIFO Interface Mode Signal Descriptions and Configuration

When either Channel A or Channel B are in 245 FIFO mode, the IO signal lines are configured as follows.

FIFO DATA BUS GROUP *Note 10

| Pin# | | Signal | Type | Description |
|---|---|---|---|---|
| Channel A | Channel B | | | |
| 40 | 13 | D0 | I/O | FIFO Data Bus Bit 0 |
| 39 | 12 | D1 | I/O | FIFO Data Bus Bit 1 |
| 38 | 11 | D2 | I/O | FIFO Data Bus Bit 2 |
| 38 | 10 | D3 | I/O | FIFO Data Bus Bit 3 |
| 36 | 9 | D4 | I/O | FIFO Data Bus Bit 4 |
| 35 | 8 | D5 | I/O | FIFO Data Bus Bit 5 |
| 34 | 7 | D6 | I/O | FIFO Data Bus Bit 6 |
| 33 | 6 | D7 | I/O | FIFO Data Bus Bit 7 |

FIFO CONTROL INTERFACE GROUP

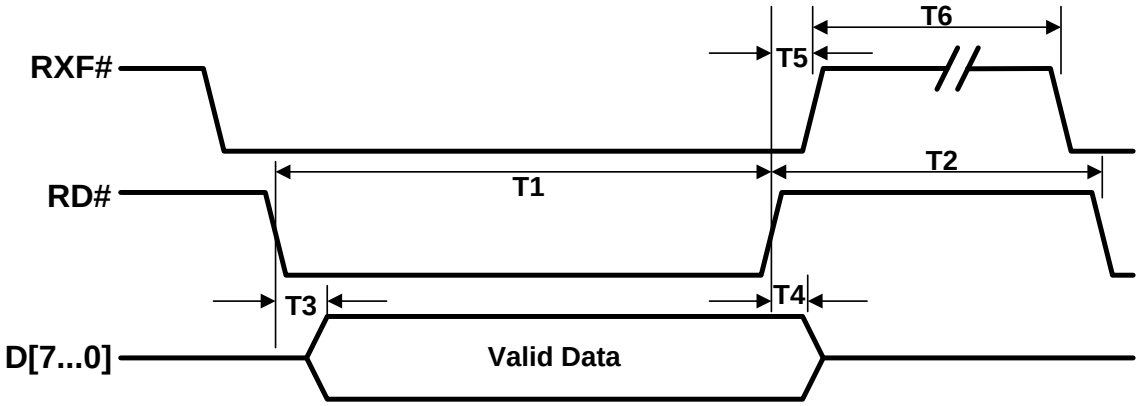
| Pin# | | Signal | Type | Description |
|---|---|---|---|---|
| Channel A | Channel B | | | |
| 32 | 5 | RXF# | OUTPUT | When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by strobing RD# low then high again * Note 11 |
| 31 | 4 | TXE# | OUTPUT | When high, do not write data into the FIFO. When low, data can be written into the FIFO by transitioning WR from high to low. * Note 11 |
| 30 | 3 | RD# | INPUT | Enables Current FIFO Data Byte on D0..D7 when low. Fetches the next FIFO Data Byte (if available) from the Receive FIFO Buffer when RD# goes from low to high. * Note 10 |
| 29 | 2 | WR | INPUT | Writes the Data Byte on the D0..D7 into the Transmit FIFO Buffer on the falling edge of WR. * Note 10 |
| 28 | 1 | SI/WUx | INPUT | The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM, strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC.<br>During normal operation (PWREN# = 0), if this pin is strobed low any data in the device TX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIOx if not used. |

*Note 10: In Input Mode, these pins are pulled to VCCIOx via 200K resistors in the FT2232D. These can be programmed to gently pull low during USB suspend (PWREN# = “1”) by setting this option in the EEPROM.

*Note 11: During device reset, these pins are tri-state but pulled up to VCCIOx via 200K resistors in the FT2232D.

## 9.3 245 FIFO Mode Timing Diagrams

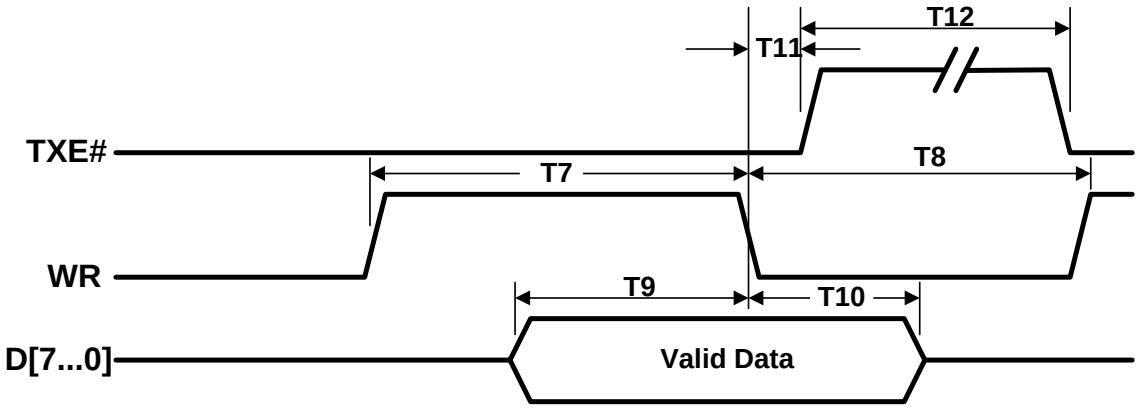
### 9.3.1 FIFO Read Cycle Timing




| Time | Description | Min | Max | Unit |
|---|---|---|---|---|
| T1 | RD# Active Pulse Width | 50 | | nS |
| T2 | RD# to RD Pre-Charge Time | 50 + T6 | | nS |
| T3 | RD# Active to Valid Data ** **Note 12** | 20 | 50 | nS |
| T4 | Valid Data Hold Time from RD# Inactive ** **Note 12** | 0 | | nS |
| T5 | RD# Inactive to RXF# | 0 | 25 | nS |
| T6 | RXF# inactive after RD# cycle | 80 | | nS |

** **Note 12:** Load 30 pF

### 9.3.2 FIFO Write Cycle Timing




| Time | Description | Min | Max | Unit |
|---|---|---|---|---|
| T7 | WR# Active Pulse Width | 50 | | nS |
| T8 | WR to WR Pre-Charge Time | 50 + T12 | | nS |
| T9 | Data Setup Time before WR inactive | 20 | | nS |

| | | | | |
|---|---|---|---|---|
| T10 | Data Hold Time from WR Inactive | 0 | | nS |
| T11 | WR Inactive to TXE# | 5 | 25 | nS |
| T12 | TXE# inactive after a read cycle | 80 | | nS |

## 9.4 Enhanced Asynchronous and Synchronous Bit-Bang Modes - Signal Description and Interface Configuration

Bit-bang mode is a special DLP-2232M-G mode that changes the 8 IO lines on either or both channels (A/B) into an 8 bit bi-directional bus. There are now two types of bit bang modes - Enhanced Asynchronous, which is virtually the same as BM-style Bit-Bang mode; and synchronous Bit-Bang mode, where data will only be read when the device is written to. Bit-Bang mode is enabled by driver commands. When either Channel A or Channel B are enabled in Enhanced Asynchronous Bit-Bang Mode, or Synchronous Bit-Bang Mode the IO signal lines are configured as follows:

BIT-BANG DATA BUS GROUP *Note 10

| Pin# | | Signal | Type | Description |
|---|---|---|---|---|
| Channel A | Channel B | | | |
| 40 | 13 | D0 | I/O | Bit-Bang Data Bus Bit 0 |
| 39 | 12 | D1 | I/O | Bit-Bang Data Bus Bit 1 |
| 38 | 11 | D2 | I/O | Bit-Bang Data Bus Bit 2 |
| 38 | 10 | D3 | I/O | Bit-Bang Data Bus Bit 3 |
| 36 | 9 | D4 | I/O | Bit-Bang Data Bus Bit 4 |
| 35 | 8 | D5 | I/O | Bit-Bang Data Bus Bit 5 |
| 34 | 7 | D6 | I/O | Bit-Bang Data Bus Bit 6 |
| 33 | 6 | D7 | I/O | Bit-Bang Data Bus Bit 7 |

BIT-BANG CONTROL INTERFACE GROUP

| Pin# | | Signal | Type | Description |
|---|---|---|---|---|
| Channel A | Channel B | | | |
| 32 | 5 | WR# | OUTPUT | ***Note 13** |
| 31 | 4 | RD# | OUTPUT | ***Note 13** |
| 30 | 3 | WR# | OUTPUT | ***Note 13** |
| 29 | 2 | RD# | OUTPUT | ***Note 13** |

*Note 10: In Input Mode, these pins are pulled to VCCIOx via 200K resistors in the FT2232D. These can be programmed to gently pull low during USB suspend (PWREN# = “1”) by setting this option in the EEPROM.

*Note 13: The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 245 FIFO, CPU FIFO interface, or Fast Opto-Isolated Serial Mode. Bit-Bang mode is not available on Channel B when Fast Opto-Isolated Serial Mode is enabled.

*Note 14: The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is set to 323 UART Mode.

## 9.5 Enhanced Asynchronous Bit-Bang Mode

Enhanced Asynchronous Bit-Bang mode is the same as BM-style Bit-Bang mode, except that the internal RD# and WR# strobes are now brought out of the DLP-2232M-G to allow external logic to be clocked by accesses to the bit-bang IO bus.

On either or both channels, any data written to the device in the normal manner will be self clocked onto the data pins (those which have been configured as outputs). Each pin can be independently set as an input or an output. The baud rate generator controls the rate at which the data is clocked out.

For the data to change there has to be new data written, and the baud rate clock has to tick. If no new data is written to the channel, the pins will hold the last value written. To allow time for the data to be setup and held around the WR# strobe, the baud rate should be less than 1 MegaBaud.

Enabling

Asynchronous Bit-Bang mode is enabled by the Set Bit Bang Mode command:

Set_USB_Device_BitMode($00,$01) ; to enable it

Set_USB_Device_BitMode($00,$00) ; to reset it

## 9.6 Synchronous Bit-Bang Mode

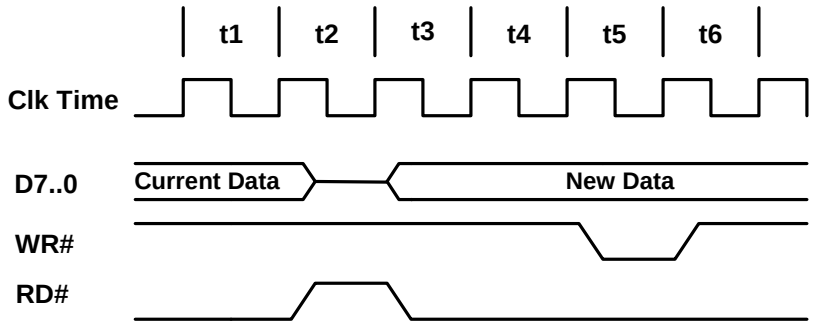
With Synchronous Bit-Bang enabled, data will only be sent out by the FT2232D if there is space in the device for data to come in. This Synchronous Bit-Bang mode will read the data bus pins first, before it sends out the byte that has just been transmitted. It is therefore 1 byte behind the output, and so to read the inputs for the byte that you have just sent, another byte must be sent.

For example:

(1)
Pins start at 0xFF
Send 0x55,0xAA
Pins go to 0x55 and then to 0xAA

Data read = 0xFF,0x55

(2)
Pins start at 0xFF
Send 0x55,0xAA,0xAA
(repeat the last byte sent)
Pins go to 0x55 and then to 0xAA
Data read = 0xFF,0x55,0xAA
Figure 25 - Synchronous Bit Bang Mode Signal Timing




| Time | Description |
|---|---|
| t1 | Current pin state is read |
| t2 | RD# is set inactive |
| t3 | RD# is set active again, and any pins that are output will change to the new data. |
| t4 | Clock state for data setup |
| t5 | WR# goes active |
| t6 | WR# goes inactive |

The internal RD# and WR# strobes are brought off-board to allow external logic to be clocked by accesses to the bit-bang IO bus.

Enabling

Synchronous Bit-Bang mode is enabled by the Set Bit Bang Mode command:

Set_USB_Device_BitMode($00,$04) ; to enable it

Set_USB_Device_BitMode($00,$00) ; to reset it

## 9.7 Multi-Protocol Synchronous Serial Engine (MPSSE) Mode Signal Descriptions and Interface Configurations

MPSSE Mode is designed to allow the DLP-2232M-G to interface efficiently with synchronous serial protocols such as JTAG and SPI Bus. It can also be used to program SRAM based FPGA's over USB. The MPSSE interface is designed to be flexible so that it can be configured to allow any synchronous serial protocol (industry standard or proprietary) to be interfaced to the DLP-2232M-G. MPSSE is available on channel A only.

MPSSE is fully configurable, and is programmed by sending commands down the data pipe. These can be sent individually, or more efficiently in packets. MPSSE is capable of a maximum sustained data rate of 5.6 Mega bits / s.

When Channel A is configured in MPSSE mode the IO signal lines are configured as follows:

| Pin# (Channel A Only) | Signal | Type | Description |
|---|---|---|---|
| 40 | TCK/SK | | |
| 39 | TDI/D0 | | |
| 38 | TDO/D1 | | |
| 37 | TMS/CS | | |
| 36 | GPIOL0 | | |
| 35 | GPIOL1 | | |
| 34 | GPIOL2 | | |
| 33 | GPIOL3 | | |
| 32 | GPIOH0 | | |
| 31 | GPIOH1 | | |
| 30 | GPIOH2 | | |
| 29 | GPIOH3 | | |
| 28 | SI/WU | | |

Enabling

MPSSE mode is enabled using the Set Bit-Bang Mode command.
Set_USB_Device_BitMode($00,$02) ; to enable.
Set_USB_Device_BitMode($00,$00) ; to reset.
MPSSE is fully described in a separate FTDI application note.

## 9.8 MCU Host Bus Emulation Mode Signal Descriptions and Interface Configuration

MCU host bus emulation mode uses both of the DLP2232M's A and B channel interfaces to make the chip emulate a standard 8048 / 8051 MCU host bus. This allows peripheral devices for these MCU families to be directly connected to USB via the DLP2232M.

The lower 8 bits (AD7 to AD0) is a multiplexed Address / Data bus. A8 to A15 provide upper (extended) addresses.

There are 4 basic operations:
1) Read (does not change A15 to A8)
2) Read Extended (changes A15 to A8)
3) Write (does not change A15 to A8)
4) Write Extended (changes A15 to A8)

Enabling

MCU Host Bus Emulation Mode enabled using the Set Bit-Bang Mode command.

Set_USB_Device_BitMode($00,$08) ; to enable it

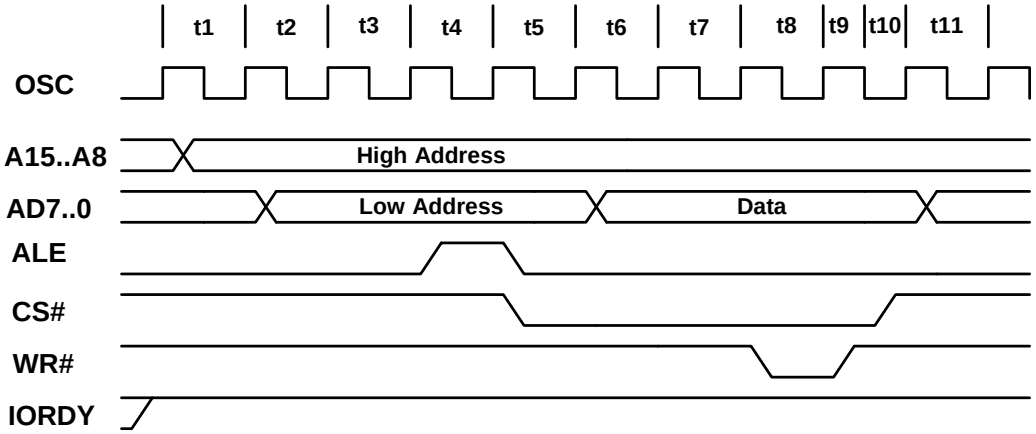
Set_USB_Device_BitMode($00,$00) ; to reset it

When MCU Host Bus Emulation mode is enabled the IO signal lines on both channels work together and the pins are configured as follows:

| Pin# | Signal | Type | Description |
|---|---|---|---|
| 40 | AD0 | I/O | Address / Data Bus Bit 0 |
| 39 | AD1 | I/O | Address / Data Bus Bit 1 |
| 38 | AD2 | I/O | Address / Data Bus Bit 2 |
| 37 | AD3 | I/O | Address / Data Bus Bit 3 |
| 36 | AD4 | I/O | Address / Data Bus Bit 4 |
| 35 | AD5 | I/O | Address / Data Bus Bit 5 |
| 34 | AD6 | I/O | Address / Data Bus Bit 6 |
| 33 | AD7 | I/O | Address / Data Bus Bit 7 |
| 32 | I/O0 | | MPSSE mode instructions to set / clear or read the high byte of data can be used with this pin. *Note |
| 31 | I/O1 | | MPSSE mode instructions to set, clear or read the high byte of data can be used with this pin. Additionally, this pin has instructions that will make the controller wait until it is high, or wait until it is low. This can be used to connect to an IRQ pin of a peripheral chip. The DLP2232M will wait for the interrupt, and then read the device, and pass the answer back to the host PC. I/O1 must be held in input mode if this option is used. *Note |
| 30 | IORDY# | INPUT | Extends the time taken to perform a Read or Write operation if pulled low. Pull up to Vcc if not being used. |
| 29 | OSC | OUTPUT | Shows the clock signal that the circuit is using. |
| 13 | A8 | OUTPUT | Extended Address Bus Bit 8 |
| 12 | A9 | OUTPUT | Extended Address Bus Bit 9 |
| 11 | A10 | OUTPUT | Extended Address Bus Bit 10 |
| 10 | A11 | OUTPUT | Extended Address Bus Bit 11 |
| 9 | A12 | OUTPUT | Extended Address Bus Bit 12 |
| 8 | A13 | OUTPUT | Extended Address Bus Bit 13 |
| 7 | A14 | OUTPUT | Extended Address Bus Bit 14 |
| 6 | A15 | OUTPUT | Extended Address Bus Bit 15 |
| 5 | CS# | OUTPUT | Negative pulse to select device during Read or Write. |
| 4 | ALE | OUTPUT | Positive pulse to latch the address. |
| 3 | RD# | OUTPUT | Negative Read Output. |
| 2 | WR# | OUTPUT | Negative Write Output. (Data is setup before WR# goes low, and is held after WR# goes high) |
| 1 | NC | | No Connect |

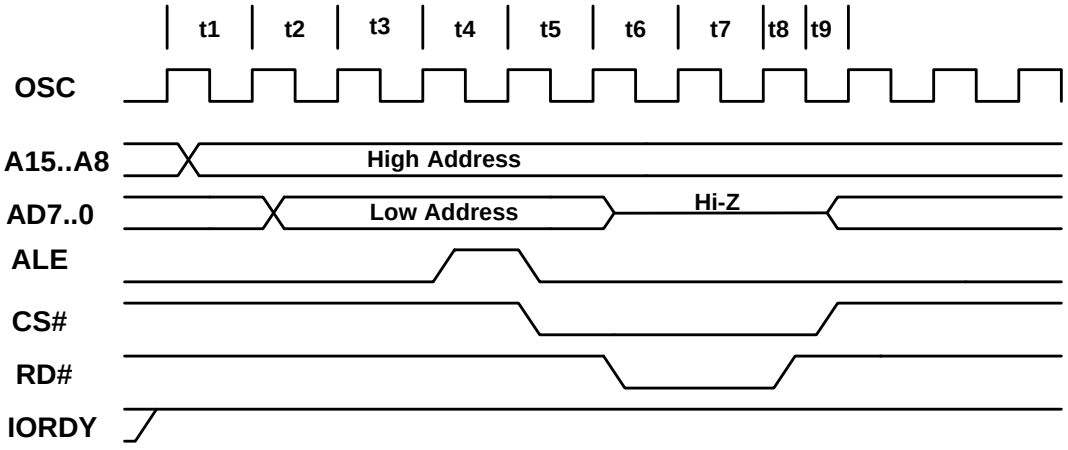
*Note: These instructions are fully described in a separate FTDI, MPSSE mode application note.

Figure 29 - MCU Host Bus Emulation Mode Signal Timing - Write Cycle



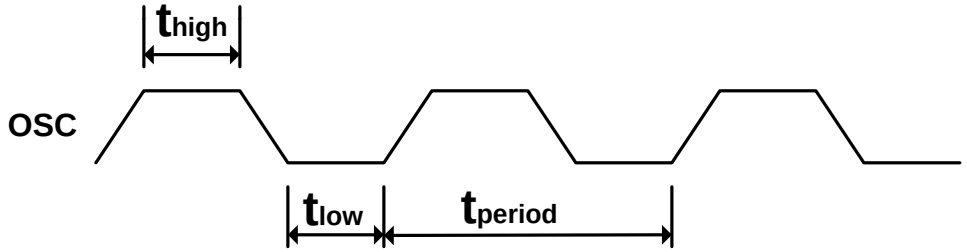

| Time | Description |
|---|---|
| t1 | High address byte is placed on the bus if the extended write is used. |
| t2 | Low address byte is put out. |
| t3 | 1 clock period for address is set up. |
| t4 | ALE goes high to enable latch. This will extend to 2 clocks wide if IORDY# is low. |
| t5 | ALE goes low to latch address and CS# is set active low. |
| t6 | Data driven onto the bus. |
| t7 | 1 clock period for data setup. |
| t8 | WR# is driven active low. This will extend to 6 clocks wide if IORDY# is low. |
| t9 | WR# is driven inactive high. |
| t10 | CS# is driven inactive, 1/2 a clock period after WR# goes inactive |
| t11 | Data is held until here and may now change |

Figure 30 - MCU Host Bus Emulation Mode Signal Timing - Read Cycle




| Time | Description |
|---|---|
| t1 | High address byte is placed on the bus if the extended read is used - otherwise t1 will not occur. |
| t2 | Low address byte is put out. |
| t3 | 1 clock period for address set up. |
| t4 | ALE goes high to enable address latch. This will extend to 2 clocks wide if IORDY# is low. |
| t5 | ALE goes low to latch address, and CS# is set active low. This will extend to 3 clocks if IORDY# is sam-pled low. CS# will always drop 1 clock after ALE has gone high no matter the state of IORDY#. |
| t6 | Data is set as input (Hi-Z), and RD# is driven active low. |
| t7 | 1 clock period for data setup. This will extend to 5 clocks wide if IORDY# is sampled low. |
| t8 | RD# is driven inactive high. |
| t9 | CS# is driven inactive 1/2 a clock period after RD# goes inactive, and the data bus is set back to output. |

Figure 31 - MCU Host Bus Emulation Mode Signal Timing - Clock (OSC) Signal




| Time | Description | Typical Value | Unit |
|---|---|---|---|
| tperiod | Clock Period | ?? | ns |

| | | | |
|---|---|---|---|
| thigh | Clock signal high time | ?? | ns |
| tlow | Clock signal low time | ?? | ns |

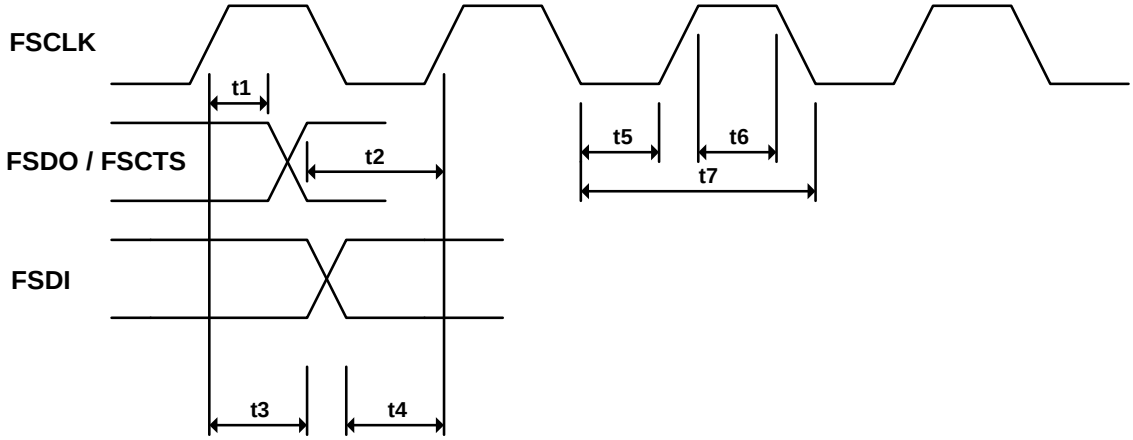
## 9.9 Fast Opto-Isolated Serial Interface Mode Signal Description and Configuration

Fast Opto-Isolated Serial Interface Mode provides a method of communicating with an external device over USB using 4 wires that can have opto-isolators in their path, thus providing galvanic isolation between systems. If either channel A or channel B are enabled in fast opto-isolated serial mode then the pins on channel B are switched to the fast serial interface configuration. The I/O interface for fast serial mode is always on channel B, even if both channels are being used in this mode. An address bit is used to determine the source or destination channel of the data. It therefore makes sense to always use at least channel B or both for fast serial mode, but not A own its own. When either Channel B or Both Channel A and B are configured in Fast Opto-Isolated Serial Interface mode following IO signal lines are configured as follows:

| Pin# | Signal | Type | Description |
|---|---|---|---|
| 13 | FSDI | INPUT | Fast serial data input |
| 12 | FSCLK | INPUT | Clock input into the chip to clock data in or out. The external device has to provide a clock signal or nothing will change on the interface pins. This gives the external device full control over the interface. It is designed to be half duplex so that data is only transferred in one direction at a time. |
| 11 | FSDO | OUTPUT | Fast serial data output. Driven low to indicate that the chip is ready to send data. |
| 10 | FSCTS | OUTPUT | Clear To Send control signal output |

Fast Opto-Isolated serial interface mode is enabled in the external EEPROM.

Figure 33 - Fast Opto-Isolated Serial Signal Timing Diagram

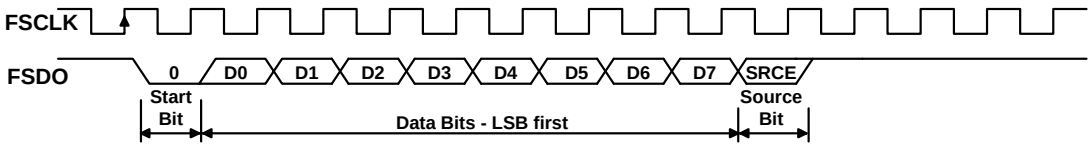



| Time | Description | Min | Max | Unit |
|---|---|---|---|---|
| t1 | FSDO / FSCTS hold time | | | ns |
| t2 | FSDO / FSCTS setup time | | | ns |
| t3 | FSDI hold time | 5 | | ns |
| t4 | FSDI setup time | 10 | | ns |
| t5 | FSCLK low | 10 | | ns |
| t6 | FSCLK high | 10 | | ns |
| t7 | FSCLK Period | 20 | | ns |

Outgoing Fast Serial Data

To send fast serial data out of the chip, the external device must clock. If the chip has data ready to send, it will drive FSDO low to indicate the start bit. It will not do this if it is currently receiving data from the external device.

Figure 34 - Fast Opto-Isolated Serial Data Format - Data output from the FT2232D



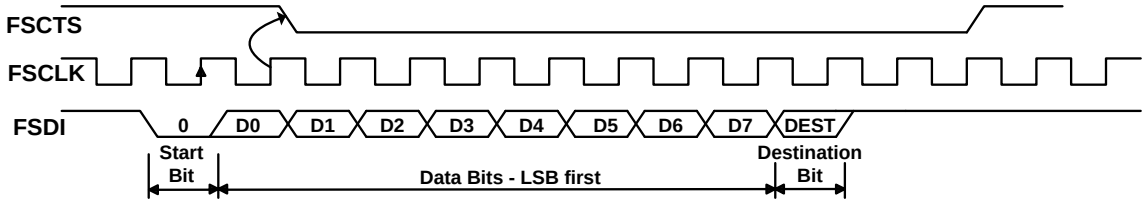

Notes:
(i) Start Bit is always 0.
(ii) Data is sent LSB first.
(iii) The source bit (SRCE) indicates which channel the data has come from. A ‘0’ means that it has come from Channel A, a ‘1’ means that it has come from Channel B.

(iv) If the target device is unable to accept the data when it detects the start bit, it should stop the FSCLK until it can accept the data.

Incoming Fast Serial Data

The external device is allowed to send data into the chip if FSCTS is high. On receipt of a Zero start bit on FSDI, the module will drop FSCTS on the next positive clock edge. The data from bits 0 to 7 is then clocked in (LSB first). The next bit determines where the data will be written. It can go to either channel A or to channel B. A '0' will send it to channel A, providing channel A is enabled for fast serial mode, otherwise it will go to channel B. A '1' will send it to channel B, providing channel B is enabled for fast serial mode, otherwise it will go to channel A. Either channel A, or channel B, or both must be enabled as fast serial mode or the circuit is disabled.

Figure 35 - Fast Opto-Isolated Serial Data Format - Data input to the DLP-2232M-G




Notes:
(i) Start Bit is always 0.
(ii) Data is sent LSB first.
(iii) The destination bit (DEST) indicates which channel the data should go to. A '0' means that it should go to channel A, a '1' means that it should go to channel B.
(iv) The target device should check CTS is high before it sends data. CTS goes low after data bit 0 (D0) and stays low until the chip can accept more data.

Contention

There is a possibility that contention may occur, where the interface goes from being completely idle to both sending and receiving at the same clock instance. In this case the chip backs off, and allow the data from the external device to be received.

Data Format

The data format for either direction is:
1) Zero Start Bit
2) Data bit 0
3) Data bit 1
4) Data bit 2
5) Data bit 3
6) Data bit 4
7) Data bit 5

8) Data bit 6
9) Data bit 7
10) Source/Destination (‘0’ indicates channel A; ‘1’ indicates channel B)

Enabling

Fast serial mode is enabled via EEPROM option bits. The device can be reset by setting an enable value of $10 to the Set Bit Bang Mode command. While this bit is set, the device is held reset.

Set_USB_Device_BitMode($00,$10) ; to reset it

Set_USB_Device_BitMode($00,$00) ; to enable it

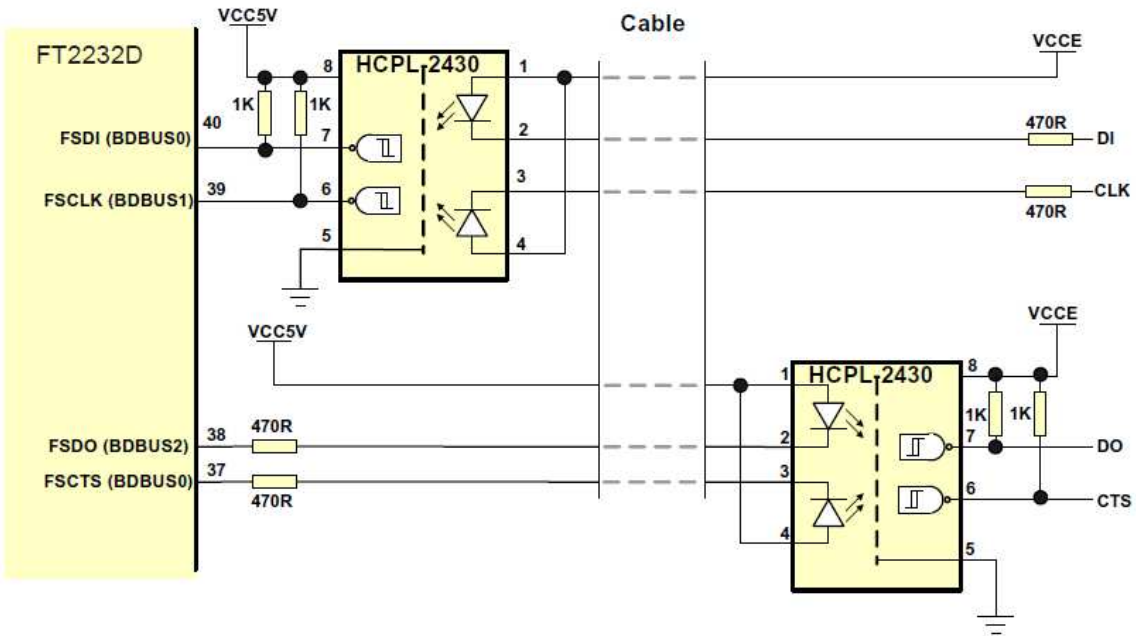



Figure 36 - Fast Opto-Isolated Serial Interface Example

## 10.0 Disclaimer



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This document provides information that may be subject to change without notice.

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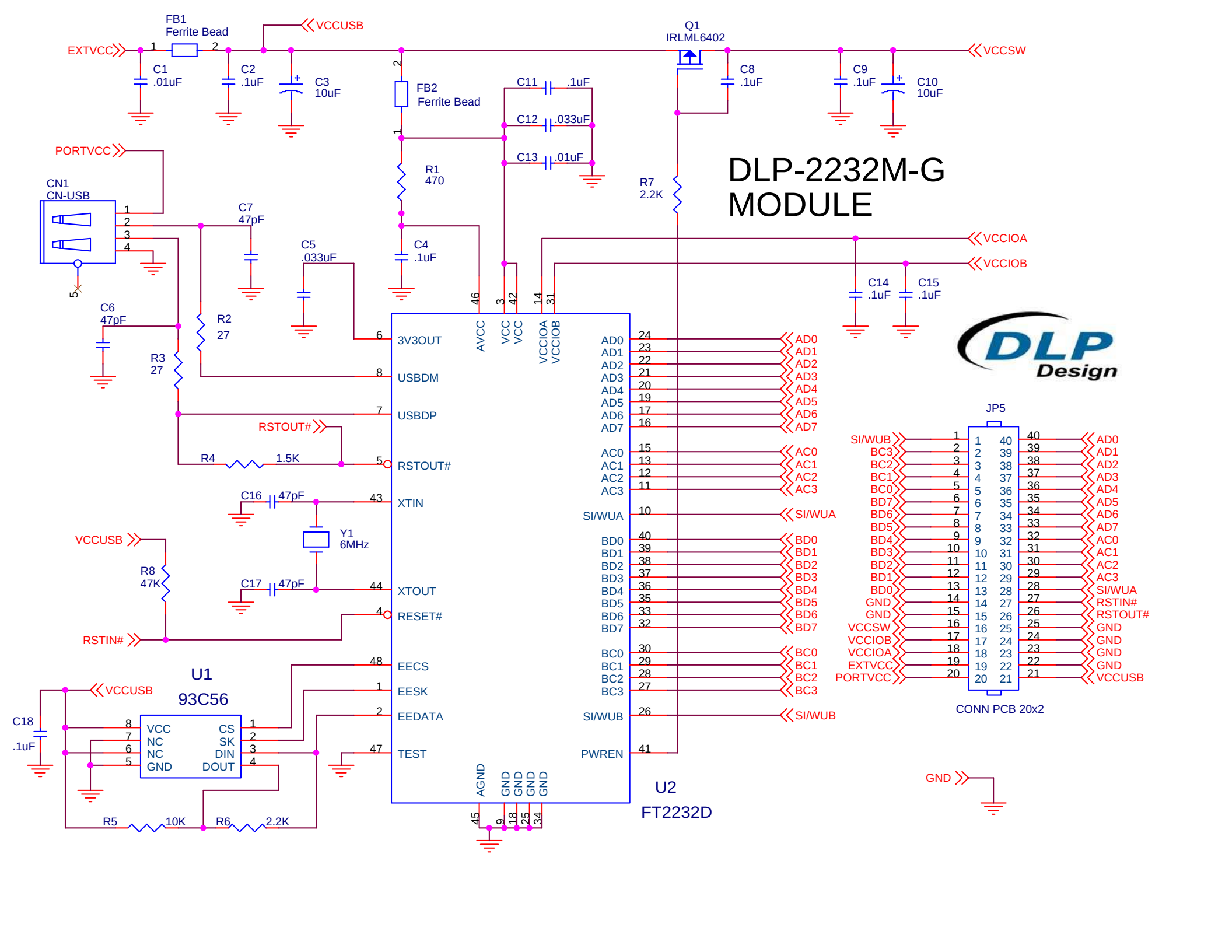
DLP-2232M-G
MODULE
FB1
Ferrite Bead
EXTVCC
VCCUSB
C1
.01uF
C2
.1uF
C3
10uF
FB2
Ferrite Bead
C11
.1uF
C12
.033uF
C13
.01uF
Q1
IRLML6402
C8
.1uF
C9
.1uF
C10
10uF
VCCSW
R1
470
R7
2.2K
PORTVCC
CN1
CN-USB
C7
47pF
C5
.033uF
C4
.1uF
VCCIOA
VCCIOB
C14
.1uF
C15
.1uF
C6
47pF
R2
27
R3
27
3V3OUT
USBDM
USBDP
RSTOUT#
R4
1.5K
RSTOUT#
C16
47pF
XTIN
Y1
6MHz
C17
47pF
XTOUT
VCCUSB
R8
47K
RESET#
RSTIN#
EECS
EESK
EEDATA
TEST
AVCC
VCC
VCC
VCCIOA
VCCIOB
AGND
GND
GND
GND
GND
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AC0
AC1
AC2
AC3
SI/WUA
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BC0
BC1
BC2
BC3
SI/WUB
PWREN
U2
FT2232D
JP5
CONN PCB 20x2
U1
93C56
VCC
NC
NC
GND
CS
SK
DIN
DOUT
C18
.1uF
R5
10K
R6
2.2K
GND