

# PRTR5V0U2X

Ultra low capacitance double rail-to-rail ESD protection diode

Rev. 02 — 14 January 2008

Product data sheet

## 1. Product profile

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### 1.1 General description

Ultra low capacitance rail-to-rail ElectroStatic Discharge (ESD) protection diode in a small SOT143B Surface-Mounted Device (SMD) plastic package designed to protect two Hi-Speed data lines or high-frequency signal lines from the damage caused by ESD and other transients.

PRTR5V0U2X incorporates two pairs of ultra low capacitance rail-to-rail diodes as well as an additional ESD protection diode to ensure signal line protection even if no supply voltage is available.

### 1.2 Features

- ESD protection of two Hi-Speed data lines or high-frequency signal lines
- Ultra low input/output to ground capacitance:  $C_{(I/O-GND)} = 1 \text{ pF}$
- ESD protection up to 8 kV
- IEC 61000-4-2, level 4 (ESD)
- Very low clamping voltage due to an integrated additional ESD protection diode
- Very low reverse current
- Small SMD plastic package

### 1.3 Applications

- USB 2.0 ports
- Digital Video Interface (DVI) / High Definition Multimedia Interface (HDMI) interfaces
- Mobile and cordless phones
- Personal Digital Assistants (PDA)
- Digital cameras
- Wide Area Network (WAN) / Local Area Network (LAN) systems
- PCs, notebooks, printers and other PC peripherals

### 1.4 Quick reference data

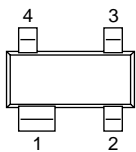
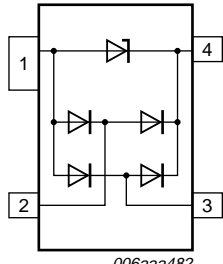
**Table 1. Quick reference data**  
*T<sub>amb</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per diode</b>						
V <sub>RWM</sub>	reverse standoff voltage		-	-	5.5	V
C <sub>(I/O-GND)</sub>	input/output to ground capacitance	f = 1 MHz; V <sub>(I/O-GND)</sub> = 0 V	[1]	1	1.5	pF
C <sub>sup</sub>	supply pin to ground capacitance	f = 1 MHz; V <sub>CC</sub> = 0 V	[2]	16	-	pF

- [1] Measured from pin 2 and 3 to ground.
- [2] Measured from pin 4 to ground.

## 2. Pinning information

**Table 2. Pinning**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND	ground		 <p style="text-align: center; font-size: small;">006aaa482</p>
2	I/O 1	input/output 1		
3	I/O 2	input/output 2		
4	V <sub>CC</sub>	supply voltage		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
PRTR5V0U2X	-	plastic surface-mounted package; 4 leads	SOT143B

## 4. Marking

**Table 4. Marking codes**

Type number	Marking code <sup>[1]</sup>
PRTR5V0U2X	*R1

- [1] \* = -: made in Hong Kong
- \* = p: made in Hong Kong
- \* = t: made in Malaysia
- \* = W: made in China

## 5. Limiting values

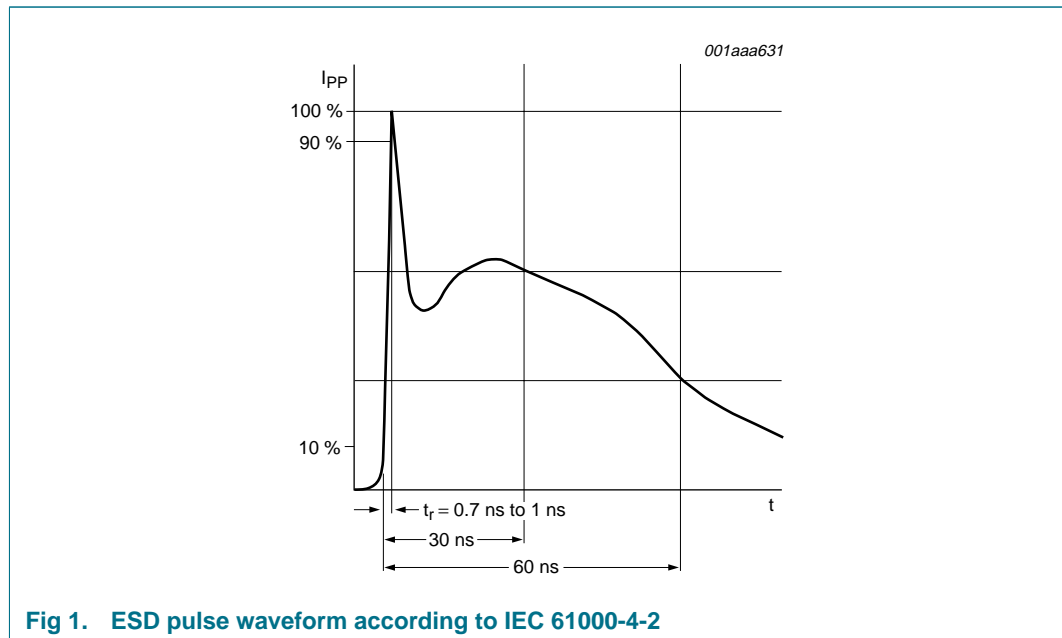
**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Per device</b>					
T <sub>amb</sub>	ambient temperature		-40	+85	°C
T <sub>stg</sub>	storage temperature		-55	+125	°C

**Table 6. ESD standards compliance**

Standard	Conditions
<b>Per diode</b>	
IEC 61000-4-2; level 4 (ESD)	> 8 kV (contact)



**Fig 1. ESD pulse waveform according to IEC 61000-4-2**

## 6. Characteristics

**Table 7. Characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

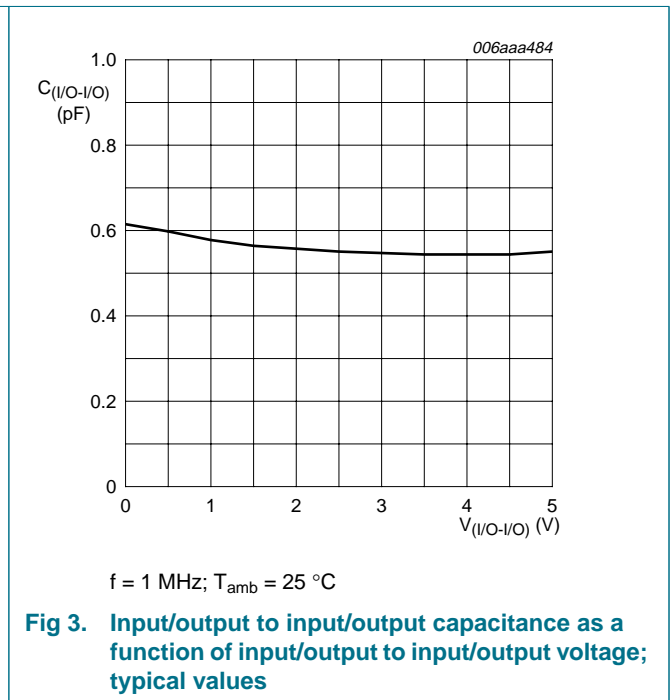
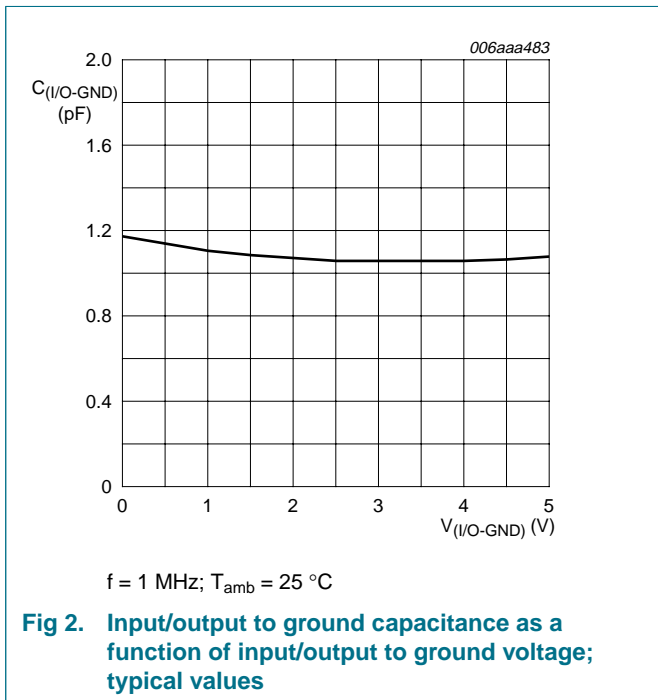
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Per diode</b>							
$V_{RWM}$	reverse standoff voltage		-	-	5.5	V	
$I_R$	reverse current	$V_R = 3\text{ V}$	[1]	< 1	100	nA	
$V_{BR}$	breakdown voltage		[2]	6	9	V	
$C_{(I/O-GND)}$	input/output to ground capacitance	$f = 1\text{ MHz};$ $V_{(I/O-GND)} = 0\text{ V}$	[3]	-	1	1.5	pF
$C_{(I/O-I/O)}$	input/output to input/output capacitance	$f = 1\text{ MHz};$ $V_{(I/O-I/O)} = 0\text{ V}$	[4]	-	0.6	-	pF
$C_{sup}$	supply pin to ground capacitance	$f = 1\text{ MHz};$ $V_{CC} = 0\text{ V}$	[2]	-	16	-	pF
$V_F$	forward voltage		-	0.7	-	V	

[1] Measured from pin 2, 3 and 4 to ground.

[2] Measured from pin 4 to ground.

[3] Measured from pin 2 and 3 to ground.

[4] Measured from pin 2 to pin 3.



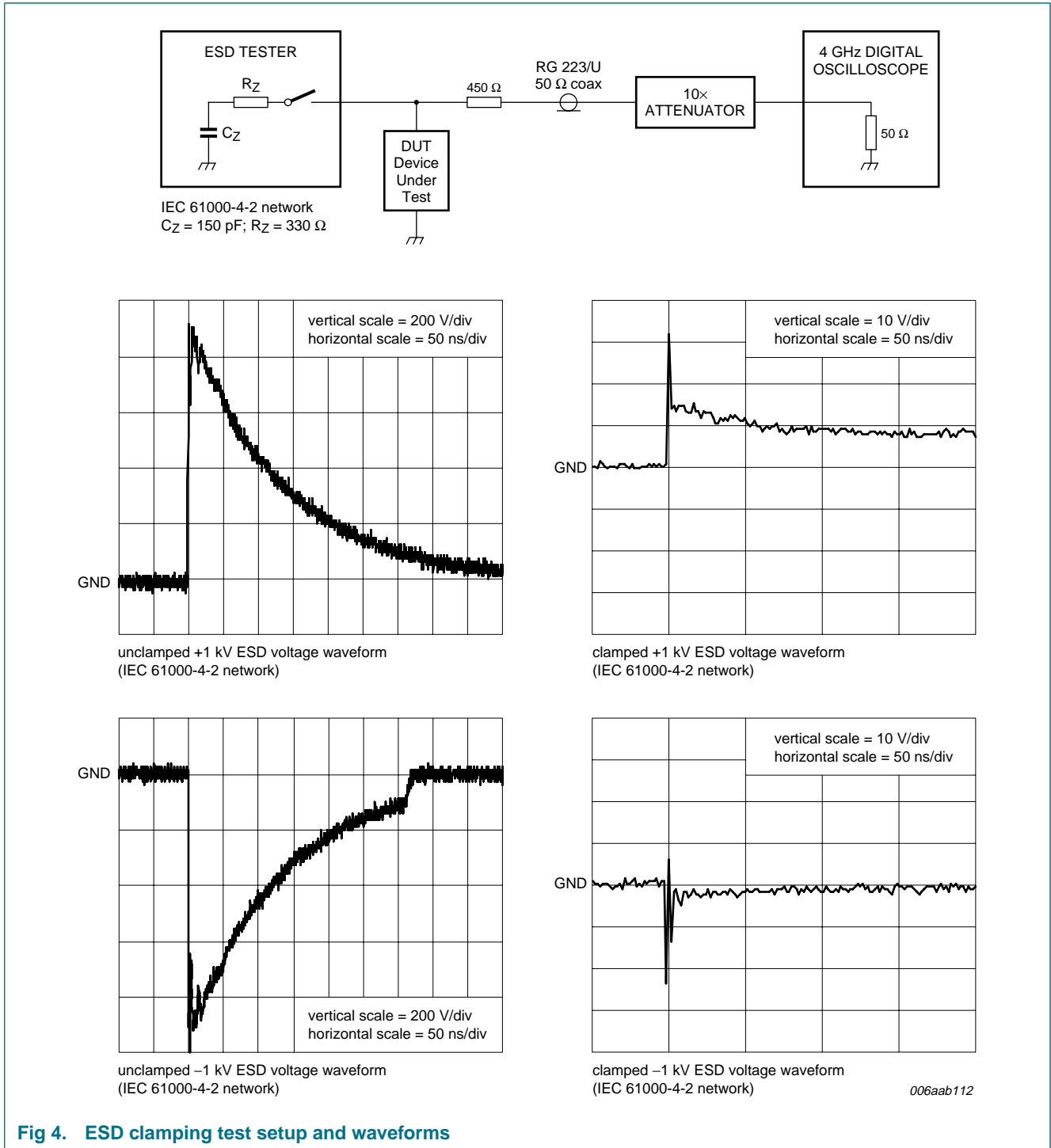


Fig 4. ESD clamping test setup and waveforms

## 7. Application information

Handling data rates up to 480 Mbit/s, USB 2.0 interfaces require ESD protection devices with an extremely low line capacitance in order to avoid signal distortion.

With a capacitance of only 1 pF, the PRTR5V0U2X offers IEC 61000-4-2, level 4 compliant ESD protection.

The PRTR5V0U2X integrates two pairs of ultra low capacitance rail-to-rail ESD protection diodes and an additional ESD protection diode.

The additional ESD protection diode connected between ground and  $V_{CC}$  prevents charging of the supply.

To achieve the maximum ESD protection level, no additional external capacitors are required.

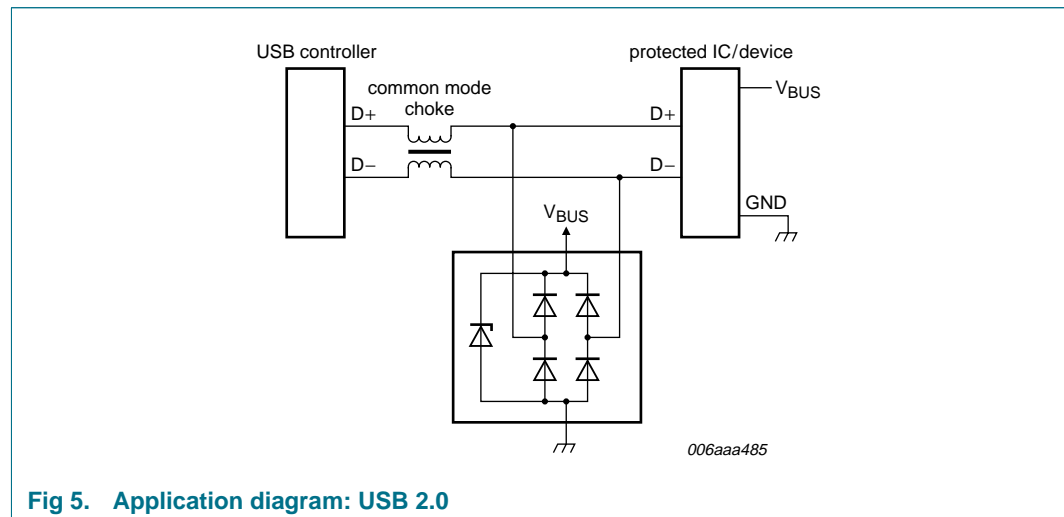


Fig 5. Application diagram: USB 2.0

### Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the PRTR5V0U2X as close to the input terminal or connector as possible.
2. The path length between the PRTR5V0U2X and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

## 8. Package outline

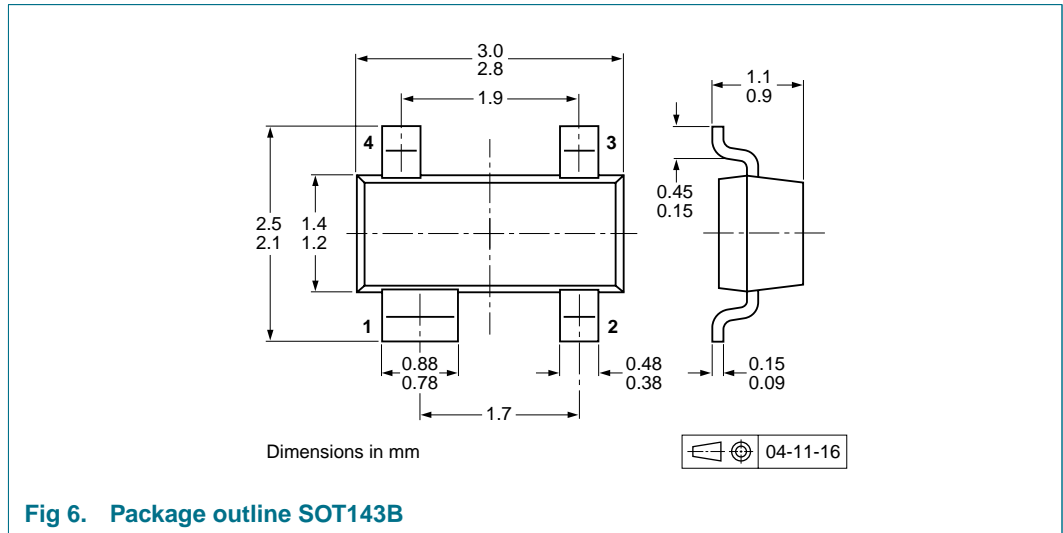


Fig 6. Package outline SOT143B

## 9. Packing information

**Table 8. Packing methods**

The indicated -xxx are the last three digits of the 12NC ordering code.<sup>[1]</sup>

Type number	Package	Description	Packing quantity	
			3000	10000
PRTR5V0U2X	SOT143B	4 mm pitch, 8 mm tape and reel	-215	-235

[1] For further information and the availability of packing methods, see [Section 13](#).

10. Soldering

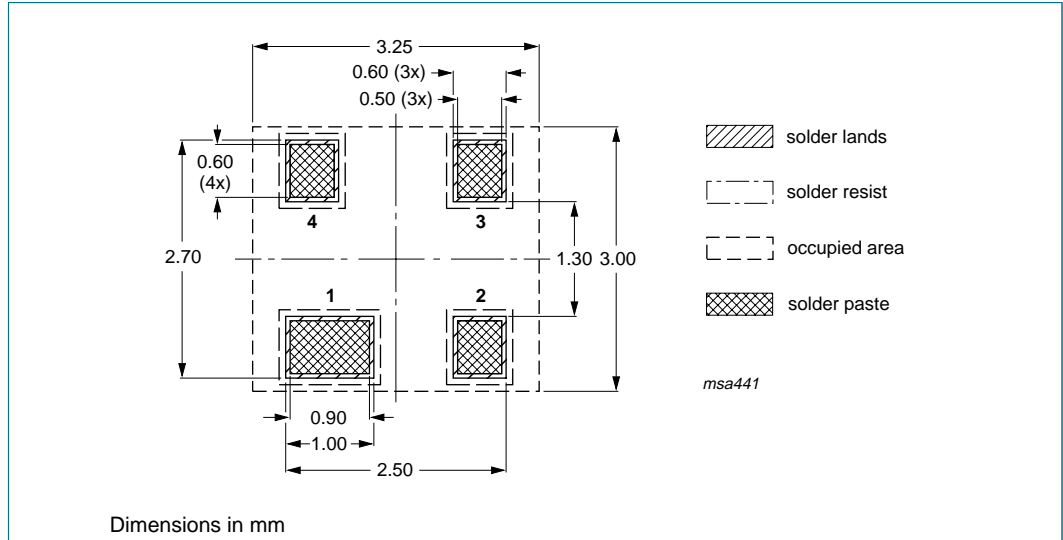


Fig 7. Reflow soldering footprint SOT143B

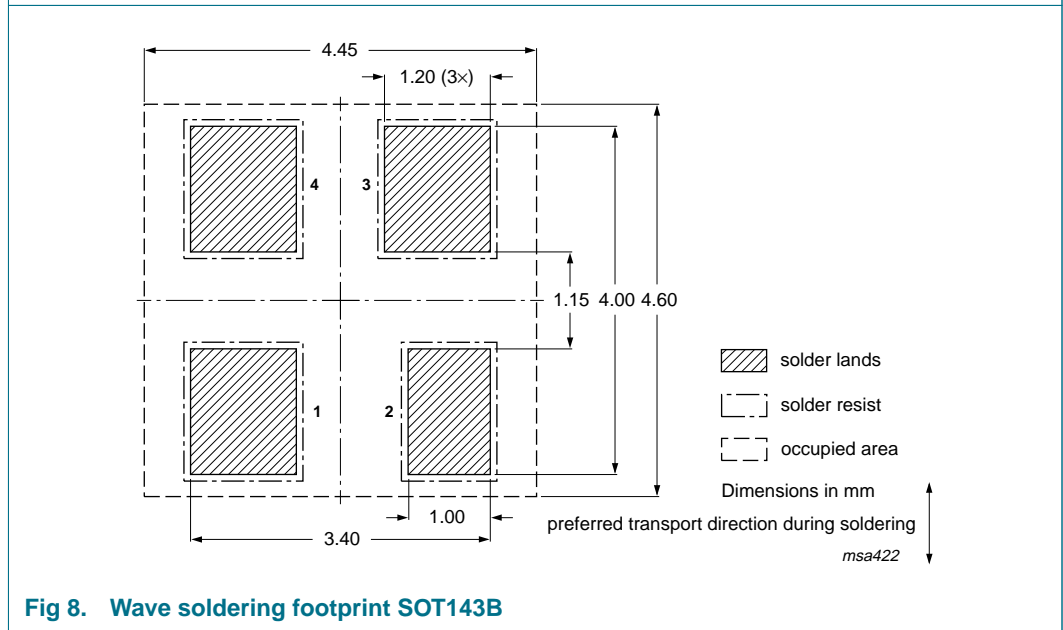


Fig 8. Wave soldering footprint SOT143B



## 11. Revision history

**Table 9.** Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PRTR5V0U2X_2	20080114	Product data sheet	-	PRTR5V0U2X_1
Modifications:		<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Table 1</a>: parameter for <math>C_{(I/O-GND)}</math> redefined to input/output to ground capacitance</li> <li>• <a href="#">Table 1 "Quick reference data"</a>: maximum value for <math>C_{(I/O-GND)}</math> added</li> <li>• <a href="#">Table 7</a>: parameter for <math>C_{(I/O-GND)}</math> redefined to input/output to ground capacitance</li> <li>• <a href="#">Table 7 "Characteristics"</a>: maximum value for <math>C_{(I/O-GND)}</math> added</li> <li>• <a href="#">Table 7</a>: parameter for <math>C_{(I/O-I/O)}</math> redefined to input/output to input/output capacitance</li> <li>• <a href="#">Table 7</a>: parameter for <math>C_{sup}</math> redefined to supply pin to ground capacitance</li> <li>• <a href="#">Section 10 "Soldering"</a>: added</li> <li>• <a href="#">Section 12 "Legal information"</a>: updated</li> </ul>		
PRTR5V0U2X_1	20050922	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 14. Contents

<b>1</b>	<b>Product profile</b> .....	<b>1</b>
1.1	General description .....	1
1.2	Features .....	1
1.3	Applications .....	1
1.4	Quick reference data .....	2
<b>2</b>	<b>Pinning information</b> .....	<b>2</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Marking</b> .....	<b>2</b>
<b>5</b>	<b>Limiting values</b> .....	<b>3</b>
<b>6</b>	<b>Characteristics</b> .....	<b>4</b>
<b>7</b>	<b>Application information</b> .....	<b>6</b>
<b>8</b>	<b>Package outline</b> .....	<b>7</b>
<b>9</b>	<b>Packing information</b> .....	<b>7</b>
<b>10</b>	<b>Soldering</b> .....	<b>8</b>
<b>11</b>	<b>Revision history</b> .....	<b>9</b>
<b>12</b>	<b>Legal information</b> .....	<b>10</b>
12.1	Data sheet status .....	10
12.2	Definitions .....	10
12.3	Disclaimers .....	10
12.4	Trademarks .....	10
<b>13</b>	<b>Contact information</b> .....	<b>10</b>
<b>14</b>	<b>Contents</b> .....	<b>11</b>

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