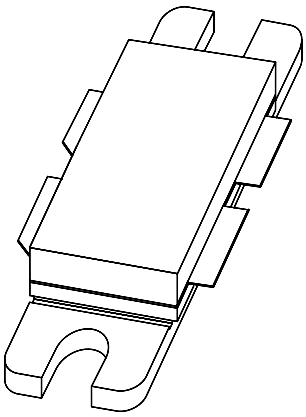
DISCRETE SEMICONDUCTORS

DATA SHEET



BLF647
UHF power LDMOS transistor

Product specification
Supersedes data of 2001 Aug 02

2001 Nov 27

Philips Semiconductors

PHILIPS

UHF power LDMOS transistor — BLF647

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (HF to 800 MHz)
- Internal input damping for excellent stability over the whole frequency range.

APPLICATIONS

- Communication transmitter applications in the HF to 800 MHz frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS push-pull transistor in a SOT540A package with ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT540A

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source, connected to flange

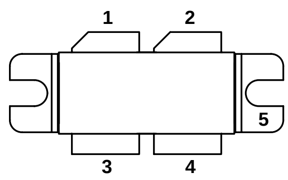


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB	600	28	120	>14.5	>55	–
2-tone, class-AB	f_1 = 600; f_2 = 600.1	28	120 (PEP)	>14.5	>40	≤–26

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	±15	V
I_D	drain current (DC)		–	18	A
P_{tot}	total power dissipation	T_{mb} ≤ 25 °C	–	290	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 290 W	0.6	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.2	K/W

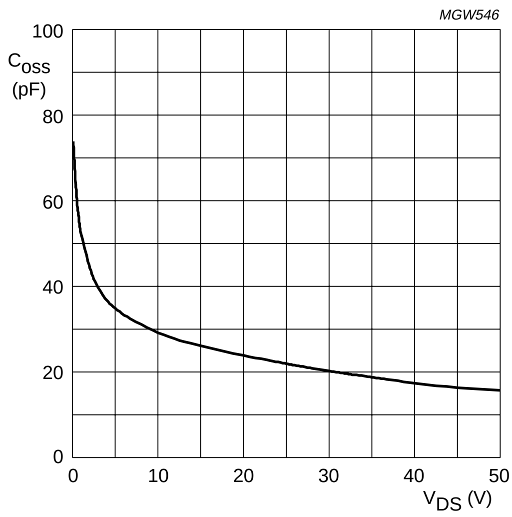
CHARACTERISTICS

T_j = 25 °C per section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 1.4 mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 20 V; I_D = 140 mA	4	–	5.5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	1.2	μA
I_{DSX}	drain cut-off current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	18	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	–	–	25	nA
g_{fs}	forward transconductance	V_{DS} = 20 V; I_D = 4 A	–	4	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = V_{GSth} + 9 V; I_D = 4 A	–	160	–	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz; note 1	–	80	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	43	–	pF
C_{rss}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	6	–	pF

Note

1. Capacitance values of the die only.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.2 Output capacitance as a function of drain-source voltage; typical values per section.

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ mb-h}$ = 0.2 K/W, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB	600	28	120	>14.5	>55	–
2-tone, class-AB	f_1 = 600; f_2 = 600.1	28	120 (PEP)	>14.5	>40	≤–26
CW, class-AB	800	32	150	typ. 12.5	typ. 60	–
2-tone, class-AB	f_1 = 800; f_2 = 800.1	32	150 (PEP)	typ. 13	typ. 45	typ. –30

Ruggedness in class-AB operation

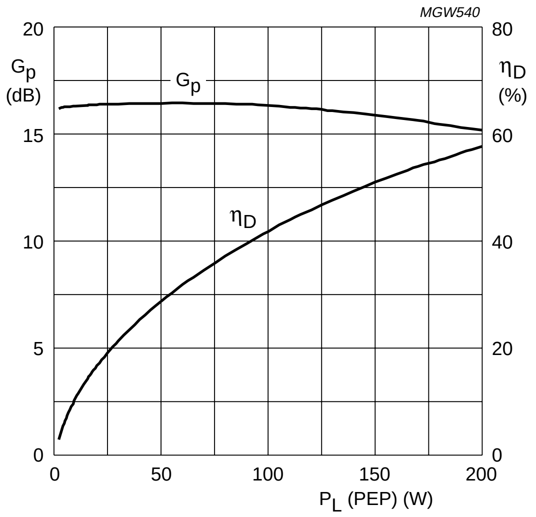
The BLF647 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; f = 100 MHz at rated load power.
The BLF647 is capable of withstanding abrupt source or load mismatch errors under the nominal power conditions.

Impedances (per section)

At f = 600 MHz, P_L = 120 W, V_{DS} = 28 V and I_{DQ} = 1 A: Z_{in} = 1.0 + j2.0 Ω and Z_L = 2.7 + j0.7 Ω.

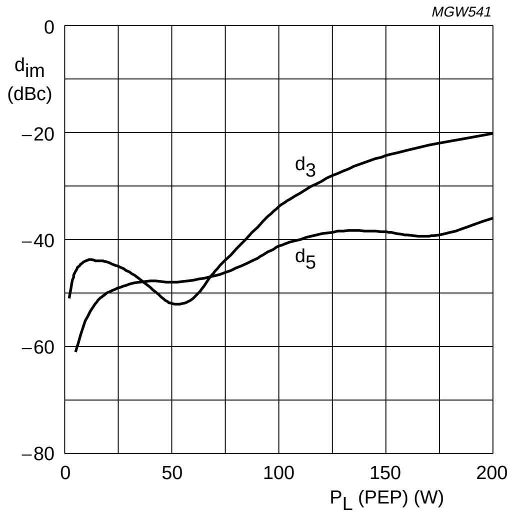
At f = 800 MHz, P_L = 150 W, V_{DS} = 32 V and I_{DQ} = 1 A: Z_{in} = 1.0 + j3.8 Ω and Z_L = 1.8 + j0.7 Ω.

Application at 600 MHz



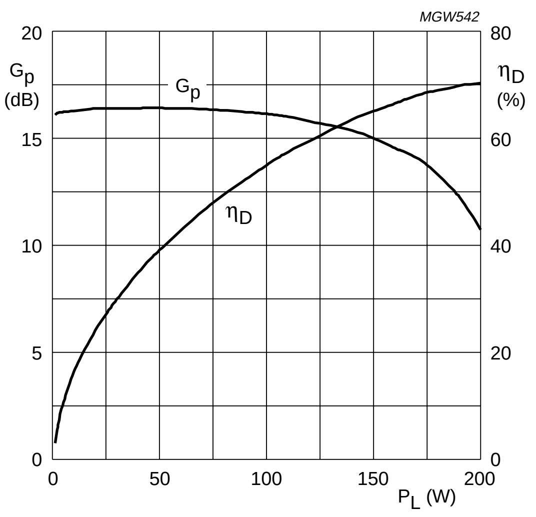
T_h = 25 °C; V_{DS} = 28 V; I_{DQ} = 1 A.
2-tone: f_1 = 600 MHz (–6 dB); f_2 = 600.1 MHz (–6 dB)
measured in 600 MHz test circuit.

Fig.3 Power gain and drain efficiency as functions of peak envelope load power; typical values.



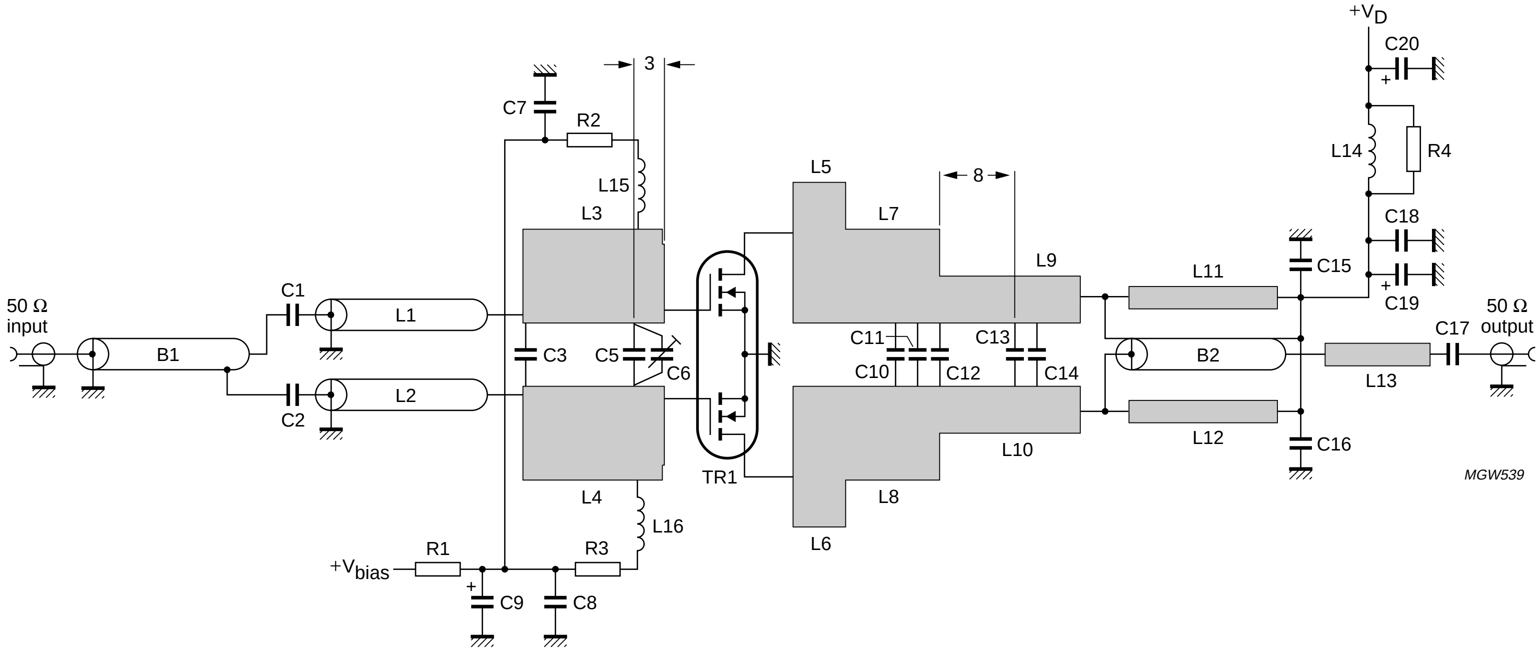
T_h = 25 °C; V_{DS} = 28 V; I_{DQ} = 1 A.
2-tone: f_1 = 600 MHz (–6 dB); f_2 = 600.1 MHz (–6 dB)
measured in 600 MHz test circuit.

Fig.4 Intermodulation distortion as a function of peak envelope output power; typical values.



T_h = 25 °C; V_{DS} = 28 V; I_{DQ} = 1 A; CW, class-AB; f = 600 MHz;
measured in 600 MHz test circuit.

Fig.5 Power gain and drain efficiency as functions of load power; typical values.



Dimensions in mm.

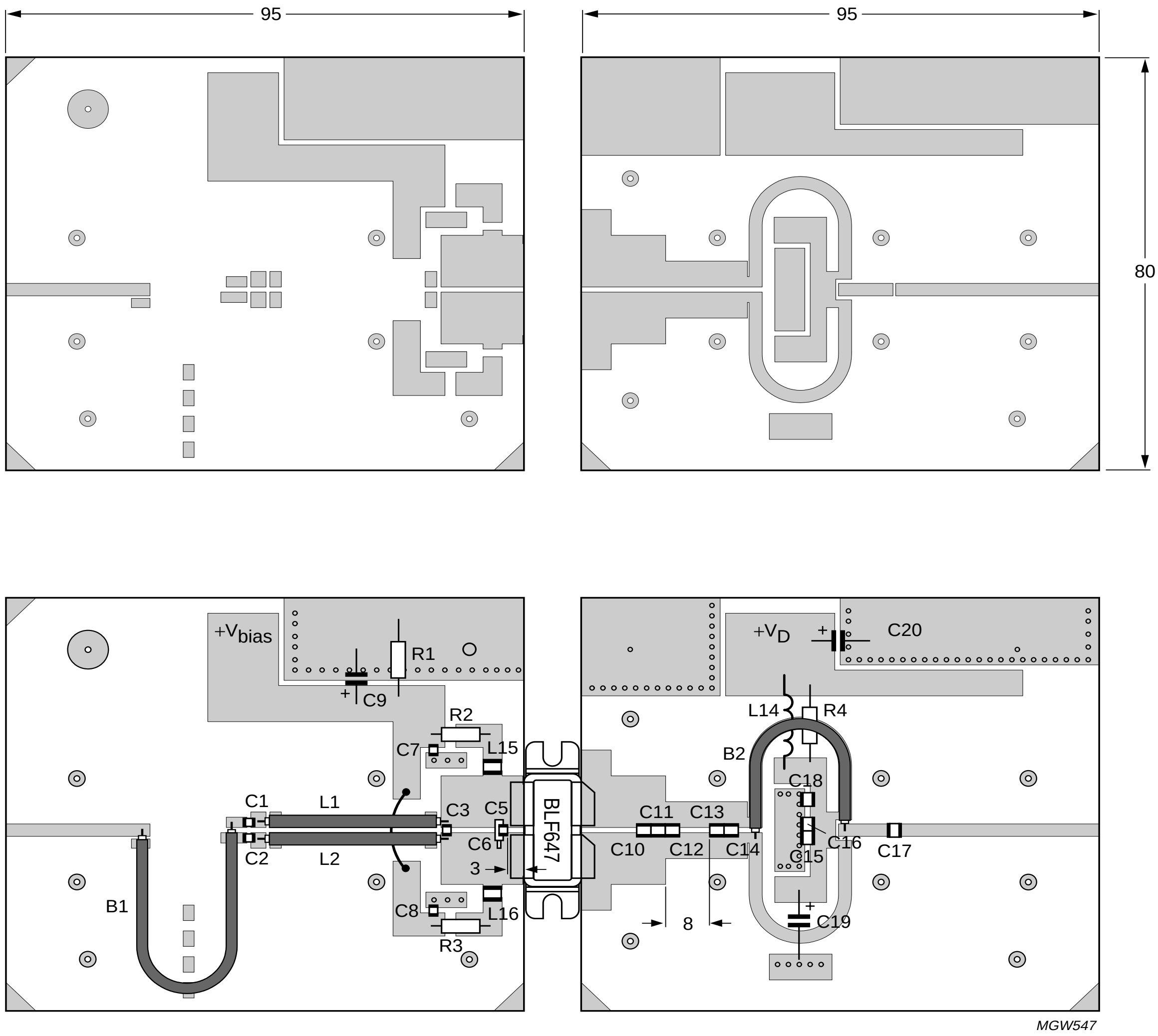
Fig.6 Class-AB common source 600 MHz test circuit.

List of components class-AB 600 MHz test circuit (see Figs 6 and 7)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2	multilayer ceramic chip capacitor; note 1	30 pF		
C3	multilayer ceramic chip capacitor; note 1	8.2 pF		
C5	multilayer ceramic chip capacitor; note 1	16 pF		
C6	Tekelec trimmer	0.6 to 7.5 pF		
C7, C8	multilayer ceramic chip capacitor; note 1	100 pF		
C9	electrolytic capacitor	10 μF		
C10	multilayer ceramic chip capacitor; note 2	2 pF		
C11, C12	multilayer ceramic chip capacitor; note 2	10 pF		
C13	multilayer ceramic chip capacitor; note 2	8.2 pF		
C14	multilayer ceramic chip capacitor; note 2	1.5 pF		
C15, C16, C17	multilayer ceramic chip capacitor; note 2	100 pF		
C18	SMD capacitor	1 μF		2222 595 16754
C19	electrolytic capacitor	470 μF		
C20	electrolytic capacitor	100 μF		
L1, L2	semi rigid coax UT70-25	Z = 25 Ω ±1.5 Ω	30.6 mm	
L3, L4	stripline; note 3		15 × 10 mm	
L5, L6	stripline; note 3		5.5 × 15 mm	
L7, L8	stripline; note 3		10 × 10 mm	
L9, L10	stripline; note 3		15 × 5 mm	
L11, L12	stripline; note 3		48.5 × 2.4 mm	
L13	stripline; note 3		10 × 2.4 mm	
L14	ferrite			
L15, L16	Coilcraft SMD coil 1008CS-102XKBC	1 μH		
B1	semi rigid coax (lambda/2)	Z = 50 Ω ±1.5 Ω	lambda/2	
B2	semi rigid coax balun UT70-25	Z = 25 Ω ±1.5 Ω	48.5 mm	
R1	resistor	1 kΩ		
R2, R3	resistor	100 Ω		
R4	resistor	3,3 Ω		

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 180R or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board: Rogers 5880 (ε_r = 2.2); thickness 0.79 mm.

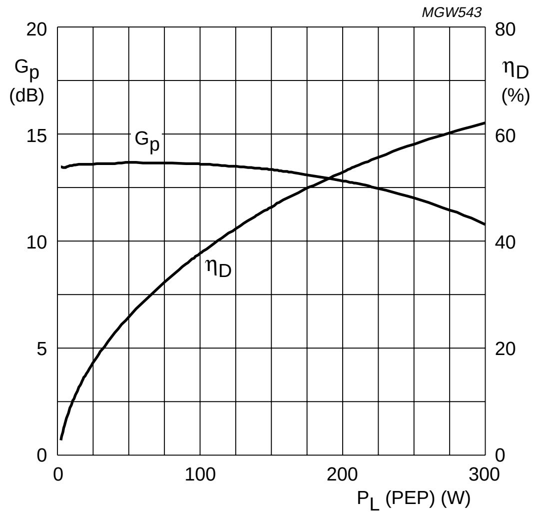


Dimensions in mm.

The components are situated on one side of the Rogers 5880 printed-circuit board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

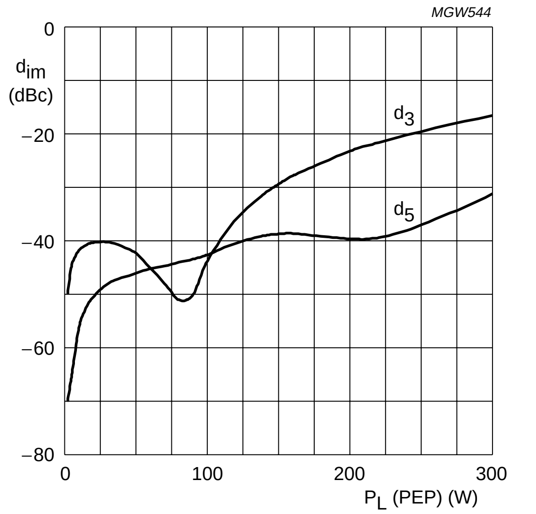
Fig.7 Printed-circuit board and component layout for class-AB 600 MHz test circuit.

Application at 800 MHz



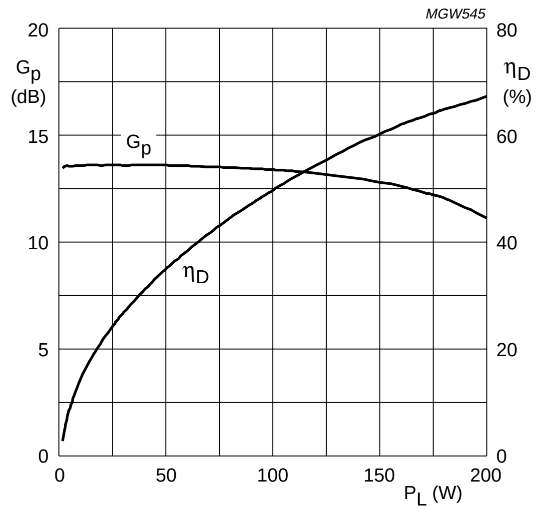
T_h = 25 °C; V_{DS} = 32 V; I_{DQ} = 1 A.
2-tone: f_1 = 800 MHz (–6 dB); f_2 = 800.1 MHz (–6 dB)
measured in 800 MHz test circuit.

Fig.8 Power gain and drain efficiency as functions of peak envelope load power; typical values.



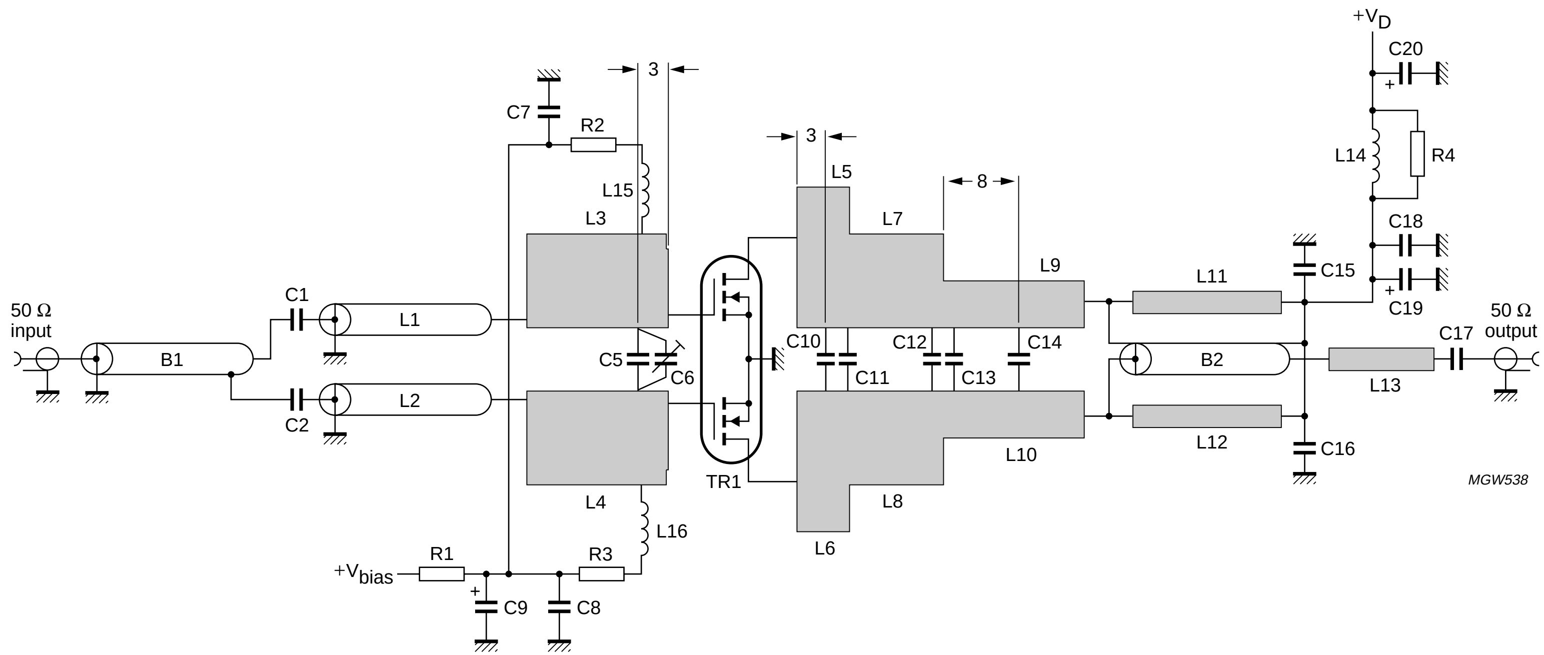
T_h = 25 °C; V_{DS} = 32 V; I_{DQ} = 1 A.
2-tone: f_1 = 800 MHz (–6 dB); f_2 = 800.1 MHz (–6 dB)
measured in 800 MHz test circuit.

Fig.9 Intermodulation distortion as a function of peak envelope output power; typical values.



T_h = 25 °C; V_{DS} = 32 V; I_{DQ} = 1 A; CW, class-AB; f = 800 MHz;
measured in 800 MHz test circuit.

Fig.10 Power gain and drain efficiency as functions of load power; typical values.



Dimensions in mm.

Fig.11 Class-AB common source 800 MHz test circuit.

List of components class-AB 800 MHz test circuit (see Figs 11 and 12)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2	multilayer ceramic chip capacitor; note 1	30 pF		
C5	multilayer ceramic chip capacitor; note 1	10 pF		
C6	tekelec trimmer	0.6 to 7.5 pF		
C7, C8	multilayer ceramic chip capacitor; note 1	100 pF		
C9	electrolytic capacitor	10 μF		
C10, C11	multilayer ceramic chip capacitor; note 2	8.2 pF		
C12, C13	multilayer ceramic chip capacitor; note 2	10 pF		
C14	multilayer ceramic chip capacitor; note 2	4.7 pF		
C15, C16	multilayer ceramic chip capacitor; note 2	100 pF		
C17	multilayer ceramic chip capacitor; note 2	20 pF		
C18	SMD capacitor	1 μF		2222 595 16754
C19	electrolytic capacitor	470 μF		
C20	electrolytic capacitor	100 μF		
L1, L2	semi rigid coax UT70-25	Z = 25 Ω ±1.5 Ω	30.6 mm	
L3, L4	stripline; note 3		15 × 10 mm	
L5, L6	stripline; note 3		5.5 × 15 mm	
L7, L8	stripline; note 3		10 × 10 mm	
L9, L10	stripline; note 3		15 × 5 mm	
L11, L12	stripline; note 3		48.5 × 2.4 mm	
L13	stripline; note 3		10 × 2.4 mm	
L14	ferrite			
L15, L16	Coilcraft SMD coil 1008CS-102XKBC	1 μH		
B1	semi rigid coax (lambda/2)	Z = 50 Ω ±1.5 Ω	lambda/2	
B2	semi rigid coax balun UT70-25	Z = 25 Ω ±1.5 Ω	48.5 mm	
R1	resistor	1 kΩ		
R2, R3	resistor	100 Ω		
R4	resistor	3,3 Ω		

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
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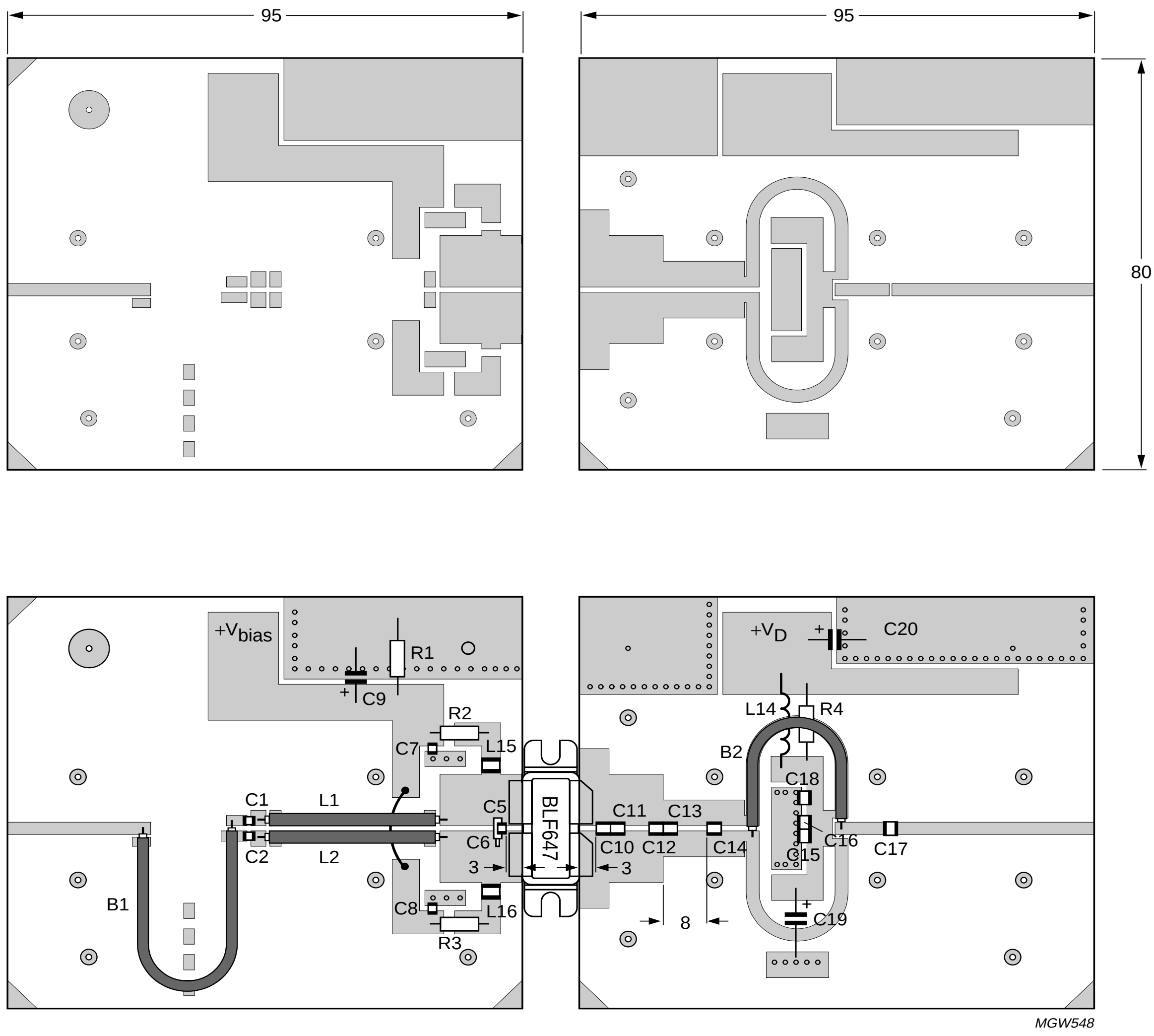
3. The striplines are on a double copper-clad printed-circuit board: Rogers 5880 (ε_r = 2.2); thickness 0.79 mm.



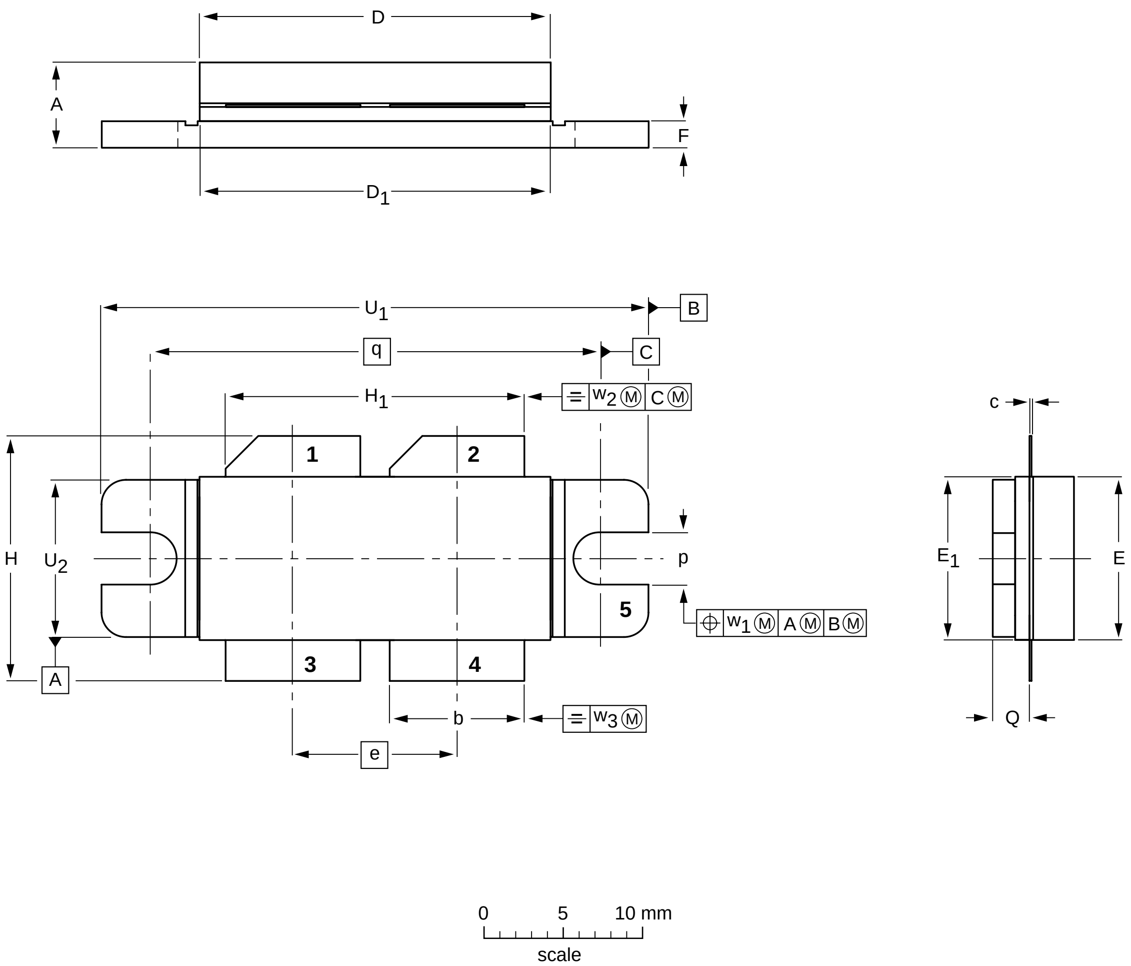
Dimensions in mm.

The components are situated on one side of the Rogers 5880 printed-circuit board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.12 Printed-circuit board and component layout for class-AB 800 MHz test circuit.

PACKAGE OUTLINE

Flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads **SOT540A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.77 5.00	8.51 8.26	0.15 0.10	22.05 21.64	22.05 21.64	10.21	10.26 10.06	10.31 10.01	1.78 1.52	15.75 14.73	18.72 18.47	3.38 3.12	2.72 2.46	27.94	34.16 33.91	9.91 9.65	0.25	0.51	0.25
inches	0.227 0.197	0.335 0.325	0.006 0.004	0.868 0.852	0.868 0.852	0.402	0.404 0.396	0.406 0.394	0.070 0.060	0.620 0.580	0.737 0.727	0.133 0.123	0.107 0.097	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT540A						~~99-08-27~~ 99-12-28

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
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