

BLL6H0514-25

LDMOS driver transistor

Rev. 04 — 30 March 2010

Product data sheet

1. Product profile

1.1 General description

25 W LDMOS transistor intended for pulsed applications in the 0.5 GHz to 1.4 GHz range.

Table 1. Application information

Typical RF performance at $T_{case} = 25\text{ °C}$; $I_{DQ} = 50\text{ mA}$; in a class-AB application circuit.

Mode of operation	f (MHz)	t _p (μs)	δ (%)	V _{DS} (V)	P _L (W)	G _p (dB)	RL _{in} (dB)	η _D (%)	P _{droop(pulse)} (dB)	t _r (ns)	t _f (ns)
pulsed RF	960 to 1215	128	10	50	25	21	10	58	0.05	8	6
	1200 to 1400	300	10	50	25	19	10	50	0.05	8	6

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (0.5 GHz to 1.4 GHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

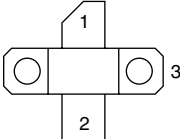
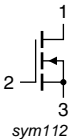
1.3 Applications

- Amplifiers for pulsed applications in the 0.5 GHz to 1.4 GHz frequency range



2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLL6H0514-25	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT467C

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	100	V
V_{GS}	gate-source voltage		-0.5	+13	V
I_D	drain current		-	2.5	A
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_{case} = 85\text{ °C}; P_L = 25\text{ W}$		
		$t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ %}$	0.86	K/W
		$t_p = 200\text{ }\mu\text{s}; \delta = 10\text{ %}$	1.11	K/W
		$t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ %}$	1.29	K/W
		$t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ %}$	1.15	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ }^\circ\text{C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 630\text{ mA}$	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 18\text{ mA}$	1.4	1.9	2.4	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$	-	-	1	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	2.1	2.5	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	100	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 18\text{ mA}$	120	150	-	mS
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 63\text{ mA}$	-	1500	2750	$\text{m}\Omega$

Table 7. RF characteristics

Mode of operation: pulsed RF; $t_p = 128\text{ }\mu\text{s}$; $\delta = 10\%$; RF performance at $V_{DS} = 50\text{ V}$; $I_{DQ} = 50\text{ mA}$; $f = 1.2\text{ GHz}$; $T_{case} = 25\text{ }^\circ\text{C}$; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_L	output power		25	-	-	W
V_{DS}	drain-source voltage	$P_L = 25\text{ W}$	-	-	50	V
G_p	power gain	$P_L = 25\text{ W}$	20	21	-	dB
RL_{in}	input return loss	$P_L = 25\text{ W}$	10	15	-	dB
η_D	drain efficiency	$P_L = 25\text{ W}$	57	59	-	%
$P_{\text{droop(pulse)}}$	pulse droop power	$P_L = 25\text{ W}$	-	0	0.3	dB
t_r	rise time	$P_L = 25\text{ W}$	-	20	50	ns
t_f	fall time	$P_L = 25\text{ W}$	-	6	50	ns

6.1 Ruggedness in class-AB operation

The BLL6H0514-25 is capable of withstanding a load mismatch corresponding to $V_{SWR} = 10 : 1$ through all phases under the following conditions: $V_{DS} = 50\text{ V}$; $I_{DQ} = 50\text{ mA}$; $P_L = 25\text{ W}$; $f = 1.2\text{ GHz}$; $t_p = 128\text{ }\mu\text{s}$; $\delta = 10\%$.

7. Application information

7.1 Impedance information

Table 8. Typical impedance

Typical values per section unless otherwise specified.

f	Z _S	Z _L
MHz	Ω	Ω
950	2.37 + j3.3	6.11 + j11.1
1000	2.44 + j2.65	7.00 + j16.0
1050	2.34 + j2.67	7.39 + j14.2
1100	2.56 + j2.06	7.0 + j16.0
1150	2.54 + j1.70	5.77 + j13.85
1200	2.25 + j1.29	7.39 + j14.2
1300	2.21 + j0.15	6.11 + j11.1
1400	2.46 – j0.52	5.00 + j10.0

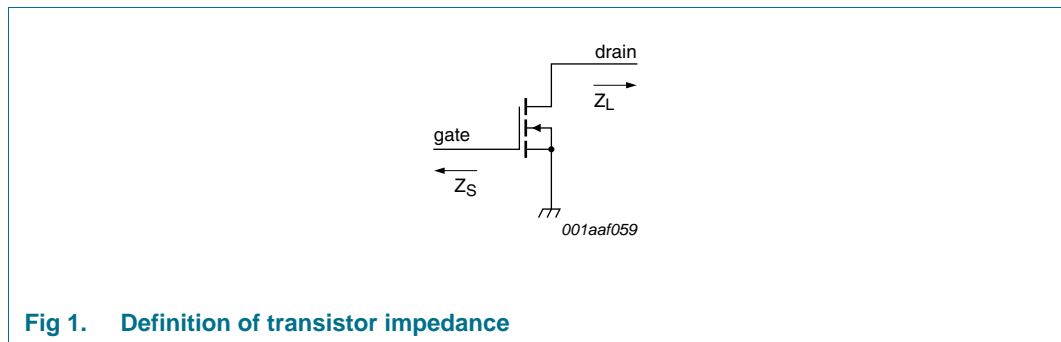


Fig 1. Definition of transistor impedance

7.2 Typical data

Table 9. Application information

Typical RF performance at $T_{case} = 25\text{ °C}$; $I_{DQ} = 50\text{ mA}$; in a class-AB application circuit.

Mode of operation	f	t _p	δ	V _{DS}	P _L	G _p	RL _{in}	η _D	P _{droop(pulse)}	t _r	t _f
	(MHz)	(μs)	(%)	(V)	(W)	(dB)	(dB)	(%)	(dB)	(ns)	(ns)
pulsed RF	960 to 1215	128	10	50	25	21	10	58	0.05	8	6
	1200 to 1400	300	10	50	25	19	10	50	0.05	8	6

7.3 Application circuit

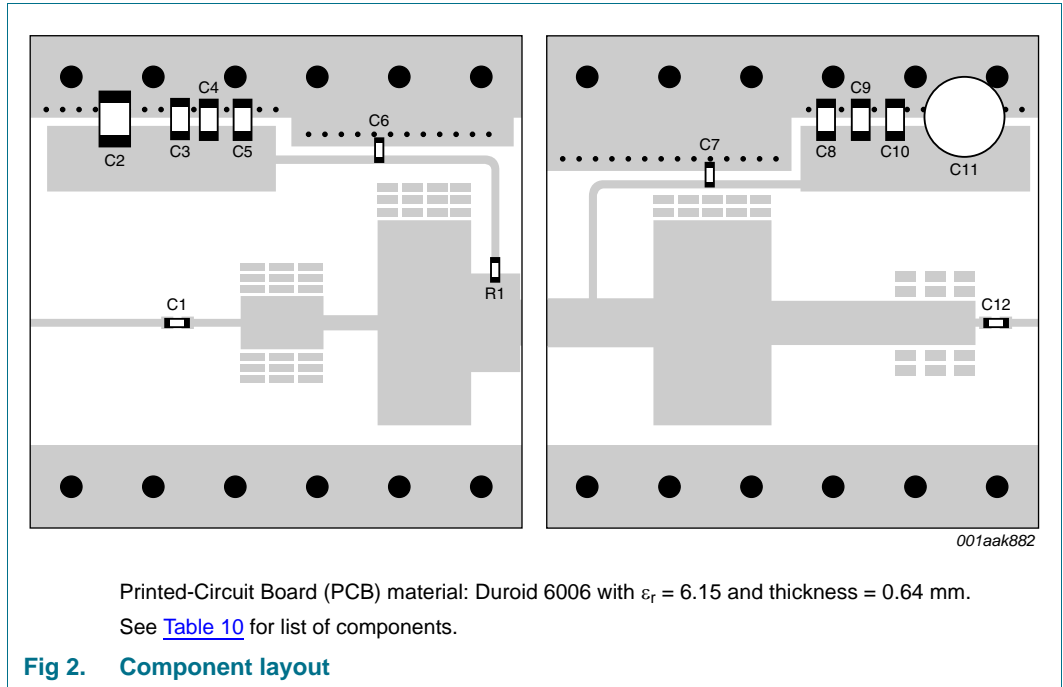


Table 10. List of components

See [Figure 2](#) for component layout.

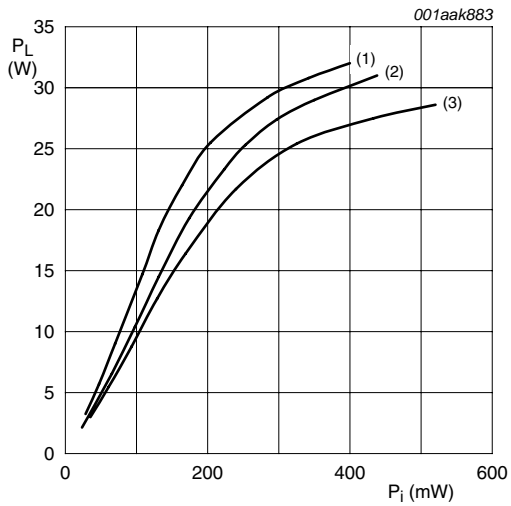
Component	Description	Value	Remarks
C1, C6, C7, C12	multilayer ceramic chip capacitor	56 pF	[1]
C2	multilayer ceramic chip capacitor	10 μ F; 25 V	
C3, C4, C8, C9	multilayer ceramic chip capacitor	100 pF	[1]
C5, C10	multilayer ceramic chip capacitor	1 nF	[2]
C11	electrolytic capacitor	68 μ F; 63 V	
R1	SMD resistor	10 Ω	SMD 0603

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

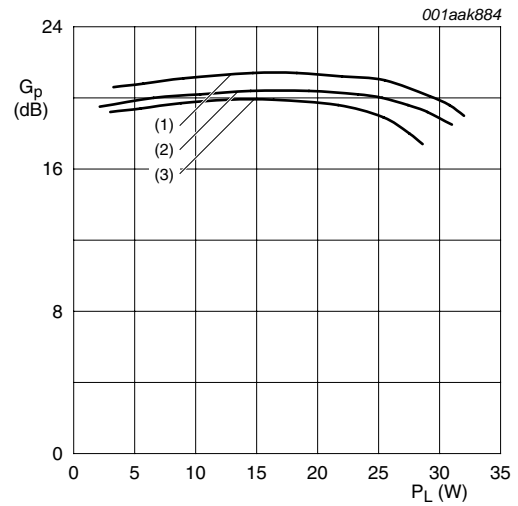
8. Test information

8.1 Performance curves



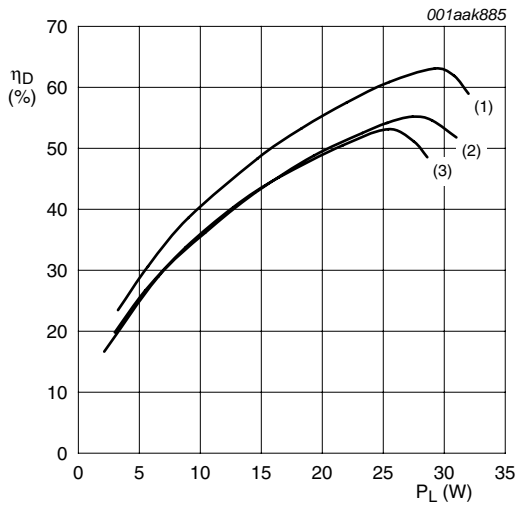
$V_{DS} = 50\text{ V}; I_{Dq} = 50\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$.
 (1) $f = 1200\text{ MHz}$
 (2) $f = 1300\text{ MHz}$
 (3) $f = 1400\text{ MHz}$

Fig 3. Load power as a function of input power; typical values



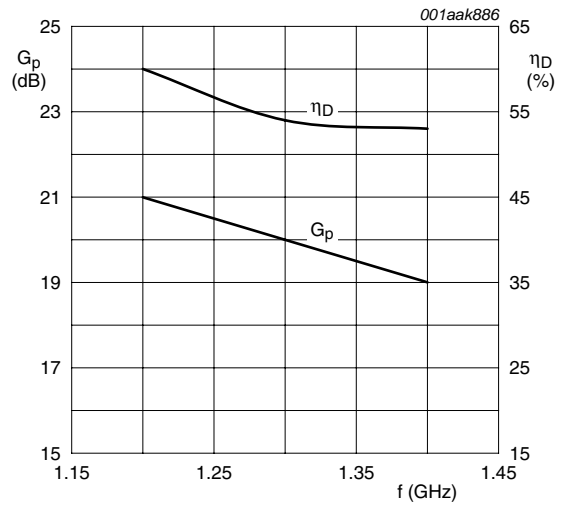
$V_{DS} = 50\text{ V}; I_{Dq} = 50\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$.
 (1) $f = 1200\text{ MHz}$
 (2) $f = 1300\text{ MHz}$
 (3) $f = 1400\text{ MHz}$

Fig 4. Power gain as a function of load power; typical values



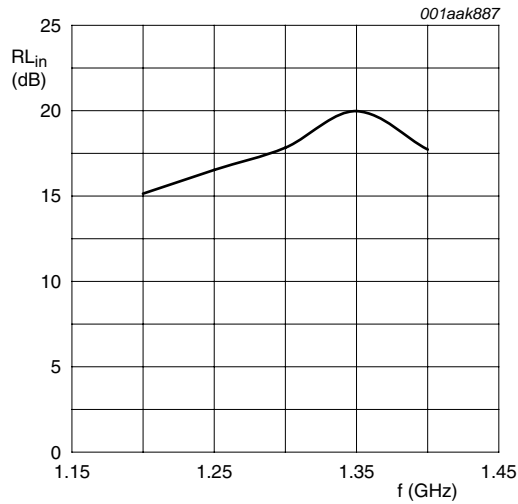
$V_{DS} = 50\text{ V}; I_{DQ} = 50\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$.
 (1) $f = 1200\text{ MHz}$
 (2) $f = 1300\text{ MHz}$
 (3) $f = 1400\text{ MHz}$

Fig 5. Drain efficiency as a function of load power; typical values



$V_{DS} = 50\text{ V}; I_{DQ} = 50\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$.

Fig 6. Power gain and drain efficiency as function of frequency; typical values



$P_L = 25\text{ W}; V_{DS} = 50\text{ V}; I_{DQ} = 50\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$.

Fig 7. Input return loss as a function of frequency; typical values

9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT467C

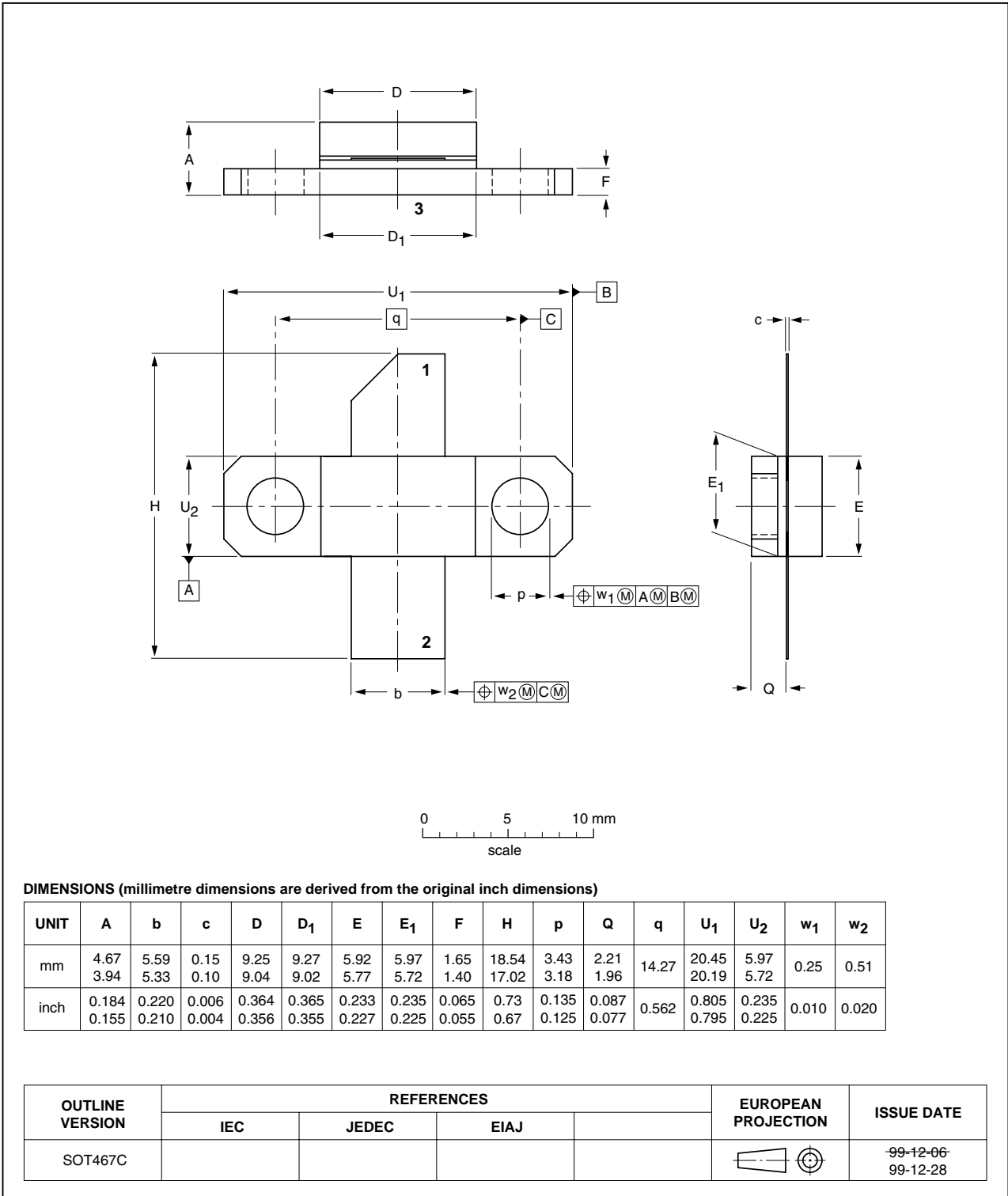


Fig 8. Package outline SOT467C

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLL6H0514-25_4	20100330	Product data sheet	-	BLL6H0514-25_3
Modifications:	• Figure 3 on page 6 : the unit on the X-axis is corrected to mW.			
BLL6H0514-25_3	20100223	Product data sheet	-	BLL6H0514-25_2
BLL6H0514-25_2	20090317	Objective data sheet	-	BLL6H0514-25_1
BLL6H0514-25_1	20090305	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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