

BSH114

N-channel enhancement mode field effect transistor

Rev. 01 — 09 November 2000

Product specification

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using **TrenchMOS™¹** technology.

Product availability:
BSH114 in SOT23.

2. Features

- TrenchMOS™ technology
- Low on-state resistance
- Very fast switching
- Surface mount package.

3. Applications

- Relay driver
- DC to DC converter
- General purpose switch.

4. Pinning information

Table 1: Pinning - SOT23, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	<p>Top view MSB003</p>	<p>MBB076</p>
2	source (s)		
3	drain (d)		

SOT23

1. TrenchMOS is a trademark of Royal Philips Electronics.



5. Quick reference data

Table 2: Quick reference data

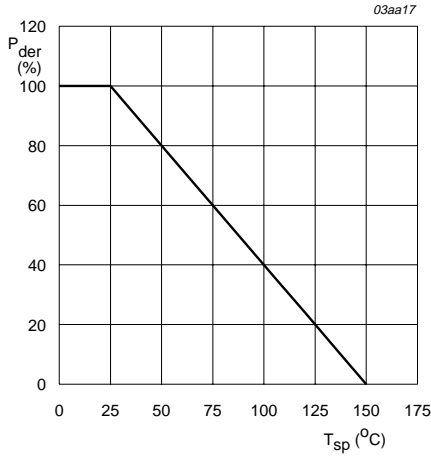
Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 150 °C	–	100	V
I_D	drain current (DC)	$T_{sp} = 25$ °C; $V_{GS} = 10$ V	–	0.85	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C	–	0.83	W
T_j	junction temperature		–	150	°C
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 0.5$ A	400	500	mΩ

6. Limiting values

Table 3: Limiting values

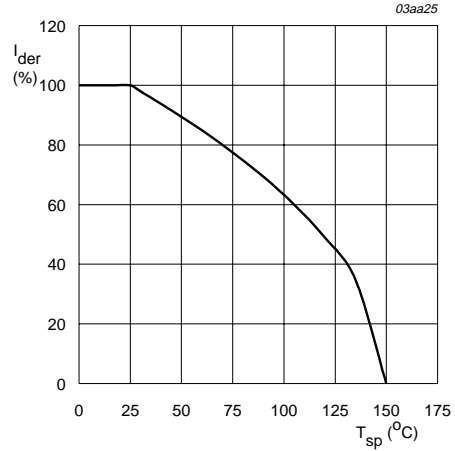
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 150 °C	–	100	V
V_{DGR}	drain-gate voltage (DC)	$T_j = 25$ to 150 °C; $R_{GS} = 20$ kΩ	–	100	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	$T_{sp} = 25$ °C; $V_{GS} = 10$ V; Figure 2 and 3	–	0.85	A
		$T_{sp} = 100$ °C; $V_{GS} = 10$ V; Figure 2 and 3	–	0.5	A
		$T_{amb} = 25$ °C; $V_{GS} = 10$ V	–	0.5	A
		$T_{amb} = 100$ °C; $V_{GS} = 10$ V	–	0.3	A
I_{DM}	peak drain current	$T_{sp} = 25$ °C; $t_p \leq 10$ μs; Figure 3	–	3.4	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C; Figure 1	–	0.83	W
		$T_{amb} = 25$ °C	–	0.36	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain (reverse) diode					
I_S	source (diode forward) current (DC)	$T_{sp} = 25$ °C	–	0.85	A
I_{SM}	peak (diode forward) source current	$T_{sp} = 25$ °C; $t_p \leq 10$ μs	–	3.4	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

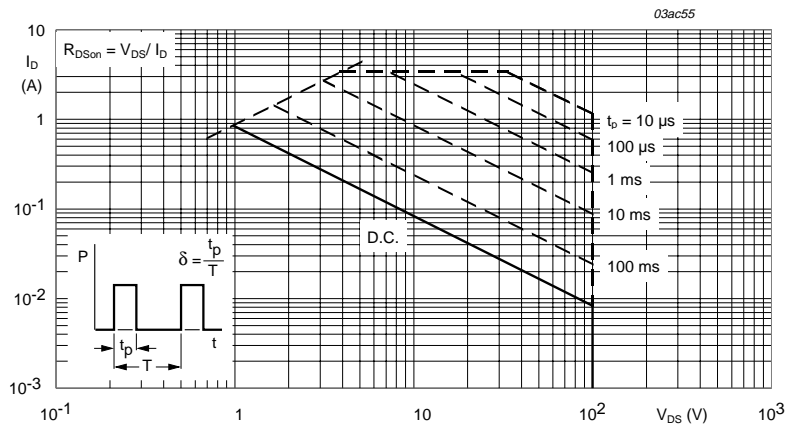
Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$V_{GS} \geq 10 \text{ V}$$

$$I_D = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



T_{sp} = 25 °C; I_{DM} is single pulse

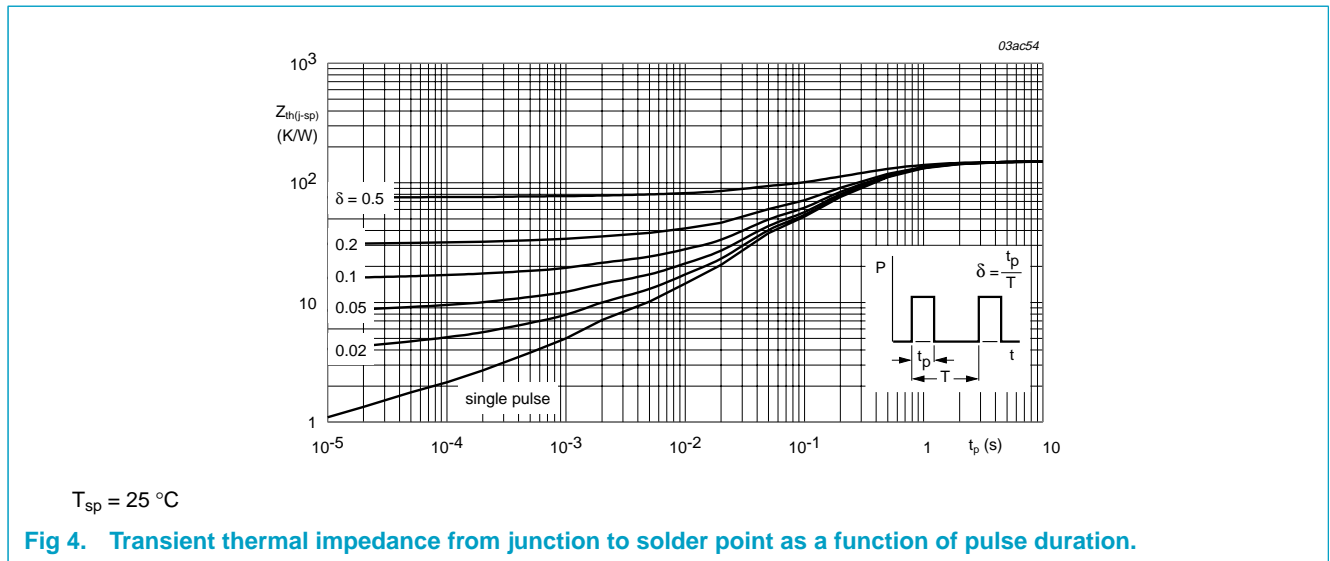
Fig 3. Safe operating area; drain and peak currents as a function of drain source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on a metal clad substrate; Figure 4	150	K/W
$R_{th(j-amb)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; minimum footprint	350	K/W

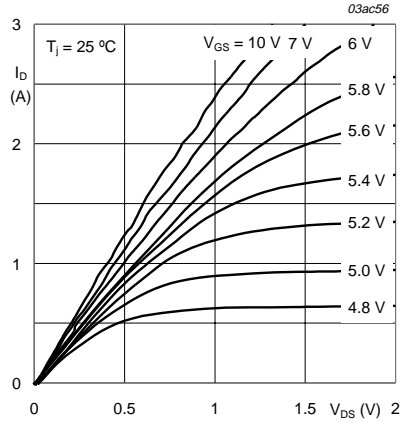
7.1 Transient thermal impedance



8. Characteristics

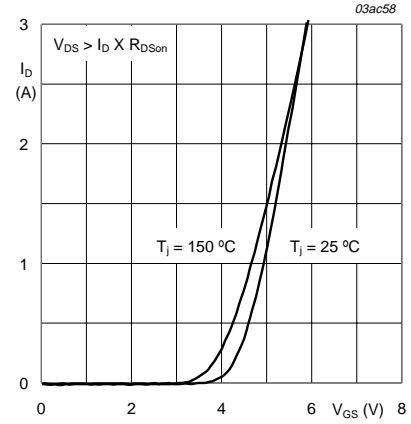
Table 5: Characteristics
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V T _j = 25 °C	100	130	–	V
		T _j = –55 °C	95	–	–	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9 T _j = 25 °C	2	3	4	V
		T _j = 150 °C	1.2	–	–	V
		T _j = –55 °C	–	–	6	V
I _{DSS}	drain-source leakage current	V _{DS} = 100 V; V _{GS} = 0 V T _j = 25 °C	–	1	25	μA
		T _j = 150 °C	–	4	250	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±20 V; V _{DS} = 0 V	–	10	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 0.5 A; Figure 7 and 8 T _j = 25 °C	–	400	500	mΩ
		T _j = 150 °C	–	–	1.15	Ω
Dynamic characteristics						
g _{fs}	forward transconductance	V _{DS} = 20 V; I _D = 0.5 A; Figure 11	0.5	1.2	–	S
Q _{g(tot)}	total gate charge	I _D = 0.5 A; V _{DD} = 80 V; V _{GS} = 10 V; Figure 14	–	4.6	–	nC
Q _{gs}	gate-source charge		–	0.8	–	nC
Q _{gd}	gate-drain (Miller) charge		–	2.1	–	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DD} = 25 V; f = 1 MHz; Figure 12	–	138	–	pF
C _{oss}	output capacitance		–	21	–	pF
C _{rss}	reverse transfer capacitance		–	12	–	pF
t _{d(on)}	turn-on delay time	V _{DD} = 50 V; R _D = 100 Ω; V _{GS} = 10 V; R _G = 6 Ω	–	6	–	ns
t _r	rise time		–	13	–	ns
t _{d(off)}	turn-off delay time		–	8	–	ns
t _f	fall time		–	5	–	ns
Source-drain (reverse) diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 0.85 A; V _{GS} = 0 V; Figure 13	–	0.84	1	V
t _{rr}	reverse recovery time	I _S = 0.5 A; di _S /dt = –100 A/μs;	–	24	–	ns
Q _r	recovered charge	V _{GS} = 0 V; V _{DS} = 30 V	–	37	–	nC



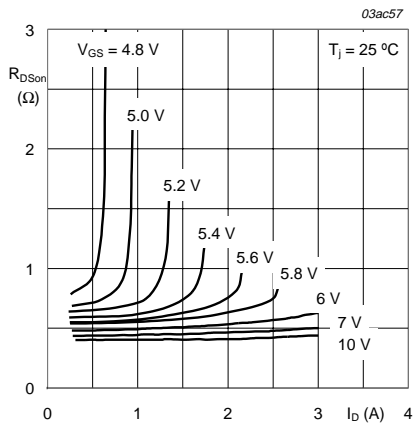
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



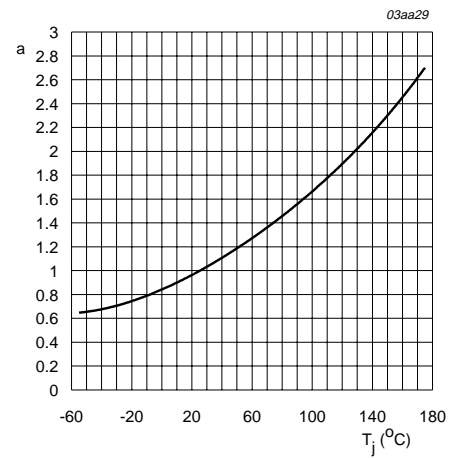
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristic: drain current as a function of gate-source voltage; typical values.



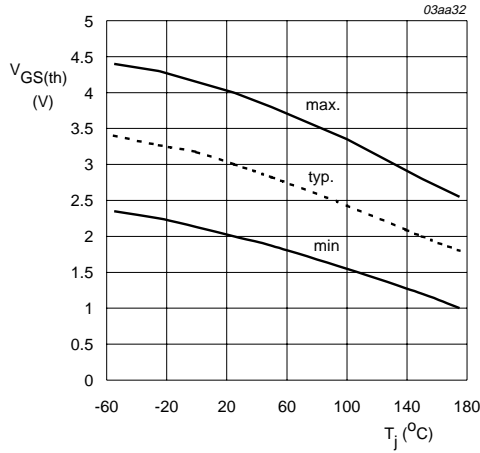
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



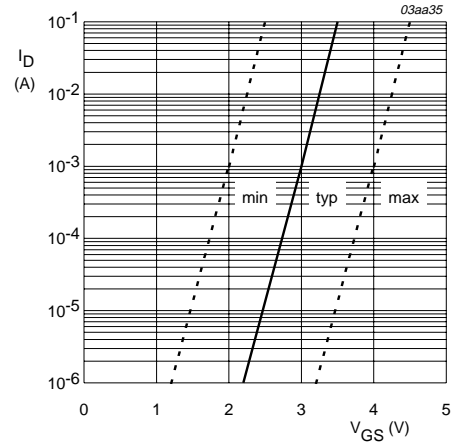
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



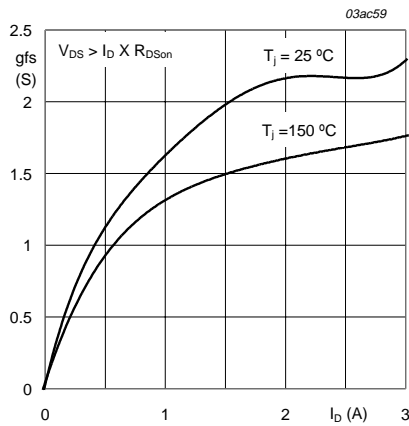
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



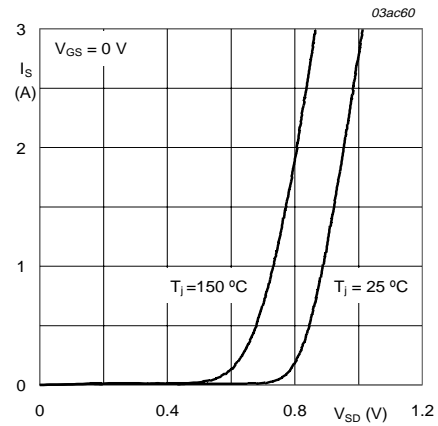
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



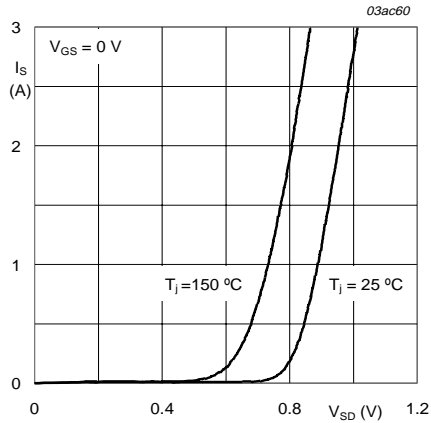
$T_j = 25 \text{ }^\circ\text{C}$ and $150 \text{ }^\circ\text{C}; V_{DS} > I_D \times R_{DS(on)}$

Fig 11. Forward transconductance as a function of drain current; typical values.



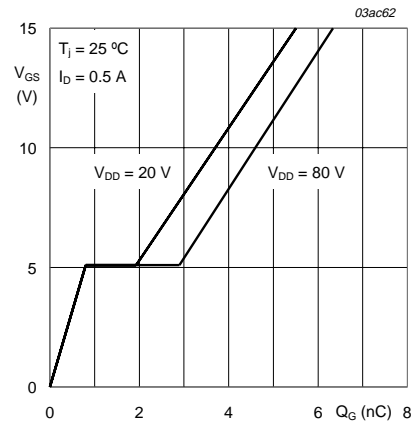
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{GS} = 0\text{ V}$

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 0.5\text{ A}$; $V_{DD} = 20\text{ V}$ and 80 V

Fig 14. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic surface mounted package; 3 leads

SOT23

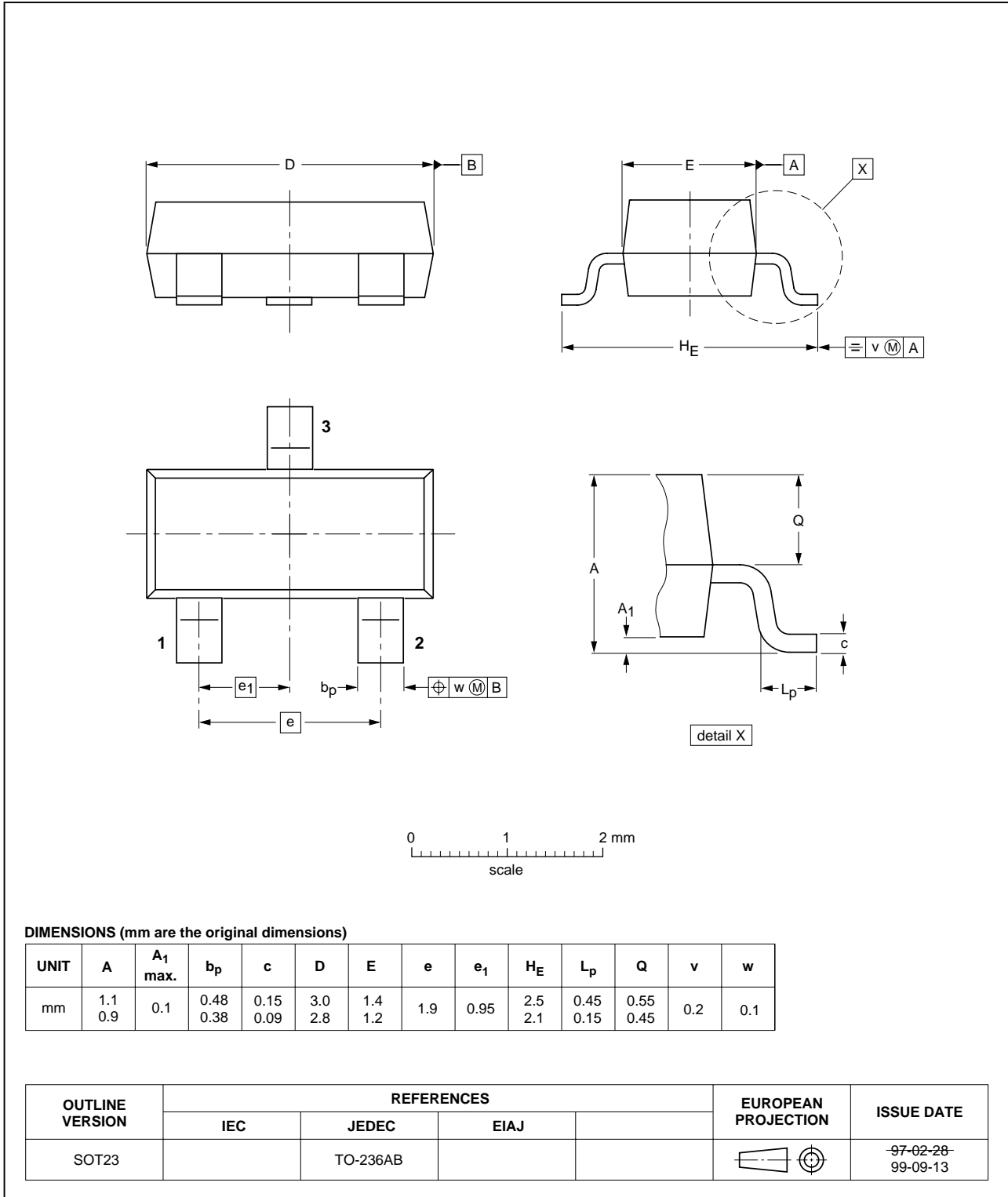


Fig 15. SOT23.

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20001109	-	Product specification; initial version

11. Data sheet status

Datasheet status	Product status	Definition ^[1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

12. Definitions

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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