

## Features

- **Industry Standard ATA / IDE Bus Interface**
  - Host Interface: 16-bit access
  - Supports 48-bit address feature set
  - Supports up to PIO Mode-6 <sup>1)</sup>
  - Supports up to Multi-Word DMA Mode-4 <sup>2)</sup>
  - Supports up to Ultra DMA Mode-6
- **Performance**
  - Sequential data read:  
Up to 60 MByte/sec
  - Sequential data write:  
Up to 30 MByte/sec
- **Power Management**
  - 3.3V power supply
  - Immediate disabling of unused circuitry without host intervention
  - Zero wake-up latency
- **Power Specification**
  - Active mode
    - 150mA typical (GLS85LP1032A)
    - 140mA typical (GLS85LP1016B)
    - 100mA typical (GLS85LP1008B)
    - 60mA typical (GLS85LP1004B)
    - 60mA typical (GLS85LP1002A)
  - Sleep mode  
500µA typical
- **Supports SMART Commands**
- **Robust Built-in ECC**
- **Expanded Data Protection**
  - WP#/PD# pin configurable by firmware for prevention of data overwrites
  - Data security through user-selectable protection zones
  - Security Erase feature
- **Integrated Voltage Detector**
  - Prevents inadvertent Write operations due to unexpected power-down or brownout
- **20-Byte Unique ID for Enhanced Security**
  - Factory pre-programmed 10-Byte unique ID
  - User-programmable 10-Byte ID
- **NAND Configuration**
  - 2 bits per cell (MLC)
- **Temperature Range**
  - Commercial: 0°C to 70°C
  - Industrial: -40°C to 85°C
- **91-ball BGA and LBGA Package** <sup>4)</sup>
  - 14mm x 24mm x 1.90mm, 1mm ball pitch, FTE (4 GB, 8 GB, 16 GB, 32 GB)
  - 14mm x 24mm x 1.45mm, 1mm ball pitch, LFTE (4 GB, 8 GB) **Note:** Devices using LFTE are not recommended for new designs.
  - 12mm x 24mm x 1.40mm, 1mm ball pitch, LBTE (2 GB)
- **All Devices are RoHS Compliant**

## Product Description

The GLS85LP1002A / 1004B / 1008B / 1016B / 1032A Industrial and Commercial Temp PATA NANDrive™ devices (referred to as “PATA NANDrive” in this fact sheet) are high-performance, fully integrated solid state drives. They combine a Greenliant NAND controller and 2, 4, 8, 16 or 32 GByte of NAND flash memory in a multi-chip package. These products are ideal for embedded and portable applications that require smaller form factor and more reliable data storage.

ATA-based solid state mass storage technology is widely used in GPS and telematics, in-vehicle infotainment, portable and industrial computers, handheld data collection scanners, point-of-sale terminals, networking and telecommunications equipment, robotics, audio and video recorders, monitoring devices and set-top boxes.

PATA NANDrive supports standard ATA/IDE protocol with up to PIO Mode-6<sup>1)</sup>, Multi-Word DMA Mode-4<sup>2)</sup> and Ultra DMA Mode-6 interface. PATA NANDrive provides complete IDE hard disk drive functionality and compatibility in a 14mm x 24mm BGA package or a 12mm x 24mm LBGA package for easy, space saving mounting to a system motherboard. These products surpass traditional storage in their small size, security, reliability, ruggedness and low power consumption.

The integrated NAND flash controller with built-in advanced NAND management firmware communicates with the host through the standard ATA protocol. It does not require any additional or proprietary software such as the Flash File System (FFS) and Memory Technology Driver (MTD).

PATA NANDrive provides a WP#/PD# pin to protect critical information stored in the flash media from unauthorized overwrites. PATA NANDrive is pre-programmed with a 10-Byte unique serial ID and has the option of programming an additional 10-Byte serial ID for even greater system security.

PATA NANDrive's advanced NAND management technology enhances data security, improves endurance and accurately predicts the remaining life of the NAND flash devices. This innovative technology combines robust error correction capabilities with advanced wear-leveling algorithms and bad block management to significantly extend the life of the product.

- 1) PATA NANDrive is capable of supporting PIO Mode-6, but Identify-Drive information report will show PIO Mode-4
- 2) PATA NANDrive is capable of supporting Multi-Word DMA Mode-4, but Identify-Drive information report will show MWDMA Mode-2

## 1.0 GENERAL DESCRIPTION

Each PATA NANDrive contains an integrated PATA NAND flash memory controller and NAND flash die in a BGA or LBGa package. Refer to Figure 2-1 for the PATA NANDrive block diagram.

### 1.1 Optimized PATA NANDrive

The heart of PATA NANDrive is the PATA NAND flash memory controller, which translates standard PATA signals into flash media data and control signals. The following components contribute to PATA NANDrive's operation.

#### 1.1.1 Microcontroller Unit (MCU)

The MCU transfers the ATA/IDE commands into data and control signals required for flash media operation.

#### 1.1.2 Internal Direct Memory Access (DMA)

PATA NANDrive uses internal DMA allowing instant data transfer from/to buffer to/from flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

#### 1.1.3 Power Management Unit (PMU)

The PMU controls the power consumption of PATA NANDrive. The PMU dramatically reduces the power consumption of PATA NANDrive by putting the part of the circuitry that is not in operation into sleep mode.

The Flash File System handles inadvertent power interrupts and has auto-recovery capability to ensure PATA NANDrive's data integrity. For regular power management, the host must send an IDLE\_IMMEDIATE command and wait for command ready before powering down PATA NANDrive.

#### 1.1.4 Embedded Flash File System

The embedded flash file system is an integral part of PATA NANDrive. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media writes and reads
2. Provides flash media wear leveling to spread the flash writes across all memory address space to increase the longevity of flash media
3. Keeps track of data file structures
4. Manages system security for the selected protection zones
5. Stores the data in flash media upon completion of a Write command (PATA NANDrive does not perform Post-Write operations, except for when the write cache is enabled)

#### 1.1.5 Error Correction Code (ECC)

High performance is achieved through optimized hardware error detection and correction.

#### 1.1.6 Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed for error reporting. During the product development stage, it is recommended to provide the SCI port on the PCB to aid in design validation.

#### 1.1.7 Multi-tasking Interface

The multi-tasking interface enables fast, sustained write performance by allowing concurrent Read, Program and Erase operations to multiple flash media.

## 1.2 SMT Reflow Consideration

The PATA NANDrive family utilizes standard NAND flash for data storage. Because the high temperature in a surface-mount soldering reflow process can alter the content on NAND flash, do not program PATA NANDrive before the reflow process.

## 1.3 Advanced NAND Management

PATA NANDrive's integrated controller uses advanced wear-leveling algorithms to substantially increase the longevity of NAND flash media. Wear caused by data writes is evenly distributed in all or select blocks in the device that prevents "hot spots" in locations that are programmed and erased extensively. This effective wear-leveling technique results in optimized device endurance, enhanced data retention and higher reliability required by long-life applications.

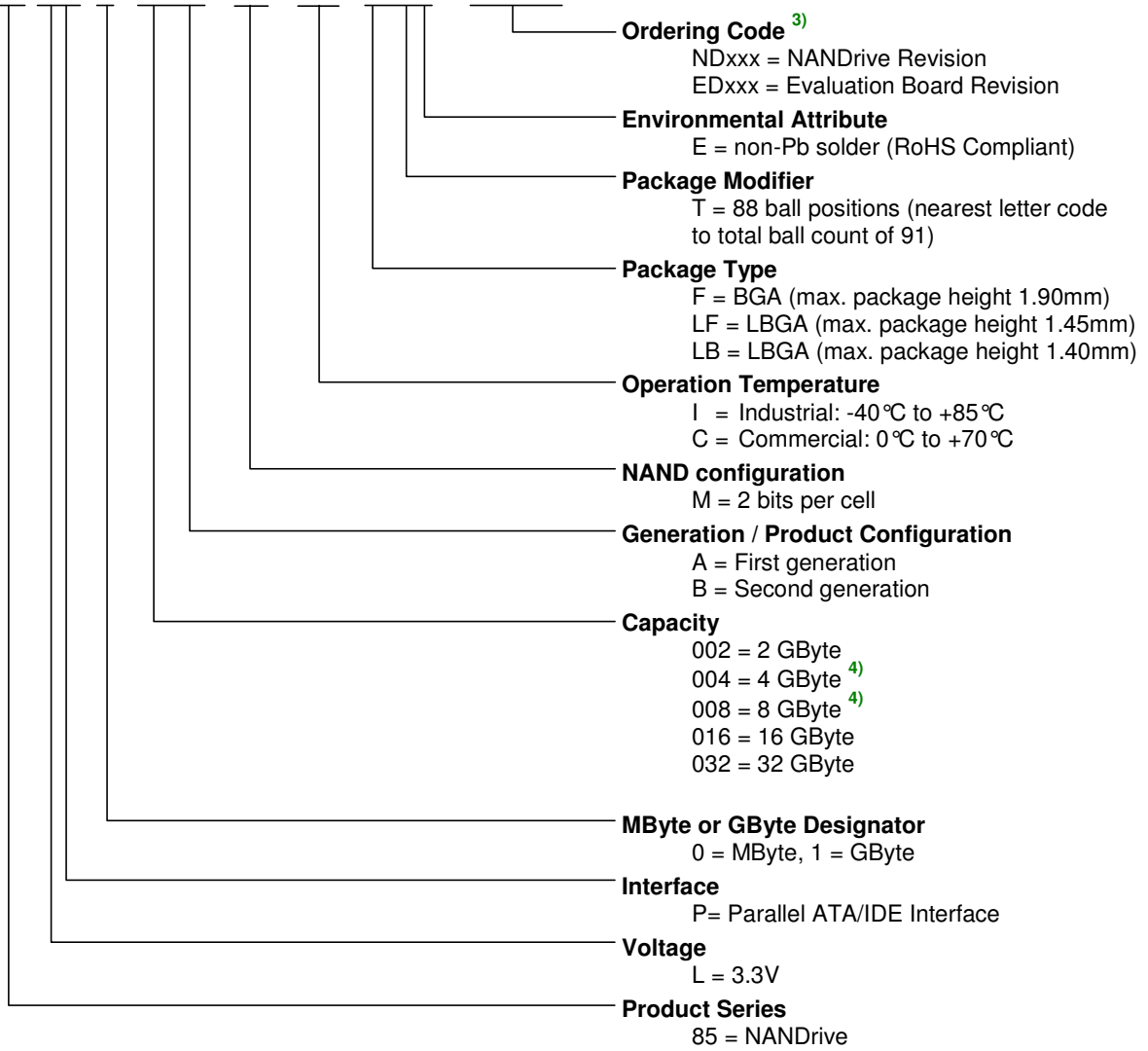
## 2.0 FUNCTIONAL BLOCKS



Figure 2-1: PATA NANDrive Block Diagram

### 3.0 PRODUCT ORDERING INFORMATION

GLS 85 LP 1 0xxB - M - C - LFTE - NDxxx  
 XX XX X XXXX - X - X - XXXX - XXXXX



- 3) For legacy NANDrive products, no ordering code is required. Note that the top side marking on the package typically does not include ordering codes (e.g. NDxxx), unless it is a special C-SPEC (custom specification) which is required by the end-customer to be marked on the device.
- 4) GLS85LP1008B and GLS85LP1004B currently have two packages available; FTE and LFTE. **Devices using LFTE are not recommended for new designs.**

### Valid Combinations

Valid product combinations are those that are in the mass production or will be in the mass production. Consult your Greenliant sales representative to confirm availability of the valid combinations and to determine availability of new product combinations.

**Table 3-1: PATA NANDrive Product Valid Ordering Numbers**

Capacity	Operating Temperature	Part Number	Package
2GB	Commercial (0 °C to 70 °C)	GLS85LP1002A-M-C-LBTE	LBTE, 12x24x1.40mm
		GLS85LP1002A-M-C-LBTE-ND000	LBTE, 12x24x1.40mm
	Industrial (-40 °C to 85 °C)	GLS85LP1002A-M-I-LBTE-ND000	LBTE, 12x24x1.40mm
4GB	Commercial (0 °C to 70 °C)	GLS85LP1004B-M-C-LFTE	LFTE, 14x24x1.45mm
		GLS85LP1004B-M-C-FTE-ND000 <sup>4)</sup>	FTE, 14x24x1.90mm <sup>4)</sup>
	Industrial (-40 °C to 85 °C)	GLS85LP1004B-M-I-FTE-ND000 <sup>4)</sup>	FTE, 14x24x1.90mm <sup>4)</sup>
8GB	Commercial (0 °C to 70 °C)	GLS85LP1008B-M-C-LFTE <sup>4)</sup>	LFTE, 14x24x1.45mm <sup>4)</sup>
		GLS85LP1008B-M-C-FTE-ND000 <sup>4)</sup>	FTE, 14x24x1.90mm <sup>4)</sup>
	Industrial (-40 °C to 85 °C)	GLS85LP1008B-M-I-FTE-ND000 <sup>4)</sup>	FTE, 14x24x1.90mm <sup>4)</sup>
16GB	Commercial (0 °C to 70 °C)	GLS85LP1016B-M-C-FTE	FTE, 14x24x1.90mm
		GLS85LP1016B-M-C-FTE-ND000	FTE, 14x24x1.90mm
	Industrial (-40 °C to 85 °C)	GLS85LP1016B-M-I-FTE-ND000	FTE, 14x24x1.90mm
32GB	Commercial (0 °C to 70 °C)	GLS85LP1032A-M-C-FTE	FTE, 14x24x1.90mm
		GLS85LP1032A-M-C-FTE-ND000	FTE, 14x24x1.90mm
	Industrial (-40 °C to 85 °C)	GLS85LP1032A-M-I-FTE-ND000	FTE, 14x24x1.90mm

<sup>4)</sup> GLS85LP1008B and GLS85LP1004B currently have two packages available; FTE and LFTE. **Devices using LFTE are not recommended for new designs.**

**Table 3-2: PATA NANDrive Evaluation Board Valid Ordering Numbers**

Capacity	Operating Temperature	Part Number	Form Factor
2GB	Commercial (0 °C to 70 °C)	GLS85LP1002A-M-C-40CN-K	Module with 40-pin ATA connector
		GLS85LP1002A-M-C-44CN-K	Module with 44-pin ATA connector
	Industrial (-40 °C to 85 °C)	GLS85LP1002A-M-I-40CN-ED000	Module with 40-pin ATA connector
4GB	Commercial (0 °C to 70 °C)	GLS85LP1004B-M-C-40CN-K	Module with 40-pin ATA connector
		GLS85LP1004B-M-C-44CN-K	Module with 44-pin ATA connector
	Industrial (-40 °C to 85 °C)	GLS85LP1004B-M-I-40CN-ED000	Module with 40-pin ATA connector
8GB	Commercial (0 °C to 70 °C)	GLS85LP1008B-M-C-40CN-K	Module with 40-pin ATA connector
		GLS85LP1008B-M-C-44CN-K	Module with 44-pin ATA connector
	Industrial (-40 °C to 85 °C)	GLS85LP1008B-M-I-40CN-ED000	Module with 40-pin ATA connector
		GLS85LP1008B-M-I-44CN-ED000	Module with 44-pin ATA connector
16GB	Commercial (0 °C to 70 °C)	GLS85LP1016B-M-C-40CN-K	Module with 40-pin ATA connector
		GLS85LP1016B-M-C-44CN-K	Module with 44-pin ATA connector
	Industrial (-40 °C to 85 °C)	GLS85LP1016B-M-I-40CN-ED000	Module with 40-pin ATA connector
		GLS85LP1016B-M-I-44CN-ED000	Module with 44-pin ATA connector
32GB	Commercial (0 °C to 70 °C)	GLS85LP1032A-M-C-40CN-K	Module with 40-pin ATA connector
		GLS85LP1032A-M-C-44CN-K	Module with 44-pin ATA connector
	Industrial (-40 °C to 85 °C)	GLS85LP1032A-M-I-40CN-ED000	Module with 40-pin ATA connector
		GLS85LP1032A-M-I-44CN-ED000	Module with 44-pin ATA connector

3.1 Package Diagrams  
 3.1.1 FTE Package

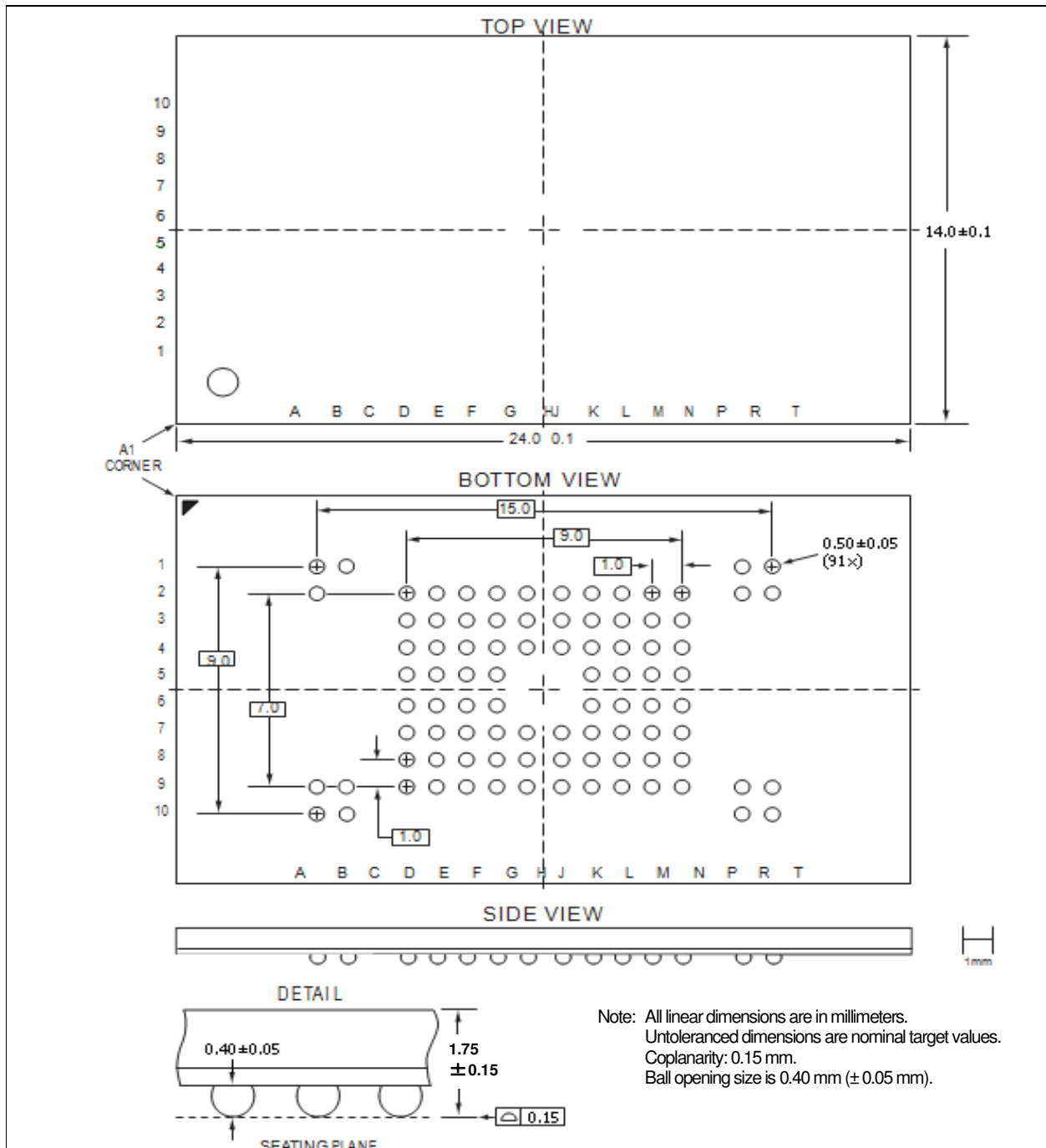


Figure 3-1: PATA NANDrive 91-Ball, Ball Grid Array (BGA) Greenliant Package Code: FTE

3.1.2 LFTE Package

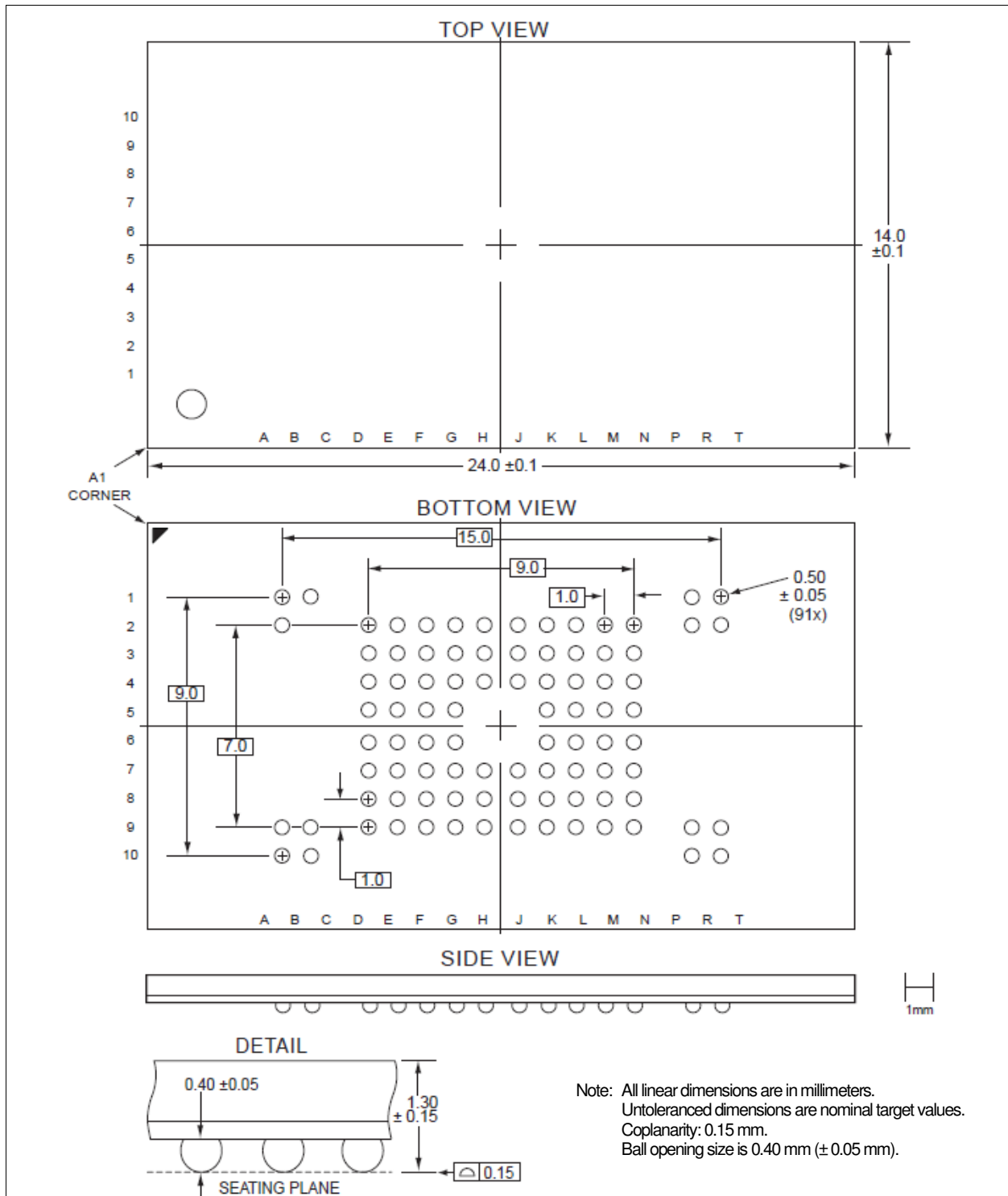


Figure 3-2: PATA NANDrive 91-Ball, Ball Grid Array (LBGA) Greenliant Package Code: LFTE



3.1.3 LBTE Package

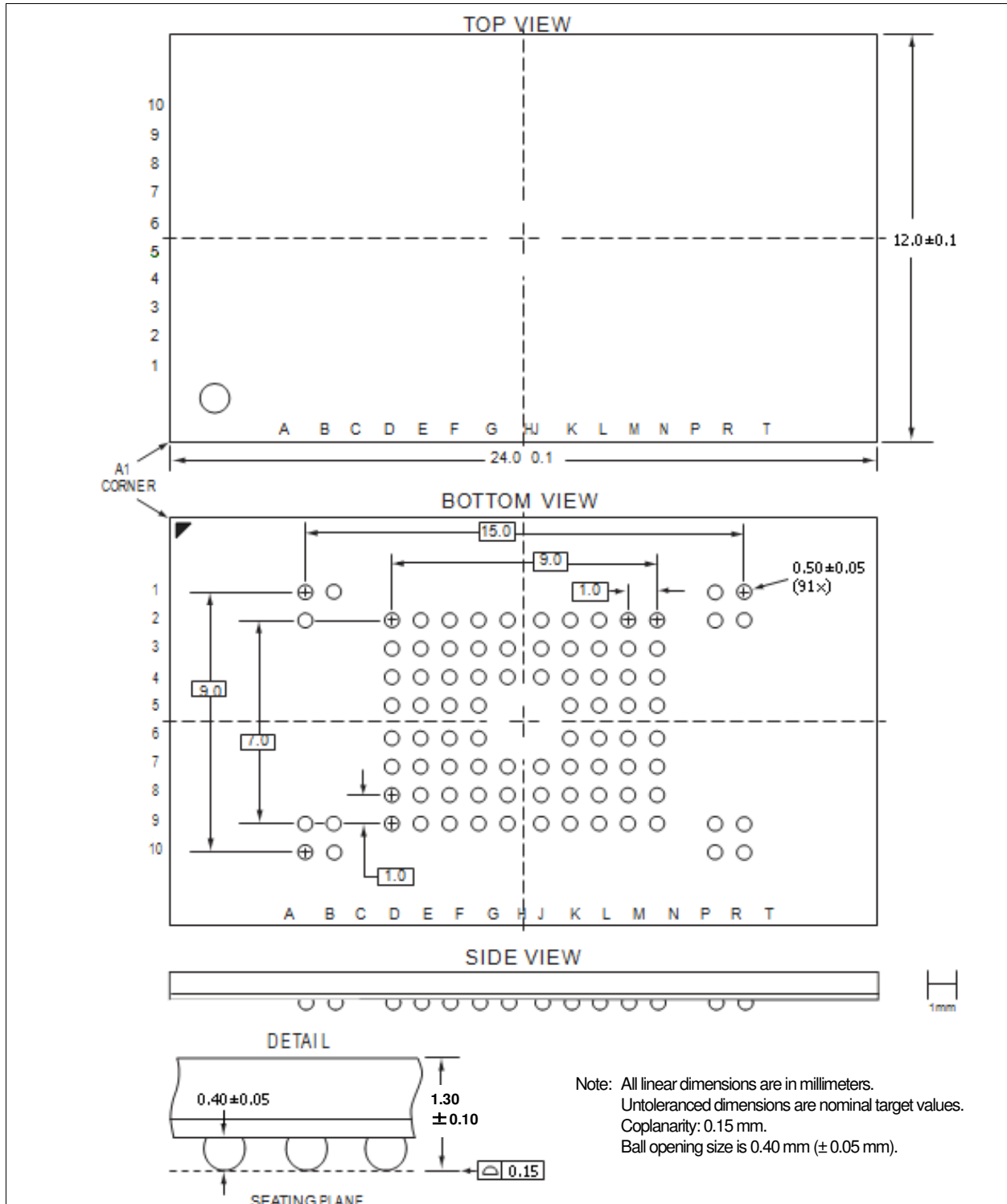


Figure 3-3: PATA NANDrive 91-Ball, Ball Grid Array (LBGA) Greenliant Package Code: LBTE



## Revision History

Revision	Description	Date
01.000	Initial release as Fact Sheet Merged information from two fact sheets into this document: - S71438-F_FactSheet_GLS85LP10xxB_C-grade_Rev02.000.pdf - S71422_FactSheet_GLS85LP1002A_C-grade_Rev01.000.pdf	July 25, 2012
02.000	Edits throughout document; Updated valid combinations in Section 4.0	December 20, 2012
02.001	Fixed typo on dimension of LBTE package on page1, from 14mm x 24mm x 1.40mm to 12mm x 24mm x 1.40mm; Placed Valid Combinations into table format in Section 4.0	February 12, 2013
03.000	Added GLS85LP1002A / GLS85LP1004B (rev.CE0); Removed Pin Assignments and Updated section numbering	September 5, 2013
03.001	Added "1mm ball pitch" on first page; Minor formatting edits throughout	February 21, 2014

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